A Novel Fast-view System for Multi-channel Remote Sensing Camera

Yongqiang Cui
School of Electronic Information, Wuhan University, Wuhan, China
E-mail: cuiyq@whu.edu.cn

Dingwen Wang
Institute of Microelectronics and Information Technology, Wuhan University, Wuhan, China
E-mail: wangdw@whu.edu.cn

Hua Xiong
Hubei Three Gorges Polytechnic, Yichang, China
E-mail: red_xiong@163.com

Shuai Zhang
School of Electronic Information, Wuhan University, Wuhan, China
E-mail: shuai173@whu.edu.cn

Xi Liu
School of Electronic Information, Wuhan University, Wuhan, China
E-mail: phyllis8866@gmail.com

***Abstract*—Multi-channel remote sensing camera fast-view system has complex structure and low versatility, and this paper presents a novel multi-channel remote sensing camera fast-view system, which could reduce development cycle and R&D costs. Taking Panchromatic and multispectral camera fast-view system as an example, this paper provides the improved system structure diagram, hardware design and software flow chart. Gigabit network interfaces and protocols are perfectly used to simplify system structure and improve system versatility. UDP protocol is implemented in FPGA hardware pipeline package and parse to improve transmission rate, and selective retransmission mechanism is devised to ensure data reliability. By means of increasing the network traffic at a steady rate up to 100MB/s, the experimental results meet the requirements of versatility design and rate at which the CCD image acquisition system asks for through hardware implementation and verification.**

***Index Terms*—remote sensing camera, UDP protocol, hardware pipeline, selective retransmission**

I. INTRODUCTION

With the rapid development of the space industry, space remote sensing camera plays a significant role in the field of military reconnaissance, resource exploration, and environmental management. Panchromatic and multispectral imaging technology has been fully developed due to its ability to obtain richer image information than the common cameras. QuickBird-2 satellite [1] launched by the United States in 2001 was equipped with one panchromatic camera and four multispectral cameras. ZY-3 satellite [2] equipped with three panchromatic cameras and one multispectral camera was launched by China on January 9, 2012.

In the development process of a remote sensing camera, the multi-channel fast-view system is needed for testing the performance of a camera. As an important part of the system, signal acquisition recorder is adapted to transfer image data to the graphics workstation. Embedded systems that adopt field programmable gate array (FPGA) as core is usually used in image acquisition. Currently, the data transmission interface between signal acquisition recorders and graphics workstation generally use PCIe or Ethernet. PCIe is an emerging bus interface which could get a high data transfer rate. CameraLink capture cards and fiber capture cards based on PCIe interface have been widely used in the image acquisition system [3-5]. However, because of the shortcomings such as short transmission distance and extending difficulty, the PCIe-based multi-channel fast-view system has complex structure and low versatility. The system not only needs PCIe acquisition card to receive data, but also needs a special multiplexing equipment to distribute data. These will lead to increased costs and manpower. Ethernet is the most widely used communication protocol standard, which has the advantages of universality and transmission in high speed and long distance. In FPGA applications, because of the Ethernet protocol stack implemented by SOPC [6], the transmission rate is low and the protocol is redundant. The Ethernet protocol stack is not suitable for high-speed image data transmission.

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In this paper, a novel multi-channel camera fast-view system is proposed by adopting Gigabit network interface communication and improving the speed and reliability of UDP protocol. The paper is organized as follows: In section II, a novel multi-channel camera fast-view system is introduced briefly. In section III&IV, the method used to realize hardware pipeline packaging and parsing of UDP protocol in FPGA, as well as to ensure the reliability and efficiency of system is discussed. In sections V, the results using the improved multi-channel CCD image acquisition system are presented. Section VI concludes the paper.

This paper has been improved in the following aspects. First, the system adopts Gigabit network interface communication, which can complete the transmission of a plurality of image acquisitions and the graphic workstation by using the general cheap Gigabit network switch. Second, the UDP (User Datagram Protocol) protocol achieves a hardware pipeline packaging and parsing in FPGA. Third, as UDP protocol is a connectionless transmission protocol, the high efficient selective retransmission mechanism is used to solve the problem of data corruption caused by dropped frames and bit errors in the transmission process, so that the data transmission becomes more reliable. Fourth, universal and modular design improves the reusability and scalability of the system and can be widely used in remote sensing camera test equipment.

II. System Design and Implementation

Panchromatic and multispectral remote sensing camera, for example, consists of 8-channel CCD cameras including 4-channel panchromatic cameras and 4-channel multispectral cameras which have LVDS Level outputs. Panchromatic camera pixel value is 8192, the bit width is 8bit, the clock frequency is 100MHz, multispectral camera pixel value is 8192, the bit width is 8bit, and the clock frequency is 25MHz. Thus, maximum data transmission rate of panchromatic cameras is 800Mbps; maximum data transmission rate of multispectral cameras is 200Mbps. The total rate is up to 4Gbps.

As shown in Figure 1, the multi-channel fast-view system includes four parts: eight signal acquisition recorders, a Gigabit network switch, graphics workstation (host) and LCD monitor. CAT-5 cable is used as connector in both sides of Gigabit network switch. Each signal acquisition recorder has an independent IP address. The host can access each signal acquisition recorder through the switch to set the parameters and read status, and receive the image data of each channel.

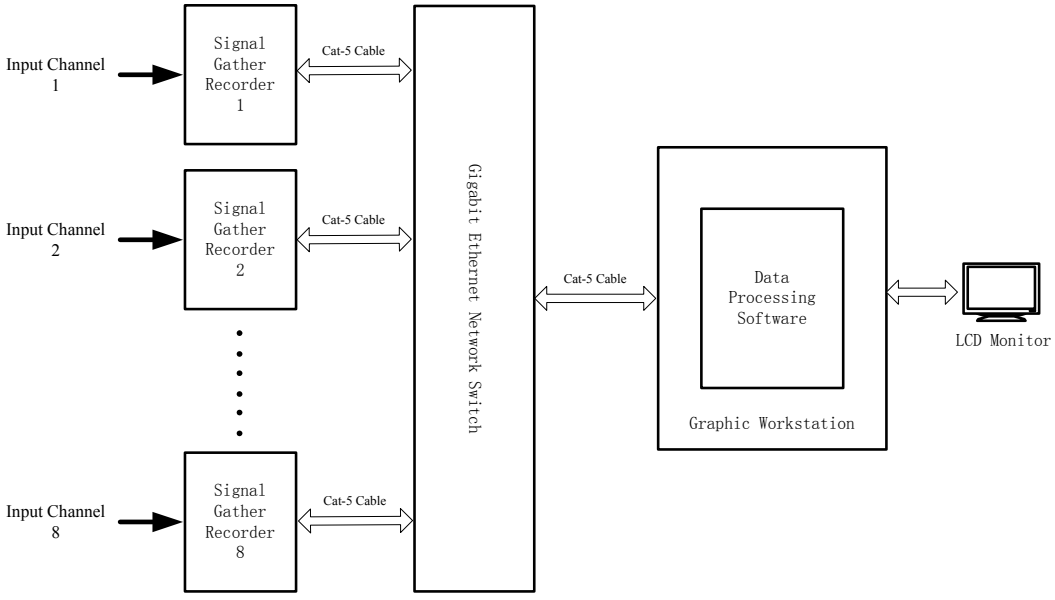

Figure 1. Block diagram of system

Realization of signal acquisition recorder block diagram is shown in Figure 2.

The important modules are described as follows. The command management module receives and parses the parameters and instructions from the host. Data processing module, on the one hand, deals with acquisition and sampling of the signal, on the other hand, deals with direct transmission, storage of real-time data and playback of stored data. In order to improve the storage speed, RAID0 [7] controller is employed to make parallel operations on 4 SSDs.

The system pipelines the UDP protocol used by FPGA hardware logic circuit, greatly improving the packaging and parsing rate of the UDP datagram. MAC layer is realized by Triple Speed Ethernet MegaCore [8,9] providing by FPGA to meet the IEEE 802.3 [10] Ethernet standard, which can provide high data throughput rates and configure their work in the GMII mode. PHY layer is achieved by using Marvell's 88E1111 [11]. The network

isolation transformer ensures reliable transmission of the signals. Network interface selects the generic RJ45 connector and network cable uses CAT-5 cable.

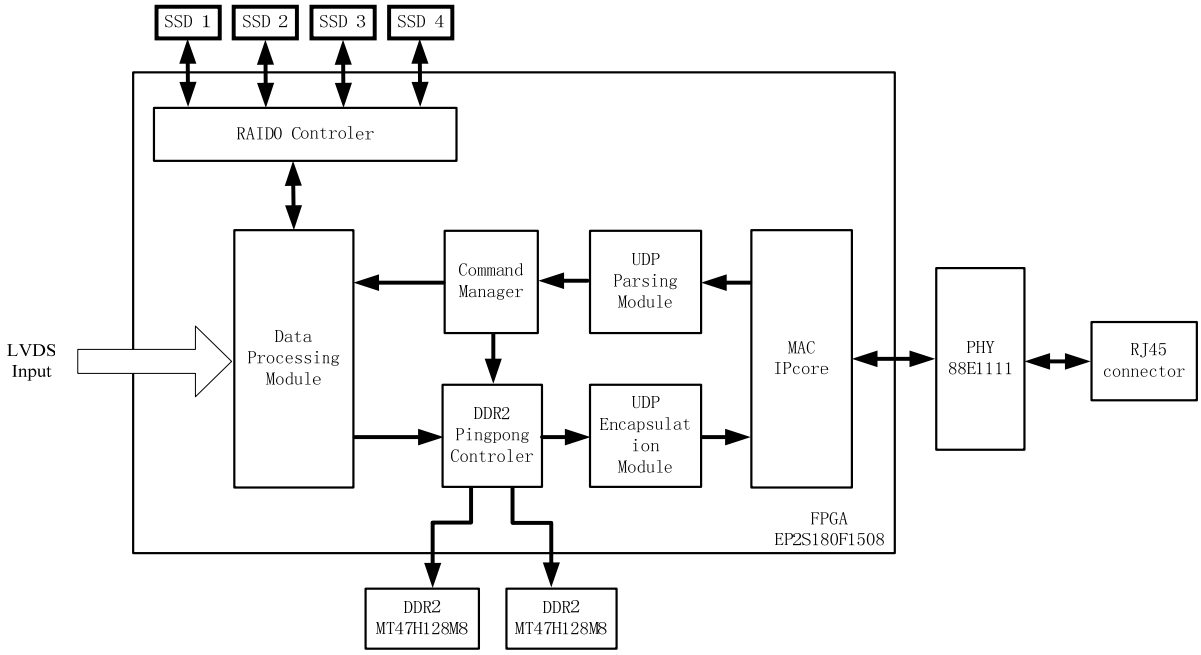

Figure 2. Block diagram of the signal acquisition recorder

III. Hardware Pipeline Implementation Of Udp Protocol

UDP protocol is a connectionless transport layer protocol in TCP/IP architecture [12], providing simple transaction-oriented unreliable messaging services. In the application process, UDP protocol does not have the consumption of establishment of connection , removal of connection and confirmation of message in TCP, so the communication rate is high, and UDP supports massive concurrent connections. Thus, UDP protocol is very suitable for application in fast-view system.

Currently, the image acquisition system usually adopts FPGA as the core in embedded systems. Such system has incomparable advantages in processing high speed and massive data, but supports the universal protocol poorly. In implementation of network communication in FPGA, it is popular to use SOPC (System on a Programmable Chip). For example, in Altera's FPGAs, the network protocol stack, such as NicheStack [13] or LWIP [14] protocol stack can be implemented by embedded real-time operating system (RTOS) based on NIOS II microprocessor [15]. Due to the limited efficiency in soft-core performance and protocol stack, they are not suitable for data transmission.

The problem will be solved while special hardware logic circuit is built to implement UDP protocol in FPGA. UDP datagram is composed of MAC header, IP header, UDP header, user data and MAC CRC checksum. The length of each component is shown in Table 1.The length of the Ethernet data frame ranges from 64bytes to 1518bytes, so that the user data length n must be satisfied: $18 \le n \le 1472$.

UDP datagram structure is shown in Figure 3. As shown in the figure, a UDP datagram consists of the following three parts: head part, user data and CRC checksum value. In the IEEE 802.3 standard, the CRC produce polynomial FCS (x) as follows:

Table I.
Datagram Length Of Each Part

MAC header	IP header	UDP header	User data	MAC CRC
14 Bytes	20 Bytes	8 Bytes	n Bytes	4 Bytes

$$FCS(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x^{1} + 1$$

In this design, the calculation of the CRC checksum value is calculated by Triple Speed Ethernet MegaCore, and is added to the tail of the data packet. There are three works to be completed: produce a header, populate user data, calculate and write the UDP checksum.

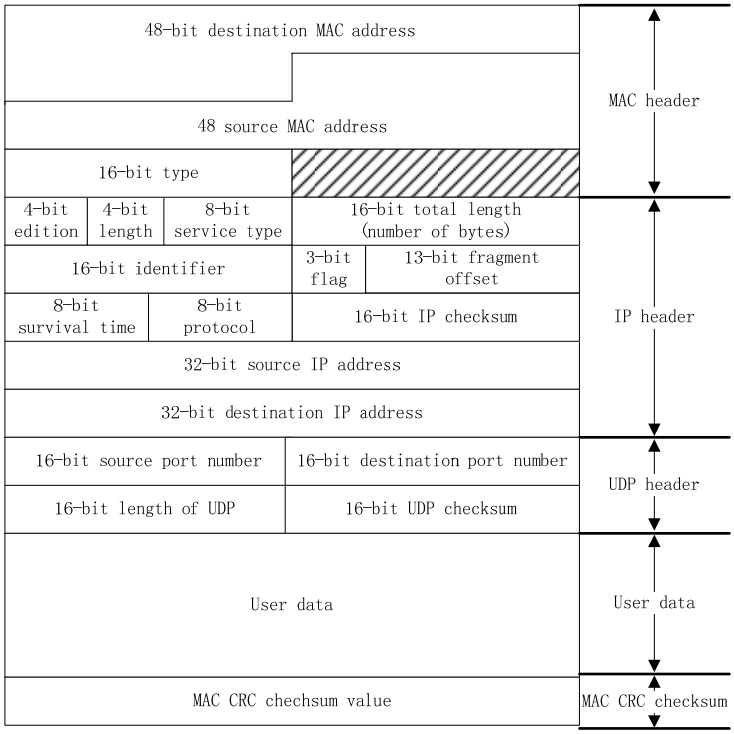

Figure 3. UDP datagram structure

For the generation of the header, Figure 3 shows that MAC header, IP header, UDP header of the contents would be determined when some fields' content in the figure 3 can be determined except for UDP checksum. In this way, it is possible to design a module to construct UDP datagram header module whose inputs are destination MAC address, source MAC address, destination IP address, source IP address, source port number, destination port number and length of the user data, while the output is the header of UDP datagram. The content and explanation of each header field of the UDP datagram can be seen in Table 2. Type selects IP datagram and Version selects universal IPv4. Protocol fills 0x11, namely select the UDP datagram. Notably, the total length is the total number of bytes of the datagram, and the UDP length is the number of bytes of the UDP header and the user data. It can be seen that most of the fields are fixed except for some need to be configured. IP checksum is calculated by the module based on IP header. IP checksum can be written directly to the IP checksum field, and the UDP checksum need UDP header and user data to calculate.

TABLE II
UDP DATAGRAM HEADER CONTENT

Name	Content	Explanation
Destination MAC address	User settings	Null
Source MAC address	User settings	Null
Type	0x0800	IP datagram
Version	0x4	IPv4
length of header	0x5	20bytes
Type of service	0x00	TOS field, no use
Total length	20+8+n，n is set by the user	Length of IP datagram
16-bit identifier	0x25eb	Not in use
3-bit flag	0x0	Fragment flag, not in use
13-bit offset	0x00	No use
Survival time	0x40	TTL field is set to 64
Protocol	0x11	UDP Protocol
IP checksum	Calculate	IP header checksum
Source IP address	User settings	Null
Destination IP address	User settings	Null
Source port number	User settings	Null
Destination port number	User settings	Null
UDP length	8+n, n is set by the user	Length UDP datagram
UDP checksum	Calculate and populate the initial value	UDP header and user data checksum

In order to achieve the pipeline filling of user data, system calls a 4KB RAM module at both ends of the UDP encapsulation module. RAM is divided as two 2KB RAM by the highest address selecting 0 or 1. As the maximum of UDP datagram is 1518 bytes, size of 2KB can meet the requirements of cache. Ping Pong operation of the RAM is neither blocking inputs nor affecting outputs. So that the data processing module can maximize performance, and the pipeline processing of data is completed.

When the UDP encapsulation Module populates user data, it needs to calculate the UDP checksum. UDP checksum and IP checksum calculation methods is both checksum coverage field of each 16-bit binary counter code summation and the result is the checksum. The length of the user data in UDP datagram may be odd, which can add a filler byte 0 to calculate. Receiver operates the sum of an anti-code of checksum coverage field after received the data packets. If the result is 0xFFFF, it indicates that the received data is correct while the other is wrong. UDP encapsulation module calculates the new UDP checksum according to the header checksum, initial value and user data filled constantly, and then write the results into UDP checksum field.

IV. The Realization Of Selective Retransmission Mechanism

UDP protocol is connectionless-oriented service, which is not concerned about the state of the channel and receivers when sending packet. UDP is a relatively unreliable communication protocol, and there may be loss of data frames, bit errors and disorder phenomena. UDP protocol does not consider these issues in the network transmission, so it can save a lot of system resource consumption on network status confirmation and data confirmation, thereby increasing the UDP protocol transmission rate and network efficiency. Fast-view system should make full use of the advantages of UDP protocol and guarantee the reliability of UDP traffic, and also implement network traffic flow control and congestion control.

For the unreliability of UDP protocol, the article has designed a mechanism to overcome these problems.

Host reads the data of multiple signal acquisition recorders in cycling, thus ensuring that only one node can send data frames to the host through exclusive channel at the same time. Therefore, it will not collide, fundamentally eliminating network congestion.

The signal acquisition recorder uses two DDR2 SDRAM(Micron MT47H128M8 128M×8-bit DDR2 SDRAM, its structure is divided into eight blocks, each block has 8K rows, each row has 1K column. [16]). Each MT47H128M8 can reach 120MB/s storage rate so that it can fully meet the requirements of the system. Ping Pong operation of the both DDR2 SDRAM improves efficiency. The host can set the cache size to balance the data flow of each channel.

As in the design, CCD Camera row of pixels is 8192, bit width is 8bit, an image has 2048 rows, so the image size is 16MB.The cache size is set to 16MB as a packet of data. To improve UDP datagram, user data is set to 1032 bytes in which the first 8 bytes are data header and the latter 1024 bytes are image data, so that sending an image needs a total of 16384 UDP datagram. In the data header, the first 4 bytes is a transmission flag which is set by the host to distinguish the transmission to the others, and the latter 4 bytes is the frame counter, recording the position of the frame data in a packet data, such as the present example for 0-16383.

After receiving a packet of data, the host detects the frame counters to judge whether there is disorder or loss of frames, and detects the IP checksum, the UDP checksum, the CRC checksum value to judge whether there are bit errors. If there is disorder, the host can rearrange a packet of data based on the frame counter. For the problem of loss of frames and bit errors, usually, there are Back N frame retransmission and selective retransmission two mechanisms to overcome. Back N frame retransmission is that when a frame error occurs, retransmit N frames following the problem frame; selective retransmission is that when frame error occurs, retransmit the problem frames without subsequent frames. The Back N frame retransmission mechanism is easier to achieve than selective retransmission mechanism, but selective retransmission mechanism can provide higher bandwidth efficiency. The system uses selective retransmission mechanism, shown in Figure 4. In order to further improve the efficiency of retransmission mechanism, system design can support retransmission of a single frame and retransmission of successive frames.

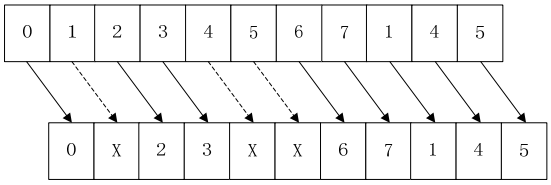

Figure 4. Selective retransmission mechanism

Host work flow chart is shown in Figure 5. First of all, the host request to send data. If there is no data entry in regular time, the host requests to resend the packet data; when loss of frames or bit errors occurs in receiving data, selective retransmission mechanism ensures the integrity of data.

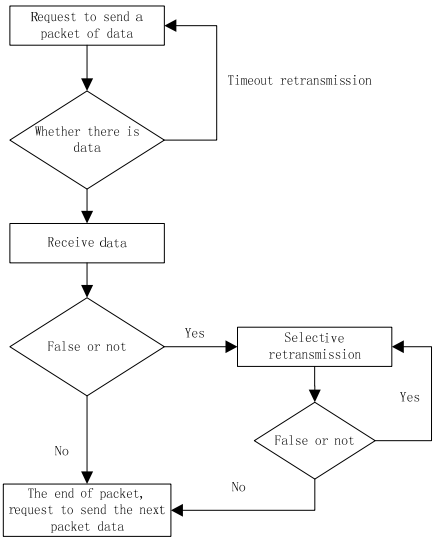

Figure 5. Host flowchart

V. Hardware Verification And Experimental Results

Signal acquisition recorder implements the UDP datagram encapsulation and parsing in the FPGA. According to the previous analysis of UDP datagram encapsulation, the UDP datagram hardware pipeline package design is shown in Figure 6.

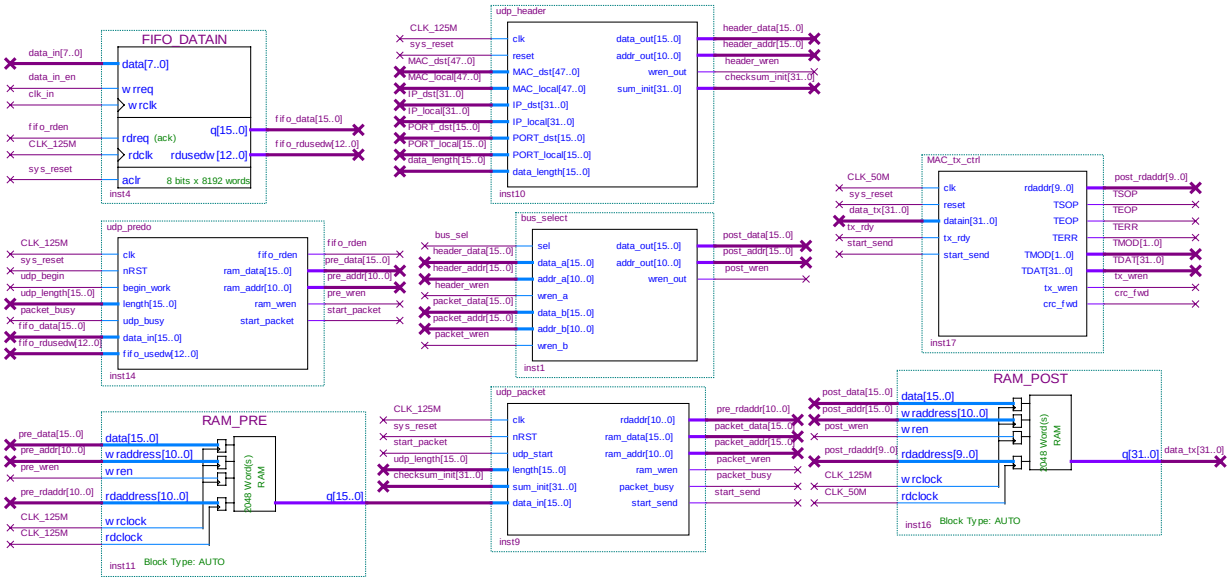

Figure 6. FPGA top-level schematic design

In the top-level design, an 8KB of FIFO is set to cache user data, udp_header module is header generating module, udp_packet module is UDP encapsulation module, RAM_PRE and RAM_POST are two input and output RAM. MAC_tx_ctrl meets the Triple Speed Ethernet MegaCore timing requirement. The Signaltap II embedded logic analyzer [17] is used to collect and analyze output data .As shown in Figure 7, it proves that UDP datagram encapsulation is correct. UDP protocol encapsulation and parsing use this hardware pipeline to achieve. The main modules work at frequency of 125MHz. The entire process uses pipelining operation to ensure the speed of data processing to meet the requirements of gigabit network 1000Mbps.

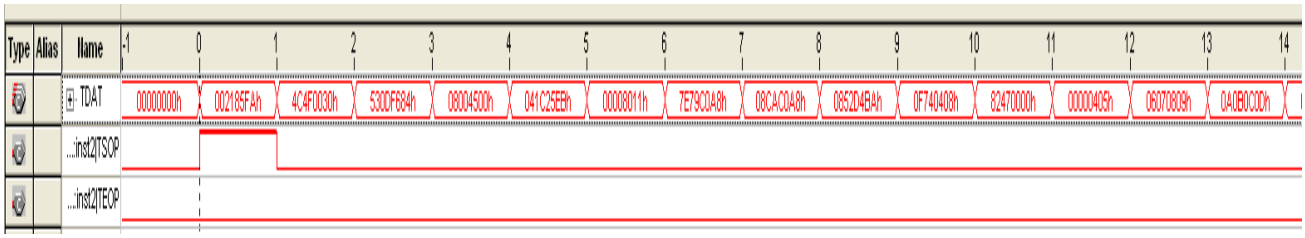

Figure 7. Signaltap II logic analyzer result

The network utilization is shown in Figure 8 when multi-channel remote sensing camera fast-view system transmits images. It can be seen that the average stable network utilization is up to 80%, namely, reliable data transmitting rate is up to 100MB/s.

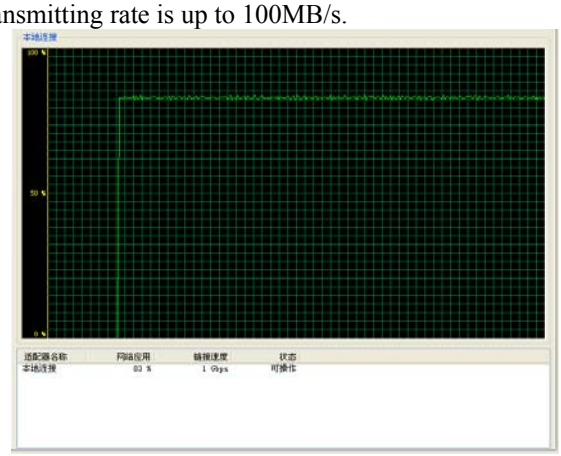

Figure 8. Network utilization

When multi-channel remote sensing camera fast-view system is working, host reads image data of 8 channels in cycling and displays on the LCD monitor. Experimental results are shown in Figure 9. The left side of the diagram is 4-way panchromatic images and the right side is 4-way multi-spectral images.

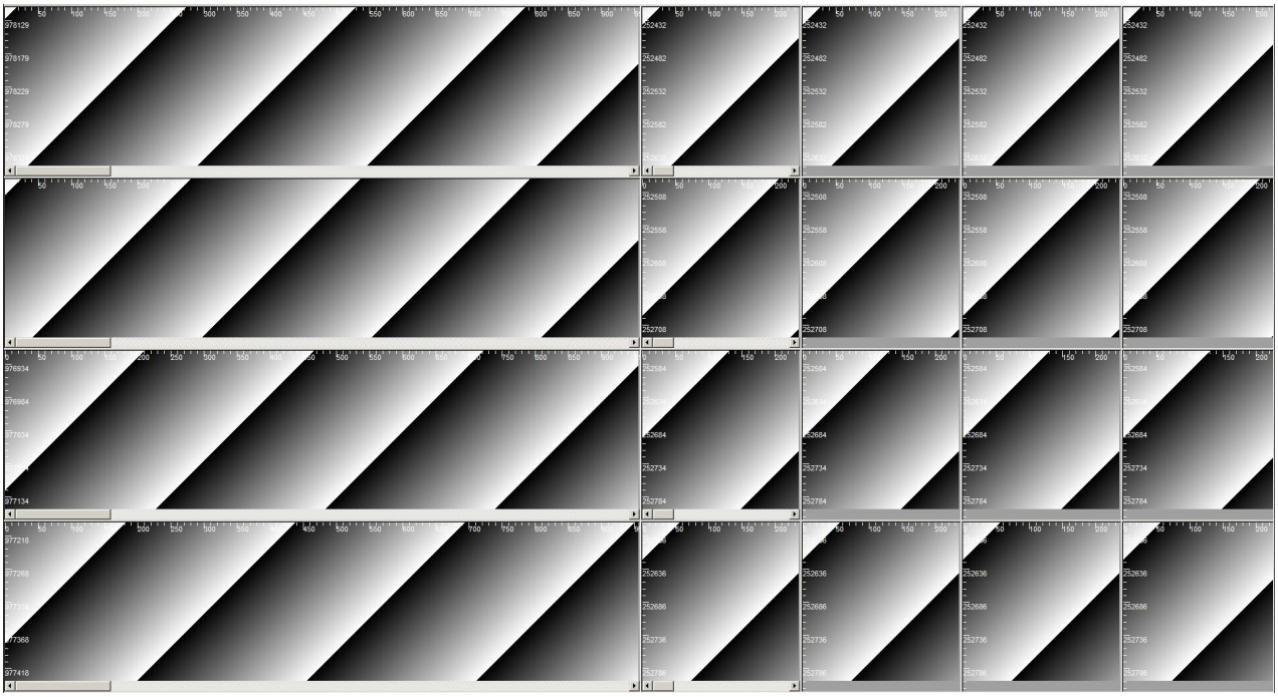

Figure 9. Panchromatic/multi-spectral camera real-time image

VI. CONCLUSION

This paper presents an improved multi-channel remote sensing camera fast-view system. FPGA-based signal acquisition recorder has achieved CCD image signal acquisition and network communication.UDP protocol encapsulation and parsing has been implemented by hardware pipeline which greatly enhances the data transfer rate. Furthermore, the high efficient selective retransmission mechanism is designed to overcome the instability of UDP protocol. A steady rate of up to 100MB/s can meet the requirements of image transmission. The system can complete the high-speed data transmission between graphics workstation and multiple signal acquisition recorders through generic

gigabit network switch. Utilization of Gigabit network interface and protocol enhances the versatility and scalability of the system, also reduces development cycles and R&D costs. The modular design allows that the system can be widely used in remote sensing camera fast-view system.

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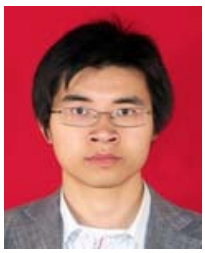
Yongqiang Cui, Shanxi, China, 1988, Ph.D. Candidate, Electronic Information School, Wuhan University Interest research: Signal Process, Satellite Communications



Dingwen Wang, Hubei, China, 1981, Associate Professor, Institute of Microelectronics and Information Technology, Wuhan University. Interest research: Intelligent Computing, Image Processing and software engineering

Hua Xiong, Hubei, China, 1978, Engineer, Hubei Three Gorges Polytechnic. Interest research: Signal Process, Artificial Intelligence

Shuai Zhang, Inner Mongolia, 1987, Ph.D. Candidate, Electronic Information School, Wuhan University Interest research: Signal Process, High Speed Circuit

Xi Liu, Hubei, China, 1991, Graduate. Candidate, Electronic Information School, Wuhan University Interest research:Hopping communication, Beidou time service