A Cluster-based Hierarchical Partitioning Approach for Multiple FPGAs

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***Abstract*—Most high performance computing systems are large-scale computing systems, and consist tens of thousands computing nodes with superior capabilities. FPGAs are able to accelerate large scope and complicated computing with flexible configurations. More and more companies and research institutions integrate multi-FPGAs into high performance computing systems to get a better trade-off between high-performance and low power. How to design an effective topology for these integrated multi-FPGAs according different applications has become a key problem in this area. Acluster based architectureand corresponding partitioning approach are proposed in this paper. The proposed hierarchical topology taking full advantages of both traditional metallic lines and emerging interconnections to implement one-hop local communication within the cluster and one-hop global high-speed communication between clusters. The case study proved that the proposed architecture and partitioning approach can implement the fast mapping from the design to real computing system with multi-FPGAs, and accelerate the realization of high performance reconfigurable computing systems.**

***Index Terms*—High performance computing, multi-FPGA architecture, FPGA partitioning, emerging interconnections**

I. Introduction

Most high performance computing systems are large-scale computing systems, and consist tens of thousands computing nodes with superior capabilities [1]. To satisfy the challenges in performance and energy consumption, the mechanisms such as NUCA (Non-uniform cache architecture) and page-recoloring[2][3]are adopted in these large-scale systems[4][5], and the communication pattern tends to non-uniform and heterogeneous. Cluster-based architectures have become the mainstream in the design of high performance computing systems. As shown in Figure 1, up to 80% computing systems adopt the cluster-based architecture, which stands in a monopolistic place in the ranking list [6].

As the advanced requirements for High Performance Computing (HPC), not only the need for reliable and high performance computingincreased, but also the demand forlow cost, low energy consumption and high speedare on the increase. The traditional high performance computing systems usually cost several millions or even up to tens of billions of dollars, and hard to upgrade. With the improvement of CMOS technology, FPGA (Field Programmable Gate Array) is able to accelerate large-scale computing, and dramatically reduce the computing power and cost with flexible configurations. More and more companies and research institutions integrate multi-FPGAs into high performance computing systems to get a better trade-off between high-performance and low power[14][15].The interconnectionnetworksareusually customized for special applications, and varies considerably for different high performance computing systems. How to design an effective topology for these integrated multi-FPGAs according different applications has become a key problem.

The interconnection network is the channels for data flows and communications between the processing nodes in the computing systems, which plays a key role for the performance improvement of HPC. Conventional VLSI mainly adopts metallic lines with low impedance and high conductivity to implement the interconnections of on-chip components. Traditional metallic interconnects face serious transmission delay, bandwidth density issues and power consumption problems asthe expanding scale of circuits. On the other hand, emerging interconnections such as optical interconnects and RF interconnects have become the alternative technologies to replace the traditional RCs [7]-[9]. These emerging interconnections are able to achieve one-hop effective communications between long distance nodes with low power and high bandwidth, and have been widely used to implement the communicationsbetween computing cabinets.The researches to implement the interconnections within computing cabinets, between boards and on chips have been also explored recently[31][32][33][34], and obvious achievements have been obtained. However, they cannot completely replace the traditional RCs in a short time due to the design challenges such as transmission interference and high sensitivity to temperature[10]. The hybrid architectures that composite traditional RCs and emerging interconnections have become an efficient

Manuscript received December 25, 2013; revised March 25, 2014; accepted April9, 2014.

doi:10.4304/jcp.9.9.2173-2180

implementation approach during the technological transition period.

To target the challenges in performance, cost and energy consumptionin large scale communications of HPCs, and exploit the local[11][12] and heterogeneous[13] properties of future large scale communications, we propose a cluster based hierarchical topology and corresponding partitioning approach. The proposed hierarchical topology taking full advantages of both traditional metallic lines and emerging interconnections to implement one-hop local direct communication within the cluster and one-hop global high-speed communication between clusters.The customized interconnection topology can be designed according different applications through the proposed approach and be implemented through the fast mapping from the design to the real high performance computing system with multi-FPGAs.

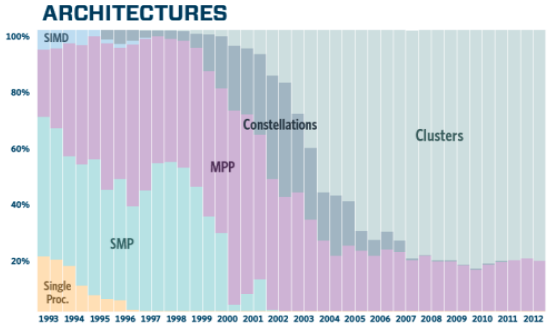


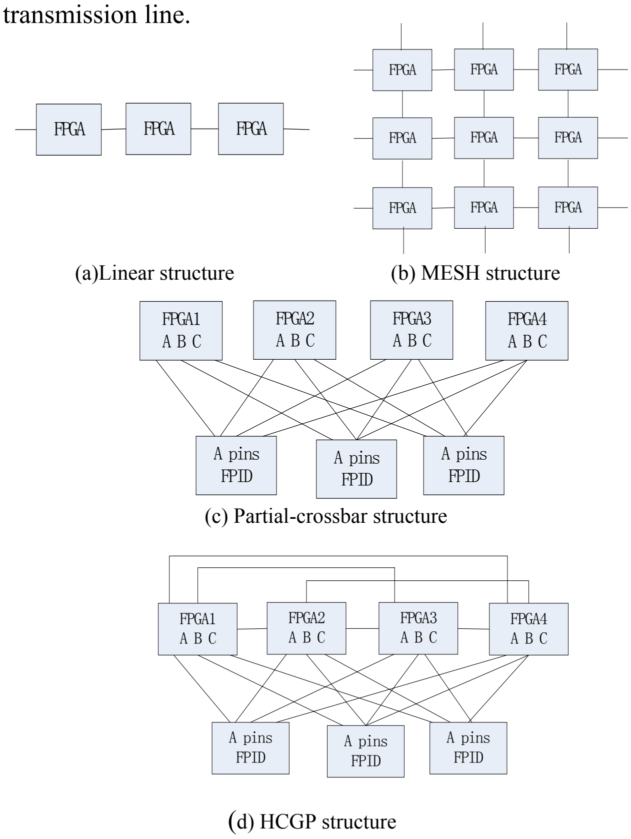
Figure 1 The architecturesdistribution of HPCs in world TOP500[6]

II.The Proposed Topology for Multi-FPGAs Oriented to HPCs

The topology of multi-FPGAs is defined as the connections between the multiple FPGAs. Currently traditional typical topologies include linearstructures[17][18],MESHbased structures[19][20][21][22],partial-crossbar structures[23][24][25] and Hybrid Complete Graph Partial-crossbar (HCGP) structures[26][27][27][29][30] (As shown in figure 2). These interconnection architectures have respective advantages to satisfy different application requirements, but might face serious scalability and routing problems for future large scale computing systems integrated tens to thousands of FPGAs.

As shown in figure 3, our proposed topology is a cluster based hierarchical architecture which consists two tier communication layers: local network (intra-cluster) and global network (inter-cluster). The interconnections within the cluster is based on traditional metallic wired links, while the inter-cluster interconnects are implemented by emerging high speed interconnections such as RF-I and optical interconnection. The local network is completely interconnected and all the nodes in the same cluster can communication each other directly. There is a relay node in each cluster to achieve the interconnection between local communication and global communication. The relay node can be designed with high performance FPGAs to integrate partial computing functions while in charge of the cross-talk communication, or can be implemented with small scale FPGAs to be only responsible for the communications between two layers. If the nodes want to communicate with other nodes in different clusters, they need to transfer the message to the local relay node firstly, then the local relay node transmit the coded message through the high speed RF channel to the relay node of the destination cluster, and finally forwards the message to the destination node by the relay node in destination cluster, so 3 hops needed for inter-cluster communications.

In traditional topologies, the communication between FPGAs that non-directly connected requires routing through intermediate FPGAs. Although these routing algorithms are designed to be simple and efficiency [35][36], communication latency will increase greatly as the computing system scales due to the limited bandwidth and massive routing hops. In our proposed architecture, the FPGAs in the same cluster communicateeach other directly through traditional interconnection, and the FPGAs in different clusters communicate through express RF-I (Radio Frequency Interconnect).The design can be scaled flexibly through the cluster augment with our proposed architecture, and only 2 intermediate hops needed for long distance communications. Besides, the RF-I between clusters divides bandwidth into frequency domains, each becoming a narrow-band signal, which saves power and improves bandwidth efficiency by sending many simultaneous streams of data over a single transmission line.



(a)Linear structure (b) MESH structure

(c) Partial-crossbar structure

(d) HCGP structure

Figure 2 Typical topologies for multi-FPGAs

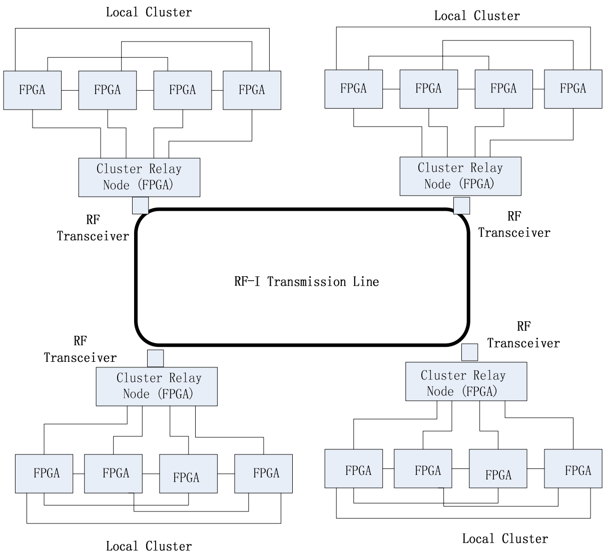


Figure 3 Cluster based hierarchical architecture for multiple FPGAs

III.CLUSTER BASED PARTITIONING APPROACH FOR MULTI-FPGAS

To minimize the average communication latency of the cluster based multi-FPGA system, we propose a partitioning approach based on the former researches[37][41][42][43][44][45] to concentrate the communications within the clusters to minimize the global communication required between clusters. The proposed partition flow is shown in Figure 4, which includes the steps of architecture initialization, partitioning and partition optimization.

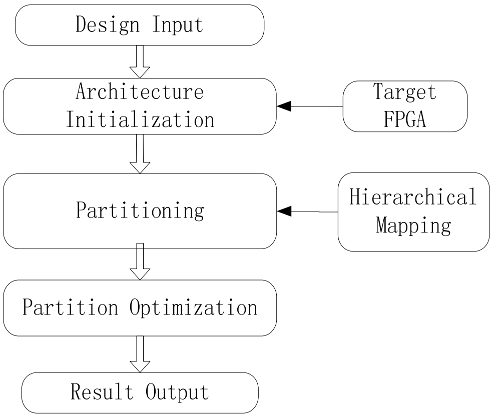


Figure 4 The hierarchicalpartitioning flow for cluster based Multi-FPGAs

A. Architecture Initialization

Before the logic partitioning and mapping, 3 architecture parameters need to be initialized, which are:

1) *Num_FPGAs*:the number of FPGAs needed to map the input design;

2)*Num_Clusters*:the number of clusters of this design;

3) *Size_Clusters:*the size of each cluster (the number of FPGAs in the cluster).

We can get the number of the mapping FPGAs through the comparison of the characteristic parameters between the input design and the target FPGA. We assume the input design is described with hardware described languages (VHDL/Verilog) in this paper. The RTL level description can be obtained through EDA tools to get the characteristic parameters of the design, such as the Configurable Logic Blocks (CLBs), the input/output pins (I/Os) and the Flip-Flops. For a given input design, the required number of target FPGAs is different when the selected mapping FPGA is not in the same size. To simplify the complexity, we assume the target FPGAs are the same size in this work.

To ensure the effective placement and routing, we constrain the capacity of the target FPGA that can be mapped to 75%. If the capacity of the target FPGA is R, the resource that can be mapped for the input design is constraint to 3R/4. We adopt the maximum value (upward rounding) of the comparisons of the characteristic parameters between input design and the constraint target FPGA as the number of target FPGAs needed for the input system. Please refer to the pseudo-code (shown in the algorithm 1) for the calculation details.

The size of clusters is a trade-off between the communication performance and interconnection cost of multi-FPGA systems. If we partition the entire system into small clusters, which means fewerFPGAs in a cluster, the communication performance can be improved greatly due to more communications going through global high-speed channels. But the hardware cost will be increaseddue to more relay nodes needed. On the contrary, if we place more FPGAs in a cluster to reduce the number of clusters of the system, the relay node might become a performance bottleneck if there are too many communications try to go through the global channel.

The interconnection interfaces supported by the target FPGA is another constraint to decided the size of clusters. The high performance FPGAs are usually integrated with high speed communication modules. Taking the Xilinx FPGAs as an example, the Rocket IO modules integrated in Xilinx FPGAs can achieve up to 3.125 Gb/s for high speed interconnections, but the number of Rocket IOs that supported by different series is different from 8 to 24 pairs. So the size of the clusters cannot exceed the number of high-speed communication interfaces supported by the target FPGA. We set the maximum size of the cluster to be m-1 in this work to implement the complete interconnections within the cluster, where, m is the number of high-speed communication interfaces supported by the target FPGA. The size of clusters can be set to be any integer less than m-1 theoretically, but the trade-off between performance and cost needs to be weighted.

Once the number of target FPGAs to be mapped is fixed and the size of clusters is constraint, we can get the number of clusters needed for the input design. The pseudo-code of the architecture initialization is shown in the algorithm 1.

B. Partitioning

To minimize the global communication overhead, we adopt the hierarchical partition approach based on the functional modules of the input design, which means try to partition the modules with the same logic function to the same cluster or the same target FPGA. The design is usually described with multiple interconnected modules if the input design is based on VHDL or Verilog, and each module is consisted with multiple processes and functional sub-modules. We exploit the hierarchy to set the mapping priority. If the module is a top module, it enjoys a higher mapping priority to choose the placement position firstly. For the modules in the same hierarchy, the mapping priority is allocated through the size of the modules, higher priority for bigger module. If the module to be mapped cannot find a reasonable position due to the size problem, the module is decomposed to smaller ones according to functional structure.

The input design is mapped to the clusters firstly, and then mapped to the target FPGAs in the clusters. We implement the two tier partition based on the same hierarchical mapping (the pseudo-code is shown in Algorithm1), the steps includes:

1) Allocate the mapping priority according the hierarchy and the size of the modules, higher priority means to choose the placement position firstly.

2）The selected module will be mapped to the position which makes the target set to have minimum remaining resources un-mapped.

3) If the module to be mapped cannot find a reasonable position due to the size problem, the module will be decomposed to smaller ones according the functional structure;

4) If there are new modules generated through the decomposition, re-allocate the priority and mapping all the un-mapped modules with the new generated modules.

```
Procedure Architecture_Initialization($V_{design}$, $FPGA_{target}$) begin
Imprt a HDLs description;
Get the number of total I/Os, FFs, LUTs of the input design $V_{design}$ :Total_LUTs, Total_FFs , Total_IOs
Get the number of total I/Os, FFs, LUTs of the target FPGA $FPGA_{target}$ :FPGA_LUTs, FPGA _FFs , FPGA _IOs
//Compute the number of FPGAs needed for the input design
Num_FPGAs = Ceil ((Total_LUTs)/(FPGA_LUTs), (Total_FFs)/(FPGA_FFs) , (Total_IOs)/(FPGA_IOs))

//Fix the Cluster Parameters:
Cluster_pattern = Num_FPGAs % m;
K = Num_FPGAs /4
if (Cluster_pattern==0)
        Num_Clusters = k
        Size_Clusters = {m,m,m,…m}
else if (Cluster_pattern==1)
        Num_Clusters = k+1
        Size_Clusters = {m,m,m,…m-1}
else if (Cluster_pattern==2)
        Num_Clusters = k+1
        Size_Clusters = {m,m,m,…m-1,m-1}
else if (Cluster_pattern==3)
        Num_Clusters = k+1
        Size_Clusters = {m,m,m,…m-1}
Return Num_Clusters, Size_Clusters
End Procedure
```

Algorithm1. The pseudo-code of the architecture initialization

C.Partition Optimization

After the logic mapping, the optimization algorithms can be adopted to further reduce the interconnection cost. In the previous step, we already tried to map the logical function-modules that are closely interconnected into the same target FPGA or FPGA cluster to get the smaller external interconnection overhead. This step is aimed primarily at the designs with stringent resource requirement. The design that is hierarchical mapped in the previous step can be used as a initialized input to traditional partitioning algorithms[38][39][40] such as KL algorithm and FM algorithm to get a further optimized partition result.

```
Algorithm Hierarchical_Set_Covering(M,C)
// M is the sets of the modules to be mapped；
// C is the mapping target sets；
            Re-organize the order of the sets M by the largest Module to
        the minimal one：V   M;
$V_g$ = ∅; $V_d$ = ∅; $V_{new}$ = ∅;
//$V_{new}$is the set of new generated modules；
// $V_g$  is the set of new generated modules of the selected module；
// $V_d$is the set of the modules that has been de-composed;

While (V≠∅)
$Num_{\_nodes}$ = size of V;
i=0;
while (i<$Num_{\_nodes}$) begin
    {
$V_{current}$= $V_i$
        for all($C_k \in C$)
if（LUTs({$V_{current} \leqslant C_k$}) && FFs({$V_{current} \leqslant C_k$})&& IOs({$V_{current} \leqslant C_k$})）
                score($C_k$,$V_{current}$) =  α Connectivity($C_k$,$V_{current}$) +  β;
            else
score($C_k$,$V_{current}$) = 0;
if all (score($C_k$,$V_{current}$) = 0) then begin
{ {$V_{new}$} = Functional_Module_Decomposition($V_{current,}$ Maximum($C_k$))
                $V_g = V_g \cup \{V_{new}\}$; }
else
{ select the pair of { $C_k$,$V_{current}$ } with the highest score;
                $V_d = V_g \cup V_{current}$;
                $C_k = C_k - V_{current}$; }
}
i++
}
end while;
  $V = V \cup V_g - V_d$;
Re-organize the order of the sets V by the largest Module to the minimal one。
end while;
```

Algorithm 2. The Pseudo-code of the hierarchical mapping

IV.A CASE STUDY OF THE PROPOSED PARTITIONING APPROACH

In this section we use an actual case study and experiment to help understand our proposed approach more clearly.

The case study is a design of the speech recognition implemented by our lab, and described with VHDL. The given input is comprised with 6 top-modules, the characteristic parameters for each module after the synthesis with Synopsys is shown in Table I. The Xilinx 4013E-1 FPGA is adopted as target FPGAs, and we assume to map the input design to the same type of FPGAs for this case study.

According to the proposed partition flow, the first step is to initialize the architecture parameters through the characteristic parameters of the input design and the target FPGA constraint. The key parameters of the target FPGA is: 1152 LUTs, 1152 Flip Flops (FFs), 192 I/Os. Considering the feasibility for placement and routing, we reserve 25% available resource. So the mappable capacity of the target FPGA is constraint as: {864 LUTs, 864 FFs, 144 I/O s}. The number of the target FPGAs to be mapped is defined as:

$$\mathrm{Num\_FPGAs}=\mathrm{Max}\left\lceil\frac{\mathrm{Total\_LUTs}}{\mathrm{FPGA\_LUTs}},\frac{\mathrm{Total\_FFs}}{\mathrm{FPGA\_FFs}},\frac{\mathrm{Total\_IOs}}{\mathrm{FPGA\_IOs}}\right\rceil=10$$

TABLE I.
THE CHARACTERISTIC PARAMETERS OF THE TOP MODULES OF THE CASE STUDY

Modules	LUTs	FFs	I/Os	Total Size
Module A	1230	987	100	2317
Module B	54	70	10	134
Module C	2100	1879	220	4199
Module D	3470	2897	330	6697
Module E	954	800	129	1883
Module F	692	751	111	2154
All Modules	8490	7384	1339	

Next we need to fix the size of the clusters. As mentioned before, the cluster size is usually a compromise between system performance and cost. If a cluster contains many FPGAs, the communication pressure is heavy for the relay FPGAs, and the transmission latency will increase, but the cost reduced due to less hardware overhead. On the contrary, the more the number of clusters, the higher performance we can get through the high speed transmission through global channel, but with more cost expense. We constraint the number of clusters as 4 or 3 to get a better trade off for this case study and choose the cluster policy with minimum number of clusters. For example, if Num_FPGAs=12, the possible cluster initialization policies might be {4,4,4} or {3,3,3,3}, the policy of {4,4,4} will be adopted since the number of cluster is only 3, less than the policy of {3,3,3,3}.

So according to the initializationalgorithm described before, the number of clusters is 3 and the size for each cluster is {4, 3, 3} for this case study. The detailed key parameters for each cluster are:

Cluster1, 4 target FPGAs, resources:{ 3456 LUTs, 3456 Flip Flops (FFs), 576 I/Os }；

Cluster2, 3 target FPGAs, resources:{ 2592 LUTs, 2592 Flip Flops (FFs), 432 I/Os }；

Cluster3, 3 target FPGAs, resources:{ 2592 LUTs, 2592 Flip Flops (FFs), 432 I/Os }；

Module D is the largest circuit module in this case study and should be mapped to the clusters firstly. But the size of module D exceeds the amount resource of the target clusters as only 3456 LUTs can be mapped to the largest cluster, cluster 1. So we de-compose the module D to module D1{1470 LUTs, 1024 Flip Flops,130 I/Os} and D2{2000 LUTs, 1873Flip Flops,200 I/Os} according the logical functions.

The priority of the top modules to be mapped is "Module C→ModuleD2→Module D1→Module A→ModuleE → ModuleF → ModuleB" after the decomposition of module D according the proposed approach. The module C enjoys the highest priority and to be the first module to be mapped, so there are 3 choices: Cluster 1, Cluster2 and Cluster 3 for module C. If the module C is mapped to cluster 1, the remaining resource would be {1356 LUTs, 1577 Flip Flops, 356 I/Os} after the mapping. If the module C is mapped to cluster 2 or cluster 3, the remaining resource of cluster 2 and cluster 3 would be {492 LUTs, 713 Flip Flops, 212 I/Os}. ）According to the principle that "the selected module will be mapped to the position which makes the target set to have minimum remaining resources un-mapped", we choose to map the module C to cluster 2, and so the remaining resource after mapping for each clusters are:

Cluster1: { 3456 LUTs, 3456 Flip Flops (FFs), 576 I/Os }；

Cluster2: {492 LUTs, 713Flip Flops (FFs), 212 I/Os }；

Cluster3: { 2592 LUTs, 2592 Flip Flops (FFs), 432 I/Os }；

On the analogy of this, the module D1 and module A are mapped to cluster1. When it is the turn for module E to choose the placement position, the mappable resources of each cluster are：

Cluster1: {756 LUTs, 1445 FFs, 346 I/Os }；

Cluster2: {492 LUTs, 713FFs, 212 I/Os }；

Cluster3: { 592 LUTs,719 FFs, 232 I/Os }；

So the module E need to be decomposed as module E1{554 LUTs, 420Flip Flops,70 I/Os} and E2{400 LUTs, 380Flip Flops,59 I/Os}. Now the modules un-mapped are module E2, module E1, module F and module B, and the priority changed to "Module F→ModuleE1→Module E2→Module B".

Byanalog, we can get the mapping result of all the modules as:

Cluster1: { Module D1, Module A, Module F, Module B }；

Cluster2: { Module C, Module E1}；

Cluster3: { Module D2, Module E2}；

The way to map the design from the cluster to target FPGAs is similar as the mapping flow mentioned above. To simplify, we only take the cluster 1 as the example. After the architecture initialization, we know the size of cluster 1 is 4, and the constraints of the target FPGAs of cluster 1are:

FPGA 1: { 864 LUTs, 864 FFs, 144 I/O s }；

FPGA 2: { 864 LUTs, 864 FFs, 144 I/O s }；

FPGA 3: { 864 LUTs, 864 FFs, 144 I/O s }；

FPGA 4: { 864 LUTs, 864 FFs, 144 I/O s }；

According the proposed algorithm, the priority of the modules to map to cluster 1 is: "Module D1→Module A→Module F→Module B", and the mapping result is:

FPGA 1: { Module B, Module D1_1 }；

FPGA 2: { Module A1, Module A2_1}；

FPGA 3: { Module F, Module A2_3}；

FPGA 4：{Module D1_2, Module A2_2}；

To further reduce the interconnection cost, the MP2 algorithm [37]is adopted in this case study to optimize the partition.

To verify the proposed approach, the partition flow is described with High-Level programming language and integrated into the EDA tools (Synopsys Certify-G) through input interfaces for this case study. Experimental result shows that the input design can be partitioned reasonably with a fast speed, and the processes of synthesis, placement and routing can be implemented correctly. We get an average of 23.8% remaining available resource after the implementation of the case design, which means the possibility to relax the constraint of the reserved mapping resource to get a better mapping policy.

V. Conclusion

To target the problems of performance, cost and energy consumption in large scale communications of high performance computing, a cluster based hierarchical topology and corresponding partitioning approachare proposed in this paper. The proposed hierarchical topology taking full advantages of both traditional metallic lines and emerging interconnections to implement one-hop local direct communication within the cluster and one-hop globally high-speed communication between clusters. The customized interconnection topology can be designed according different applications through the proposed partitioning approach to get a better trade-off between performance and cost. The case study proved that the partitioning approach can implement the fast mapping from the design to real high performance computing system with multi-FPGAs, and accelerate the realization of high performance reconfigurable computing systems.

Although the emerging interconnections are advanced in long distance and high bandwidth communications, the introduced extra overhead and cost cannot be ignored for multi-FPGA systems. It is necessary to analyze the performance and energy consumption quantitatively to achieve anoptimum configuration for these emerging effective interconnections. In addition, how to allocate the limited high speed communicationbandwidth and how to solve the traffic congestions are also the important problems to be explored in future works.

Acknowledgment

This work was supported by the Beijing Municipal Natural Science Foundation (No.4122010, 2012.1 - 2014.12) and Beijing innovation platform of Science and technology.

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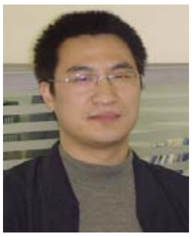

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