# Design and Implementation of Data Synchronization System Based on FPGA

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*Abstract*— **This paper mainly aims at solving the problems of sampled data synchronization in digital substation based on Filed Programable Gate Array (FPGA). Compared with traditional substations, the design achieves data synchronization without connecting an external clock. Synchronization algorithm is based on Newton interpolation algorithm. The system consists of multi-channel data sampling module, synchronization module, Ethernet module etc. The design realizes the concept of modular design with FPGA processor, ensuring that each sub-module gets parallel execution. It is verified that speed is improved to ns level which is difficult to achieve in current systems. Finally, software simulations and hardware tests prove the accuracy and efficiency of the design. Therefore, the design is of great significance for the automation level in smart grid, especially for the enhancement and development.**

*Index Terms*— **data synchronization system, Newton interpolation algorithm, merging unit (MU), Filed Programmable Gate Array (FPGA)**

## I. Introduction

As the integration and digitization of substation, some functions of bay level need to be moved to process level, which will increase the complexity and importance of process level. In process level, electronic transformer output interface is one of the key equipments and merging unit (MU) is the important part of digital interfaces [1].

In substation, it is necessary for secondary equipments to analyze and process the information promptly. Therefore, guaranteeing the information to be collected at the same time is quite important. Asynchronous data processing will not only affect the judgment of protective devices, but also influence the results of measuring equipments. As a result, a shorter and more stable delay is essential for MU to send data after collecting it. The delay jitter cannot exceed 10us. However, time hack function in substation is not very proper or accurate, how to keep the sampling data to be synchronous has been an urgent issue to solve [2].

The traditional synchronization systems still use 51 series micro-controllers as the control core of hardware, which has shown a distinct disadvantage. To achieve the synchronization of sampling data, the current substations need to pay more attention to the high speed Digital Processing Signal (DSP) Chip and Field Programmable Gate Array (FPGA). Compared with the traditional systems, this system is more accurate [3]. Because the grid has the features of wide coverage and huge amount of information, MU remain using traditional controllers at present. There haven't been any synchronization devices with improved processors in the market, so it is desirable to study the technology further.

The rest of this paper is organized as follows. Section II introduces data synchronization algorithm based on Newton interpolation, also gives a comparison between Newton and other interpolation algorithms. Section III shows the design of system in detail. The software design is presented in section IV. Section V focuses on the experimental results and presents analysis about the results. Finally, section VI outlines the conclusion.

## II. Data Synchronization based on Newton Interpolation Algorithm

For current substation, there are mainly two synchronization methods: time synchronization and interpolation algorithm [4] [5]. In the former one, to complete the collection of current or voltage information from different units, a common clock source is needed for each merging unit. The latter one don't have to. And the latter one mainly processes the digital signal based on synchronization algorithm after sampling.

### A. Data Synchronization Algorithm

In synchronization algorithm, multi-channel signals choose one channel signal as the reference signal, and other channels signal are synchronized to the reference one. For example, there are two-channel signals in Fig. 1. We select one channel signal named $S_1$ as the reference, while the other channel signal $S_2$ is to be synchronized. The two signals are sampled at the rate of $T = t$. Denote the *i*'and *(i +1)*' sampled values of $S_2$ as $V_i$ and $V_{i+1}$ *(i = 1, ..., n)*, where the time moment is referred to $T_i$ and $T_{i+1}$. Then denote the *i*' sampled value of $S_1$ as $V_{i1}$, and define the time moment of $V_{i1}$as reference time $T_i$'. The difference between $T_i$ and $T_i$' is $\Delta$t. After interpolating, we can obtain the sampled value $V_i$' of $S_2$ at the moment of $T_i$'. Subsequent data is calculated in accordance with this principle. After interpolation, the data obtained is the value needed after synchronization [6].

### B. Interpolation Simulation and Error Analysis

As [7] mentioned, there are various data synchronization methods. Linear interpolation, an algorithm easy to be realized, has been widely researched and used in


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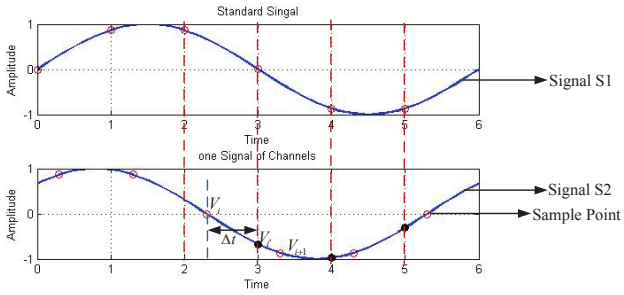


Figure 1. Algorithm of Data Synchronization.

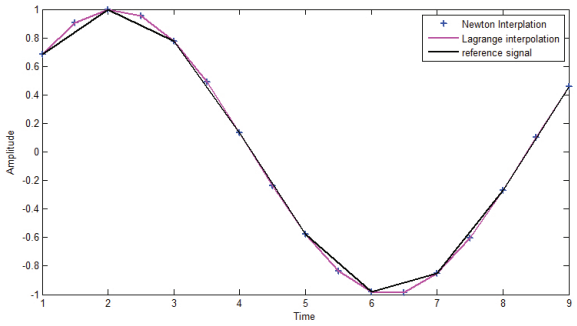


Figure 2. Simulation of Lagrange and Newton Interpolation Algorithms.

systems, as referred in [8] [9]. Lagrange and Newton interpolation algorithm are the two widely used methods. In this paper we give an simulation and analysis of the two methods through Matlab software. We select an reference signal and give the simulation waveform based on Lagrange and Newton interpolation algorithm respectively. The simulation waveform is shown in Fig. 2.

It can be seen that the simulation results of the two method are similar and have same error. However, Lagrange method lacks inherited property which means it can't use the calculated results to estimate the subsequent results. If a new node is introduced into the system, it is necessary to re-calculate the result, which leads to heavy computation. As a result, synchronization algorithm is based on Newton interpolation algorithm in this paper. As shown in Fig. 3, inputs are abscissa and ordinate vectors of *n+1* known points on a function. *c* is the coefficient vector of Newton interpolation polynomial used to draw *m-1* order Newton interpolation polynomial *Z*(*Tt*).

Fig. 4 shows the simulation waveform of sync signal using Matlab software. In Fig. 4, the $1^{st}$ channel signal is the reference signal and the $2^{nd}$ channel signal is to be synchronized. The solid line of third channel is the signal after synchronization of $2^{nd}$ channel. It can be seen that the phase of $2^{nd}$ channel has been synchronized to the $1^{st}$ channel completely without changing the amplitude of original signal. As shown in Fig. 4, the higher the sample frequency is, the smaller the error will be after synchronization. In this paper, we compare data calculated according to the actual polynomial and polynomials derived by interpolating 7 points, 13 points or 25 points. Take the same time $T_t$ = 5 and calculate the values through

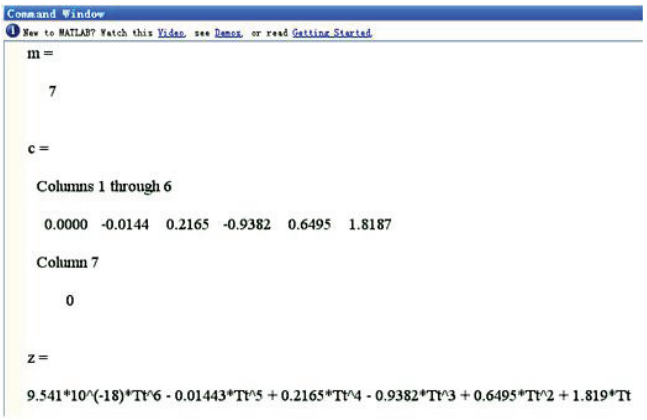


Figure 3. Output of Newton Interpolation Algorithms.

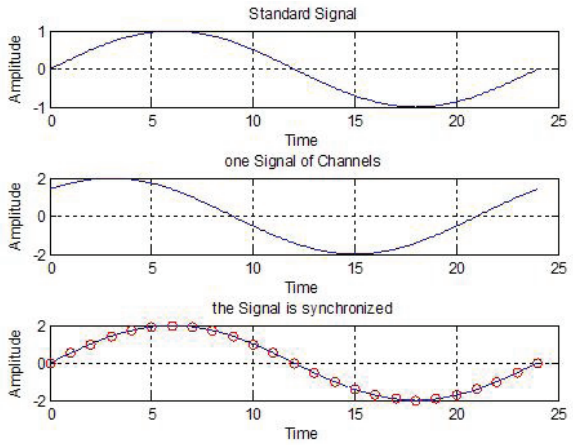


Figure 4. Matlab Simulation of Newton Interpolation Algorithm.

the interpolating and standard polynomials respectively. By interpolating different points, the comparison result of error is displayed in Tab. I. The error calculated in Tab. I is based on Newton interpolation algorithm.

It can be seen from Tab. I that the larger the number of interpolation points is, the higher the accuracy of result and the smaller the error will be. However, as the number increases, the data window will get longer, the amount of computation will increases as index folding. In practical applications, the larger the number is, the worse the stability of data will be. In the design, we interpolated 24 values in each period, which not only meets the accuracy of system, but also maintains a moderate amount of computation and improves the stability of data.

## III. Design of Data Synchronization System

### A. System Architecture

Considering the functions to be accomplished and the definition of merging unit, data synchronization system is divided into several modules. The system includes multi-channel data receiving and processing module, data synchronization module, ethernet module and external auxiliary modules [10]. The overall architecture is displayed in Fig. 5.

TABLE I.
ERROR COMPARISON OF ALGORITHM WITH DIFFERENT SAMPLING POINTS

| Order $n$ | Interpolation polynomial $Z(Tt)$ | $Tt$ =5, Measured value /Standard value | Error $R$ |
|---|---|---|---|
| 7 | $Z$=-0.0144×$Tt^5$+0.2165× $Tt^4$-0.9382× $Tt^3$+0.6495×$Tt^2$+1.8187×$Tt$ | -1.6315 / -1.7321 | 5.807% |
| 13 | $Z$=3.46×10-11×$Tt^{11}$-1.232×10-21×$Tt^{12}$-2.284×10-9×$Tt^{10}$++0.04773×$Tt^3$-8.94×10-5×$Tt^2$+1.047×$Tt$ | 0.9995 / 1.0000 | 0.0500% |
| 25 | $Z$=1.305×10-31×$Tt^{23}$-4.565×10-34×$Tt^{24}$-1.757×10-29×$Tt^{22}$+-0.00598×$Tt^{35}$-5.33×10-11×$Tt^2$+0.5236×$Tt$ | 1.9319 / 1.9319 | 0.0000% |

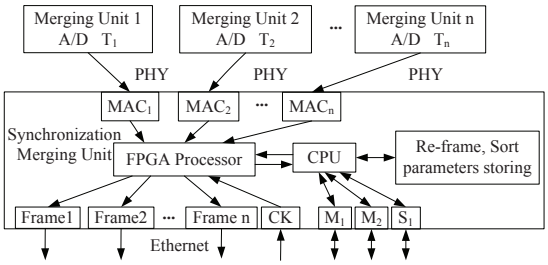


Figure 5. System Architecture.

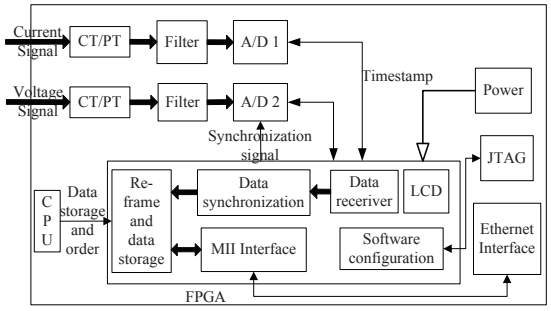


Figure 6. Block Diagram of Hardware Platform.

In Fig. 5, merging units 1 to $n$ should perform A/D transmission after bucking the received analog signal. Digital signals are sampled at different rates according to the needs of bay level, and forwarded to subsequent synchronization unit by Ethernet module. FPGA implements sampling and completes synchronization of multi MUs after simultaneous calculation. In the end, frames and sorting parameters will be restructured, then encapsulated into a new data packet and transmitted to the secondary equipments of bay level by ethernet module.

### B. Hardware Design of System

System hardware platform, consisting of FPGA core part and peripheral accessories, is a combination of hardware and software. The system is mainly made up of FPGA control module, SRAM and Flash module, ethernet module, MII control module, JTAG module, UART transceiver module, power supply module and other necessary peripheral modules. Fig. 6 is a block diagram of hardware platform.

*1) Interface between FPGA and SRAM:* SRAM in the system uses CY7C1041BV33 chip packaged in 44-pin TSOP. The chip has 16 data bits and 18 address bits. The

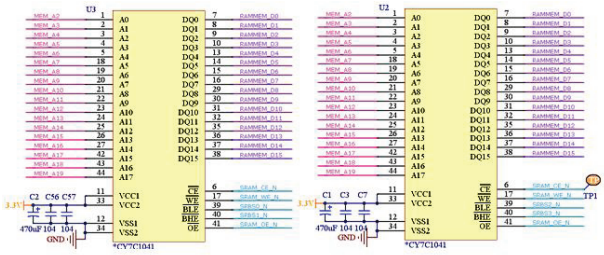

Figure 7. Interface between SRAM and FPGA.

system realizes 32 data bits by paralleling two chips. Just connect the SAM_CE_N signal of FPGA to the select signal $\overline{CE}$ of two SRAM chips. When $\overline{BLE}$ actives low, data from $I/O_0$ to $I/O_7$ will be written to the specified position of address frames. When $\overline{BHE}$ actives low, data from $I/O_8$ to $I/O_{15}$ will be written to the specified position of address frames. It is necessary to connect decoupling capacitors near power supply module of the chips. In the system each power supply module is connected to two $0.1uF$ SMD capacitors and a $470uF$ electrolytic capacitor. The schematic diagram of FPGA and SRAM connection is shown in Fig.7.

*2) Interface between FPGA and Flash:* Fig. 8 is a schematic diagram of single-chip Flash,' including 18 address lines A [17:0] and 16-bit data lines DQ [15:0]. In read and write mode, we can select either 8-bit or 16-bit mode by setting $\overline{BYTE}$ bit in accordance with the need. In the system, 16-bit mode is selected and bit $A_1$ is set as the LSB in address bits. A dislocation connection in address lines is needed between Flash and FPGA, meaning that $A_{22}$ of FPGA is connected to $A_{21}$ of Flash, and $A_1$ of FPGA is connected to $A_0$ of Flash. $\overline{CE}$ is the select signal of chip and $\overline{OE}$ is the output enable signal. Two signals should active low. The data bits and address bits of NOR Flash and SRAM are connected to BANK3 and BANK2 of FPGA respectively. The other control pins are controlled by FPGA.

*3) Ethernet physical layer circuit:* TCP/IP protocol is necessary for the transmission of ethernet data. According to the program serial operation and complexity of statutes in different layer, it is difficult to ensure the delay of each module and the accuracy of data. The system completes ethernet communication between MAC layers based on FPGA, without considering the upper layer protocols. Transmission distance and interfaces are as same as in TCP/IP protocol so that communication of the system

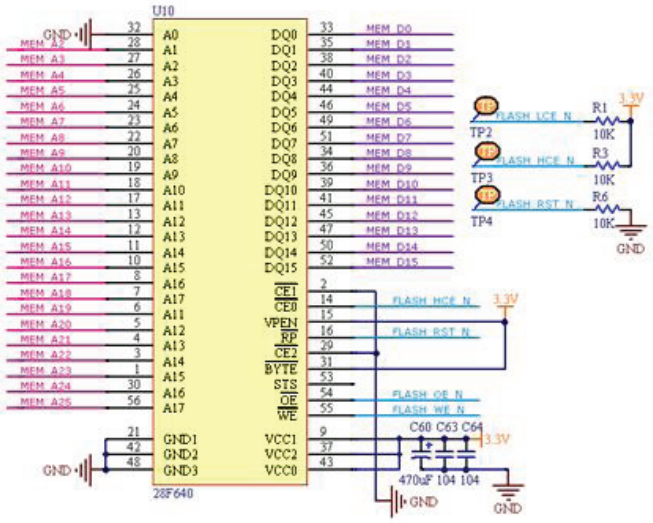


Figure 8. Interface between Flash and FPGA.

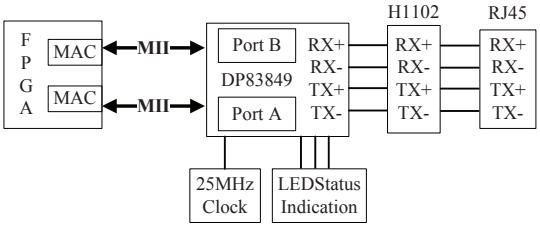


Figure 9. Interface of Ethernet.

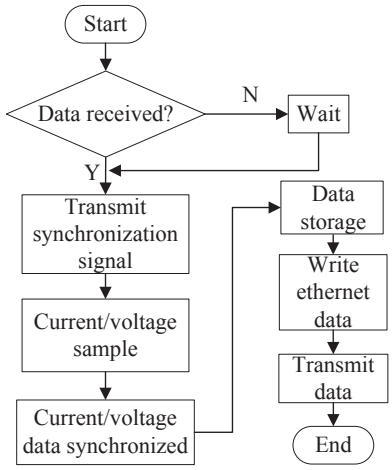


Figure 10. Software Design of System.

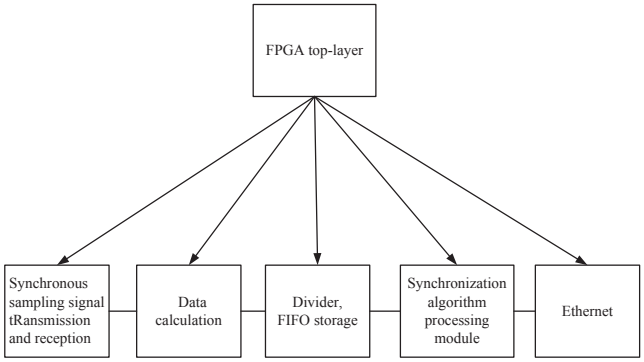


Figure 11. Block Diagram of System.

does not need the upper layer protocols. As a result, packet loss or delay of the communication is very low, but the data rate and accuracy is quite high.

In this system, the interface device used to connect system with Internet is DP83849IF PHY chip produced by U.S. Semiconductor Company. The MII interface circuit is shown in Fig. 9. The dual ethernet physical layer transceiver has two completely independent 10/100Mbps ports with rich routing functions. To achieve the transmission of data, two DP83849IF PHYs are relevance together through external wiring and the chip's internal data route functions. The clock signal of DP83849IF is provided by an external 25MHz crystal oscillator. The internal LEDs are controlled to display work status. The main task of FPGA is to provide the required voltage and configure I/O of DP83849IF.

## IV. Software Design of System

### A. Software Architecture of System

The software architecture of synchronization system includes four parts: the sampling data receiver module, data synchronization module, ethernet module and other peripheral control module. The MU has a high demand for the real-time and accuracy of data transmission. Therefore, software should has a high performance. Code is simple, but execution efficiency is respectively high. The logic diagram is explained in Fig. 10.

As shown in Fig. 10, detecting whether last data transmission is completed firstly. If completed, send synchronous sampling signal to each MU by FPGA, otherwise continue to wait. After receiving unified sampling signal, MU completes analog-to-digital conversion and acquires sampled data of current or voltage by FPGA, then timestamps the data at the same time. The data is stored in First In First Out (FIFO) sequentially after reframed and synchronized.

System adopts a hierarchy architecture [11] [12]. Underlying files implement complex logic algorithm through text input. The top files use a more intuitive and simple graphical input design style. The system consists of a top module and 5 sub-modules as displayed in Fig. 11. Top-level module contains organization, coordination and management of all sub-modules, also includes I/O signals description. Bottom module mainly implements functions of divider, data operation, synchronization algorithm, sampling control merging unit and ethernet transmission.

### B. Design of Synchronization Algorithm

Hardware realization of synchronization algorithm introduces the concept of difference quotient. To get inter-

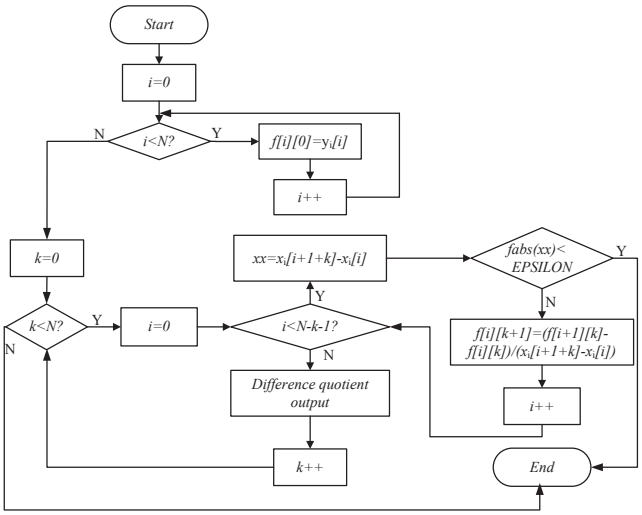


Figure 12. Procedure of Searching Difference Quotient.

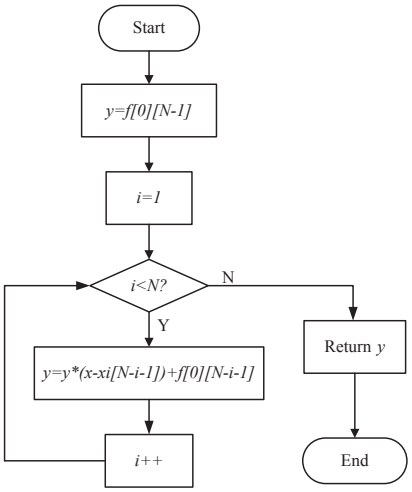


Figure 13. Calculation of Coordinate Values after Interpolation.

polation polynomial, it is important to find the difference quotients of order N-1 firstly. Fig. 12 is a flow chart of seeking difference quotient table. Difference quotient $f(x_i, x_{i+1},..., x_{i+k})$ is generated by known point $(x_i, y_i)$ and stored in the variable *f[i][k]*. Calculate the difference quotient in turn when *k* is less than the number of basis points *N*. *xx* is the difference of adjacent abscissa. It is detected by accuracy comparison function *fabs()* whether difference meets the minimum accuracy requirements of the chip. If less than the accuracy to be provided, program is exited with none difference. Otherwise, continue to seek difference and divide to calculate difference quotient. Convolution is also important in interpolation algorithm. Fig. 13 illustrates how to obtain the point after interpolation. During the process, difference quotient table is utilized. After calculation, value of *pn(xi)* is returned.

### C. Design of Ethernet Transmission Module

The data frame sent to secondary equipments contains necessary information of sampled current and voltage,

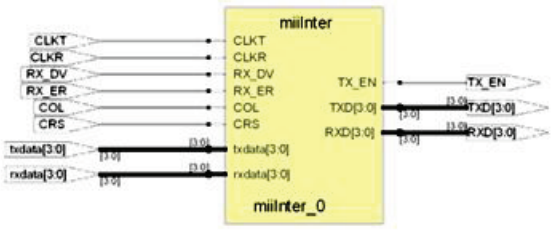


Figure 14. RTL Viewer of MII Interface.

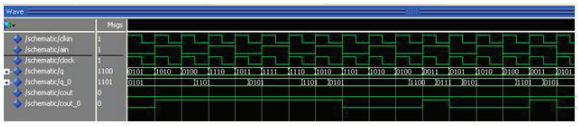

Figure 15. Simulation Waveform of Synchronization Algorithm.

also contains some basic information and timestamps to reflect states [13]. Standard stipulates that transmission of data frame in data link layer should be based on ISO/IEC 802.3 protocol. Destination MAC address, source MAC address, length, type, and data are generated in the upper layer protocol as OSI model defined. Whereas transmission in the present system just based on MAC layer, so several fields of specific data are given by the program.

The communication interface between MAC layer and physical layer is MII interface. MII interface comprises a data interface and management interface. MII management module communicates with physical layer through a clock signal and a data signal. Fig. 14 is the RTL figure after consolidating the code of MII module.

## V. Experimental Results

### A. Simulation of Synchronization Module

According to the process of top-level, each module works well verified by the simulation. In Fig. 15, the final simulation explains the effective operation result of synchronization. Since the MII interface is 4-bit, so the output data is divided into low 4-bit and high 4-bit. In Fig. 15, variable *q* is the high 4-bit data and variable $q_0$ is the low 4-bit data, while clock is the only input signal. In conclusion, the system has an high integration degree.

### B. Simulation of Ethernet Transmission Module

At first, current and voltage signal is repackaged into frame format based on IEC 61850-9 standard by synchronization unit. Then the frame is sent to the secondary protection or measuring equipments by ethernet respectively. During the transmission, it is necessary to check the correctness of contents.

Transmit data: Fig. 16 is the simulation waveform of transmission timing. Clkt is the clock signal, as well as the reference clock for tx_en, txd and tx_er. When tx_en is effective, data on txd is received by PHY, otherwise the data has no effect for PHY.

Figure 16. Simulation Waveform of Data Transmission.

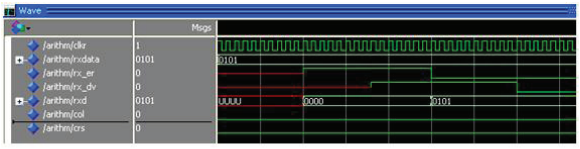

Figure 17. Simulation Waveform of Data Reception.

Receive data: Fig. 17 is the simulation waveform of receiving timing. Rx_tv is synchronized to clkr and driven by PHY. In order to receive the rxd data successfully during clkr clock cycle, the effective time of rx_dv must be able to cover the entire frame process. Rx_er is synchronized to clkr. During data transmission, if the rx_er hold high more than one clock cycle and rx_en is effective, data transferred will be invalid.

### C. Test of Entire System

To verify the validation of synchronization data, we select consecutive 24-point data to analyze. Input is coordinates of data to be synchronized and interpolation points, while output is coordinates of data after interpolation. The output values are shown in Tab. II. To reduce the complexity of data processing in FPGA, decimal is moved two bits to left. In order to facilitate observation, the data has been converted into decimal and the negative data turns into its complemental code. For example, the first data 0x2C shall be 0.44 in fact. Select a positive data as the first point from which are changed from negative to positive. The selected data is selected as the longitudinal axis and their time acts as the horizontal axis.

According to the synchronization coordinates, we can get synchronization waveform by Matlab as shown in Fig. 18.

Waveform 1 is the reference waveform. Waveform 2 is one of the multi-signals to be synchronized, and waveform 3 is the synchronization waveform obtained after synchronization. Red circle is the standard value for the point, while the solid blue line is the coordinate values derived by the synchronization algorithm. As shown in Fig. 18, synchronized data shows a good coherence, without hopping. In conclusion, MU completes data synchronization function within the selected range.

TABLE II.
SYNCHRONOUS COORDINATES OF SINGLE-CYCLE

| | 0 | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| 0 | 0.00 | 0.44 | 0.89 | 1.29 | 1.60 | 1.79 |
| 1 | 1.85 | 1.79 | 1.60 | 1.30 | 0.92 | 0.47 |
| 2 | 0.007 | -0.46 | -0.90 | -1.27 | -1.56 | -1.74 |
| 3 | -1.79 | -1.71 | -1.50 | -1.16 | -0.73 | -0.24 |

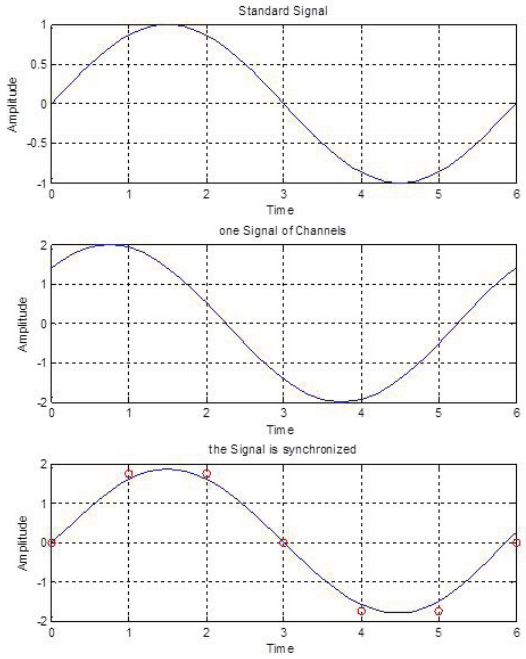


Figure 18. Simulation Waveform of Synchronization Algorithm.

From the test, we can learn that MU in this design completes interface function with electronic transformer. In addition, data processing and transmission functions also meet the requirement.

## VI. CONCLUSION

The design achieves data synchronization based on Newton interpolation algorithm without external clock source. Through the simulation of algorithm and analysis of experimental data, the design achieves better quality and effects compared to traditional synchronization system.

Program is carried out in VHDL language by taking full advantages of FPGA compared with CPU, such as modular programming, rich I/O resource, and high-speed data processing capabilities. The design includes a variety design of computing devices, the FIFO circuits, the synchronization module and the ethernet module.

This design is easy to be implemented and flexible to be modified, and achieves a preliminary design with high degree of independence in synchronous merging units. Compared with the traditional MU, the system improves the accuracy and speed. The simulation verifies the feasibility and effectiveness of the system. In conclusion, the design is of high practical value for equipments in substation system, especially for equipments which have high requirements for real-time and synchronization.

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