A Sub-1V High-PSRR Piecewise-Linear Bandgap Reference

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***Abstract*—A piecewise-linear bandagp reference (BGR) with high power supply rejection ratio (PSRR) and low temperature coefficient is designed for analogue and mixed signal systems in this paper. By adopting LDO regulator, the designed high PSRR piecewise-linear BGR achieves well performances and has a simple architecture. Simulation results show that the PSRR of the designed piecewise-linear BGR with LDO regulator at 10Hz, 1kHz and 100kHz achieves, respectively, -110.42dB, -109.18dB and -64.51dB. Compared to the designed BGR without LDO regulator, the PSRR of the designed high PSRR piecewise-linear BGR with LDO regulator has the improvements of about 35dB, 36.9dB and 29.28dB at 10Hz, 1kHz and 100kHz respectively. The designed piecewise-linear BGR with LDO regulator generates an output voltage of 0.68V with 1.65ppm/ºC temperature coefficient in the range from -50 ºC to 125 ºC. The deviation of the output voltage is within 98.23μV when the power supply voltage V_{DD} changes from 1.2V to 7V.**

***Index Terms*—bandgap reference (BGR), piecewise-linear, LDO regulator, power supply rejection ratio (PSRR)**

I. INTRODUCTION

Bandgap reference (BGR) is a very important block for many analogue and mixed signal electronic devices such as data converters, DC-DC converters, DRAMs, linear regulators and so on. The BGR should be independent of fluctuations of power supply voltage and temperature, and also be implemented without modification of fabrication process. In modern CMOS technology, the output voltage of BGR is usually a weighted sum of the forward-bias emitter-base voltage of diode-connected parasitic vertical PNP transistor and the thermal voltage [1]. Conventional BGR has a large temperature coefficient over the whole temperature range and cannot meet the requirements of high precision circuits. To improve the temperature performance of BGR, many temperature compensation techniques have been reported, such as correlated double sampling technique [2], curvature correction [3-6] and so on. Recently, demands for low-voltage BGR circuits have increased enormously because they are widely used in portable electronic applications. Simultaneously, the most significant noise injected to the output of BGR circuit is the supply noise regarding to the other noise. On the other hand, a high power supply rejection ratio (PSRR) BGR is desired to achieve high performance analogue and mixed signal systems, particularly in wireless communications. Therefore, a BGR structure, which has high PSRR over broad frequency range, should be chosen to reject the supply noise coupled from the high-speed digital circuit on the chip.

In the recent past, many approaches have be developed to improve the PSRR of BGR, such as supply independent current source technique [7], pre-regulator technique [8-11], subtractor technique [12], pseudo floating voltage source technique [13], cascode current-mode technique [14], self-cascode current mirror technique [15], low dropout (LDO) regulator technique [16], voltage follower technique with PMOS as input transistor [17] and so on. In general, these reported BGR with PSRR enhancement have achieved well performance. However, to further improve the performance of BGR, the high PSRR BGR structure must still be analyzed and discussed.

In this paper, a high PSRR CMOS BGR with less than 1V output voltage is designed and analyzed. Employing an improved piecewise-linear temperature compensation technique and a LDO regulator, the designed BGR achieves a high PSRR performance over a wide frequency range and a well temperature characteristic over a wide temperature range. The analysis and design of piecewise-linear BGR without LDO regulator will be given in Section II. Section III will discuss the high PSRR piecewise-linear BGR with LDO regulator. Simulation results are described in Section IV. Finally, conclusions are given in Section V.

II. ANALYSIS AND DESIGN OF PIECEWISE-LINEAR BGR

The designed BGR is shown in Fig.1, which consists of a start-up circuit and a core circuit of BGR. There are two possible equilibrium points in the core circuit of BGR, so a start-up circuit is necessary. M_{s1}~M_{s5} form the start-up circuits, as shown in Fig.1 (b). The core circuit of piecewise-linear BGR will provide a sub-1V bandgap

doi:10.4304/jcp.9.5.1274-1281

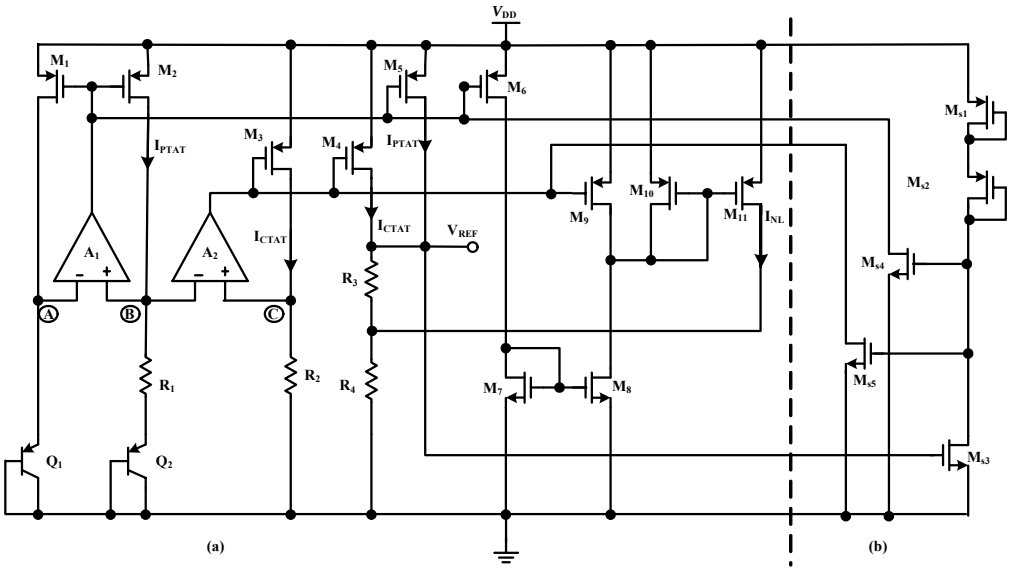

Figure 1. Designed BGR (a) core circuit of BGR, (b) start-up circuit

voltage V_{REF} and has a good temperature characteristic. At the same time, all MOS transistors adopt the long channel transistor so that the channel-length modulation effect is negligibly small in this paper.

For convenience, it is assumed that W_j, L_j and I_j are, respectively, channel-width, channel-length and drain current of transistor M_j in this paper, here j=1, 2, 3…. The core circuit of piecewise-linear BGR consists of transistors M_1~M_{11}, bipolar transistors Q_1 and Q_2, resistors R_1~R_4, and amplifiers A_1 and A_2. Amplifiers A_1 and A_2 are entirely the same, and their dc gain A_d has that A_d>>1. Amplifier A_1 forces the voltages V_A and V_B be equal, and amplifier A_2 forces the voltages V_B and V_C be equal, i.e. V_A=V_B=V_C=V_{EB1}. Here, V_A, V_B, V_C and V_{EB1} are, respectively, the voltages of node A, node B, node C and emitter-base voltage of Q_1. Transistors M_1, M_2 and M_5 are entirely the same, and Q_2 has an emitter area that is m times that of Q_1. So, the drain currents of transistors M_2 and M_5 can be derived as

$$I_2 = I_5 = \frac{kT}{q}\frac{1}{R_1}\ln m \tag{1}$$

where, k is Boltzmann's constant, q is electronic charge, and T is absolute temperature. It is concluded that currents I_2 and I_5 are proportional to the absolute temperature T. Amplifier A_2 force voltages V_B and V_C be equal, and transistors M_3 and M_4 are entirely the same. Therefore, the drain currents of M_3 and M_4, i.e. I_3 and I_4, can be derived as

$$I_3 = I_4 = \frac{V_{EB1}}{R_2} \tag{2}$$

V_{EB1} has a negative temperature coefficient, so it is concluded that currents I_3 and I_4 have a negative temperature coefficient. Transistors M_2 and M_6 have the same aspect ratio, and M_3 and M_9 have also the same aspect ratio. Therefore, it is concluded that I_6=I_2 and I_3=I_9.

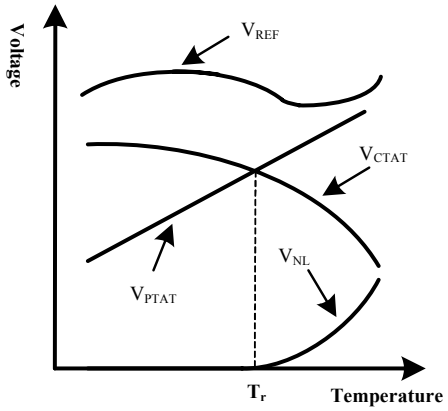

Figure 2. Operation of designed BGR

Transistorss M_7 and M_8 form the current-mirror pair, and transistor M_8 has the aspect ratio that is α times that of transistor M_7. By optimizing the value of parameter α, it can be achieved that I_9=I_8=αI_2 under the condition of room temperature Tr. Therefore, the following expression can be derived as

$$\begin{cases} I_8 = \alpha\dfrac{kT}{q}\dfrac{1}{R_1}\ln m < I_9 = \dfrac{V_{EB1}}{R_2}, when \quad T < T_r \\ I_8 = \alpha\dfrac{kT}{q}\dfrac{1}{R_1}\ln m = I_9 = \dfrac{V_{EB1}}{R_2}, when \quad T = T_r \\ I_8 = \alpha\dfrac{kT}{q}\dfrac{1}{R_1}\ln m > I_9 = \dfrac{V_{EB1}}{R_2}, when \quad T > T_r \end{cases} \tag{3}$$

M_{10} and M_{11} form current-mirror pair and have entirely the same aspect ratio. Therefore, the drain current I_{NL} of transistor M_{11} can be derived as

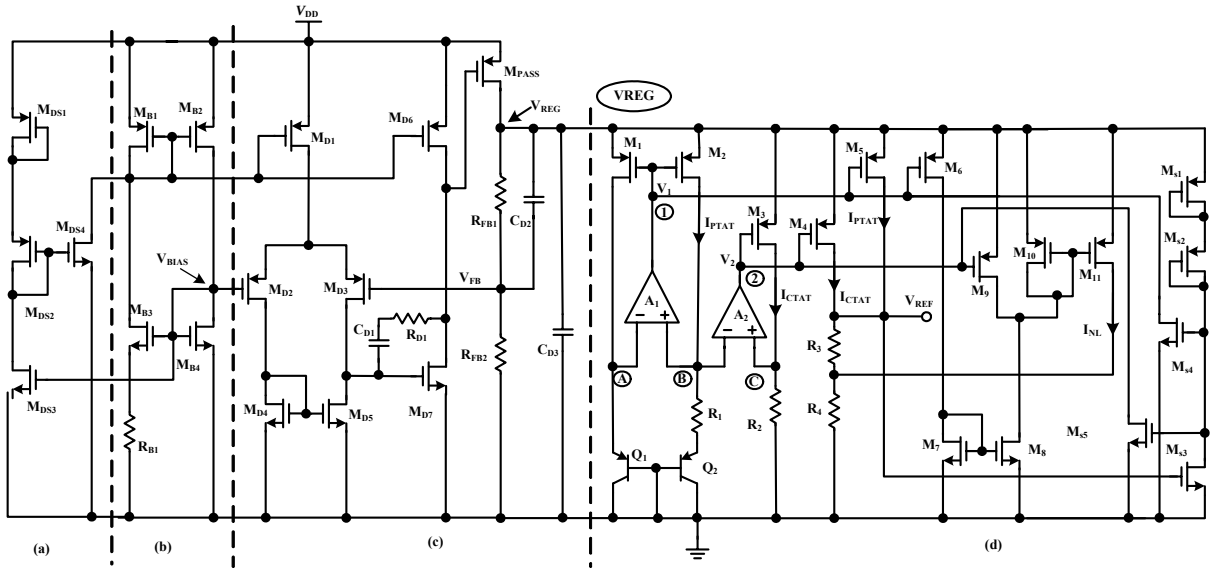

Figure 3. Designed high PSRR BGR with LDO regulator (a) start-up circuit, (b) supply-independent bias circuit, (c) LDO regulator, (d) core circuit of piecewise-linear BGR

$$\begin{cases} I_{NL} = 0, & when \quad T \le T_r \\ I_{NL} = \alpha \dfrac{kT}{q}\dfrac{1}{R_1}\ln m - \dfrac{V_{EB1}}{R_3}, & when \quad T > T_r \end{cases} \tag{4}$$

So, the output voltage V_{REF} of piecewise-linear BGR can be derived as

$$\begin{aligned} V_{REF} &= (R_3 + R_4)\left(\frac{kT}{q}\frac{1}{R_1}\ln m + \frac{V_{EB1}}{R_2}\right) + R_4 I_{NL} \\ &= V_{PTAT} + V_{CTAT} + V_{NL} \end{aligned} \tag{5}$$

$$V_{PTAT} = (R_3 + R_4)\frac{kT}{q}\frac{1}{R_1}\ln m \tag{6}$$

$$V_{CTAT} = (R_3 + R_4)\frac{V_{EB1}}{R_2} \tag{7}$$

$$V_{NL} = R_4 I_{NL} \tag{8}$$

According to (1) ~ (8), it is concluded that V_{PTAT}, V_{CTAT} and V_{NL} are, respectively, the voltages with positive-temperature coefficient, negative-temperature coefficient and piecewise temperature coefficient, and their relations are shown in Fig.2. Equation (5) shows that the piecewise-linear BGR can achieve a low temperature coefficient bandgap reference voltage V_{REF} by optimizing resistors R_1~R_4 and parameter α in theory. However, the operating supply voltage of piecewise-linear BGR, which is shown in Fig.1, is the power supply voltage V_{DD}, and it cannot achieve high PSRR over a wide frequency range. Therefore, the piecewise-linear BGR cannot be effectively applied to analogue and mixed signal systems that have the requirement of high PSRR. Therefore, to further improve PSRR of BGR, a high PSRR piecewise-linear BGR is designed by adopting LDO regulator in this paper, and will be analyzed in Section III.

III. Analysis and Design of High PSRR Piecewise-Linear BGR

Fig.3 shows the designed high PSRR piecewise-linear BGR, and all MOS transistors adopt the long channel transistor so that the channel-length modulation effect is negligibly small. The designed high PSRR piecewise-linear BGR consist of a start-up circuit, a supply-independent bias circuit, a LDO regulator and a core circuit of piecewise-linear BGR. The core circuit of piecewise-linear BGR is entirely the same as that designed in Section II, but whose operating supply voltage is the output voltage V_{REG} of LDO regulator instead of power supply voltage V_{DD}. Therefore, the designed high PSRR piecewise-linear BGR with LDO regulator can achieve an output voltage V_{REF} with low temperature coefficient and high PSRR. The supply-independent bias circuit produces supply-independent bias voltages, and will be discussed in Section III.A. Because there are two possible equilibrium points in the supply-independent bias circuit, a start-up circuit is necessary. M_{DS1}~M_{DS4} form the start-up circuits, as shown in Fig.3 (a). The function of LDO regulator is to produce an internally regulated voltage V_{REG} that is the operating supply voltage of core circuit of piecewise-linear BGR instead of power supply voltage V_{DD}. The analysis and design of LDO regulator will be given in Section III.B.

A. Supply-Independent Bias Circuit

As shown in Fig.3 (b), the supply-independent bias circuit consists of M_{B1}~M_{B4} and R_{B1} [18]. MOS transistors M_{B1}~M_{B4} operate in the saturation region, and M_{B1} and M_{B2} are entirely the same. The channel lengths of M_{B3} and M_{B4} are the same, but M_{B3} has a channel width that is N times that of M_{B4}. Therefore, the drain currents I_{B3} and I_{B4} can be expressed as

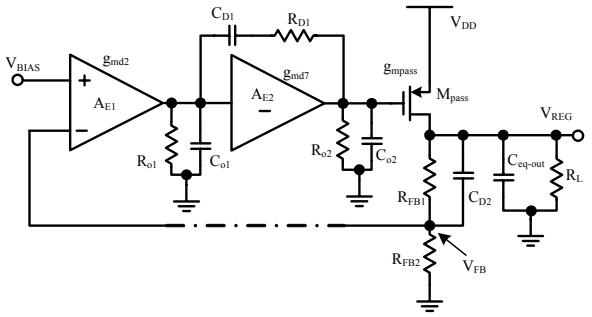

Figure 4. Topologic architecture of LDO regulator

$$I_{B3} = I_{B4} = \frac{2}{\mu_n C_{ox}(W_{B4}/L_{B4})} \frac{1}{R_{B1}^2}\left(1-\frac{1}{\sqrt{N}}\right)^2 \quad (9)$$

where, μ_n is the mobility of an electron, C_{ox} is the gate oxide capacitance per unit area. Equation (9) indicates that the bias-current I_{B4} is independent of the power supply voltage V_{DD}. Therefore, the gate-voltage V_{BIAS} of MOS transistor M_{B4} can be derived as

$$V_{BIAS} = \frac{2}{\mu_n C_{ox}(W_{B4}/L_{B4})} \frac{1}{R_{B1}}\left(1-\frac{1}{\sqrt{N}}\right)+V_{THN} \quad (10)$$

where, V_{THN} is the threshold voltage of NMOS transistor. Equation (10) indicates that the bias voltage V_{BIAS} is also independent of the power supply voltage V_{DD}.

B. Analysis and Design of LDO Regulator

The designed LDO regulator is shown in Fig.3 (c), which consists of error amplifier, a PMOS power transistor M_{pass}, and a feedback resistive network. The feedback resistive network consists of capacitor C_{D2}, and resistors R_{FB1} and R_{FB2}. The error amplifier consists of MOS transistors M_{D1}~M_{D7}, resistor R_{D1} and capacitance C_{D1}. The error amplifier compares the reference voltage V_{BIAS}, which is provided by the supply-independent bias circuit, with the feedback voltage V_{FB} that is provided by the feedback resistors R_{FB1} and R_{FB2}, and generates an error voltage signal which is fed into the gate of power transistor M_{pass} to change its over-drive. The over-drive adjusts the drain current of M_{pass} and forces the output voltage V_{REG} of LDO regulator to be corrected to the proper level. The error amplifier and power transistor M_{pass} form a negative feedback system, which is equivalent to a three-stage amplifier negative feedback system. Therefore, the open-loop stable of LDO regulator is critical issue.

To analyze the stability of LDO regulator, the open-loop transfer function of LDO regulator should be analyzed and discussed. For convenience, the topologic architecture of LDO regulator is shown in Fig.4. The first-stage error amplifier A_{E1} consists of MOS transistors M_{D1}~M_{D5}, whose equivalent input transconductance is written as g_{md2}. The second-stage amplifier A_{E2} consists of MOS transistors M_{D6} and M_{D7}, whose equivalent input transconductance is written as g_{md7}. R_{o1} and R_{o2} are the output resistance of amplifier A_{E1} and A_{E2} respectively, and C_{o1} and C_{o2} are the parasitic capacitances at the output of A_{E1} and at the gate of M_{pass} respectively. g_{mpass} is the equivalent transconductance of M_{pass}, and R_L is the equivalent load resistance. In Fig.4, $C_{eq\text{-}out}=C_{D3}+C_L$, here C_L is the equivalent capacitance of internal power line.

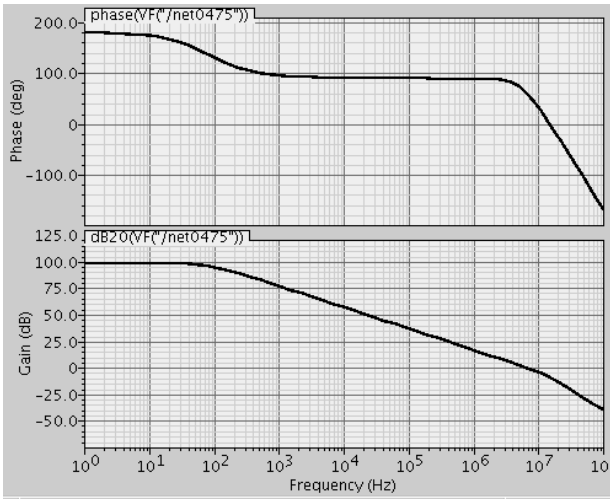

Figure 5. Open-loop frequency response of LDO regulator

To simplify the transfer function without losing accuracy with the goal of providing a clearer insight into the designed LDO regulator structure, it is assumed that capacitors C_{D1}, C_{D2} and $C_{eq\text{-}out}$ are much greater than the parasitic capacitance C_{o1} and C_{o2}, and the gains of each stage is much greater than one, i.e. $g_{md2}R_{o1}$, $g_{md7}R_{o2}$ and $g_{mpass}R_L>>1$. On the other hand, the feedback resistance R_{FB2} is much greater than the load resistance R_L, and R_{o1} and R_{o2} are greater than R_{D1}. Therefore, the loop transfer function of the designed LDO regulator can be approximated to

$$T_{loop}(s) = \frac{T_0(1+s/z_1)(1+s/z_f)}{(1+\frac{s}{p_{-3dB}})(1+\frac{s}{p_1})(1+\frac{s}{p_2}+\frac{s^2}{p_2 p_3})(1+\frac{s}{p_f})} \quad (11)$$

$$T_0 = g_{md2}R_{o1}g_{md7}R_{o2}g_{mpass}R_L\frac{R_{FB2}}{R_{FB2}+R_{FB1}} \quad (12)$$

$$p_{-3dB} = \frac{1}{g_{md7}R_{o1}R_{o2}C_{D1}} \quad (13)$$

$$p_1 = \frac{1}{C_{eq-out}R_L} \quad (14)$$

$$p_2 = \frac{g_{m2}}{C_{o1}+C_{o2}} \quad (15)$$

$$p_3 = \frac{1}{R_{D1}(C_{o1}//C_{o2})} \quad (16)$$

$$p_f = \frac{1}{C_{D2}(R_{FB1} // R_{FB2})} \quad (17)$$

$$z_1 = \frac{1}{C_{D1}(R_{D1} - 1/g_{md7})} \quad (18)$$

$$z_f = \frac{1}{R_{FB1}C_{D2}} \quad (19)$$

C_{o1} and C_{o2} are the lumped capacitance, so the non-dominant poles p_2 and p_3 will shift to a higher frequency than the unity-gain frequency (UGF). To cancel the effect of non-dominant poles in the designed LDO regulators, the zero z_f should be lower than poles p_1 and p_f, so R_{FB2} should be much smaller than R_{FB1}, i.e. $z_f << p_f$. That is to say, the effect of the pole p_1 can be cancelled by z_f. To ensure z_1 be left-plane zero, R_{D1} should be selected much larger than $1/g_{md7}$. At the same time, since C_{D1} and C_{D2} are the compensation capacitor, it is practical to take the assumption of $z_1 < p_f$ by optimizing resistors R_{D1} and R_{FB1}, and compensation capacitors C_{D1} and C_{D2}. From the above discussion, the LDO regulator will be stable because it is similar to a single pole system. Fig.5 shows the simulated open-loop frequency response of the designed LDO regulator. Simulation results show that the phase margin is about 61°, which is sufficient to ensure the loop stability of LDO regulator.

C. Analysis of PSRR

To improve the PSRR of piecewise-linear BGR, a LDO regulator is adopted in this paper, as shown in Fig.3. The operating supply voltage of core circuit of piecewise-linear BGR is the output voltage V_{REG} instead of power supply voltage V_{DD}. Therefore, the PSRR of piecewise-linear BGR with LDO regulator will be improved. Under the condition of low frequency, the PSRR can be quantitatively analyzed as follows.

For convenience, it is assumed that g_{mj} and i_{mj} are, respectively, the transconducatnce and the small-signal drain current of transistor M_j, here j=1, 2, 3…. Assumed that power supply voltage has an incremental variation v_{dd}, the incremental current i_{b1} of M_{B1} can be derived as

$$i_{b1} = \frac{v_{dd}}{\frac{1}{g_{mb1}} + g_{mb3}R_{B1}r_{dsb3}} \quad (20)$$

where, r_{dsb3} is the source-drain resistance of M_{B3}. M_{B1} and M_{B2} form current mirror pair, and they are entirely the same. Therefore, the gate-source variation v_{bias} of M_{B4} can be derived as

$$v_{bias} = \frac{v_{dd}}{g_{mb4}(\frac{1}{g_{mb1}} + g_{mb3}R_{B1}r_{dsb3})} \quad (21)$$

Assumed that v_{reg} is the output voltage variation of LDO regulator, and the feedback voltage variation v_{fb} can be derived as

$$v_{fb} = \frac{v_{reg}}{R_{FB1} + R_{FB2}} R_{FB2} \quad (22)$$

As shown in Fig.3, the error amplifier of LDO regulator is made up of MOS transistors M_{D1}~M_{D7}, resistor R_{D1} and compensation capacitor C_{D1}. To simple the analysis, it is assumed that the dc gain A_v of error amplifier is far greater than 1, i.e. $A_v >> 1$. Neglected the effect of drain current variation of M_{D1} and M_{D6}, the gate voltage variation v_{gpass} of power transistor M_{PASS} can be derived as

$$v_{gpass} = \frac{A_v R_{FB2} v_{reg}}{R_{FB1} + R_{FB2}} - \frac{A_v v_{dd}}{g_{mb4}(\frac{1}{g_{mb1}} + g_{mb3}R_{B1}r_{dsb3})} \quad (23)$$

According to (20) ~ (23) and the Kirchhoff current law (KCL) at the output node VREG of the LDO regulator, it is derived as

$$\frac{v_{reg}}{v_{dd}} = g_{mpass}R_{eq-L}\frac{1 + \frac{A_v}{g_{mb4}(\frac{1}{g_{mb1}} + g_{mb3}R_{B1}r_{dsb3})}}{1 + g_{mpass}R_{eq-L}\frac{A_v R_{FB2}}{R_{FB1} + R_{FB2}}} \quad (24)$$

where, R_{eq-L} is the equivalent resistance seen from node VREG to ground. In the similar way, it is assumed that v_a, v_b and v_1 are, respectively, the voltage variations at node A, node B and node 1. So, v_a and v_b can be derived as

$$v_a = g_{m1}(v_{reg} - v_1)r_a \quad (25)$$

$$v_b = g_{m2}(v_{reg} - v_1)r_b \quad (26)$$

where, r_a and r_b are the resistance seen from node A and node B to ground respectively. Amplifier A_1 and A_2 are entirely the same, and whose dc gain A_d is far greater than 1, i.e. $A_d >> 1$. In Fig.3, the voltage variation v_1 at node 1 has that $v_1 = A_d \times (v_b - v_a)$. According to (25) and (26), it is derived as

$$v_1 = \frac{A_d g_{m1}\beta v_{reg}}{1 + A_d g_{m1}\beta} \quad (27)$$

where, $\beta = r_b - r_a$. MOS transistors M_1, M_2, M_5 and M_6 are entirely the same, and it is concluded that $g_{m1} = g_{m2} = g_{m5} = g_{m6}$. Therefore, it is derived as

$$i_{1,2,5,6} = g_{m1}\frac{1}{1 + A_d g_{m1}\beta}v_{reg} \quad (28)$$

The voltage variation v_2 at node 2 has that $v_2 = A_d \times (v_c - v_b)$, here v_c is voltage variation at node C. MOS transistors M_3, M_4 and M_9 are entirely the same, and it is concluded that $g_{m3} = g_{m4} = g_{m9}$. In the similar way, it is derived as

$$i_{3,4,9} = g_{m3}\frac{1 + A_d g_{m1}\beta + A_d g_{m1}r_b}{(1 + A_d g_{m1}\beta)(1 + A_d g_{m4}R_2)}v_{reg} \quad (29)$$

Transistors M_7 and M_8 form the current mirror pair, and transistor M_8 has the aspect ratio that is α times that

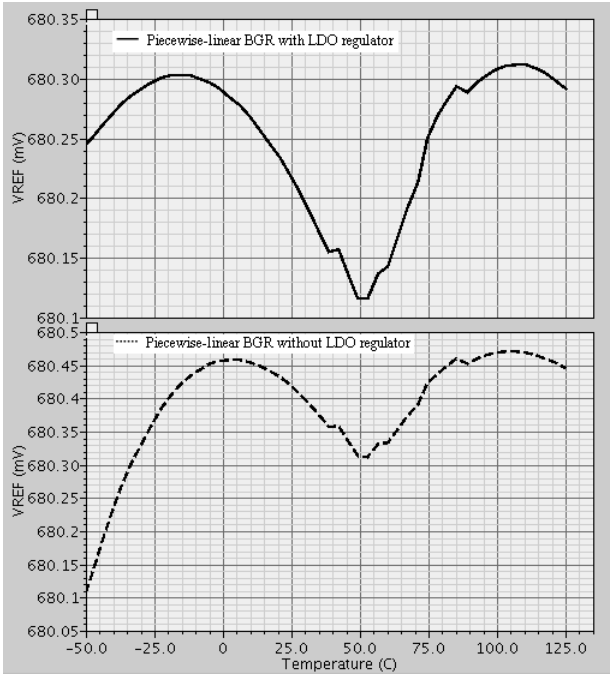

Figure 6. Output voltage V_{REF} of piecewise-linear BGR with- and without- LDO regulator as a function of temperature T

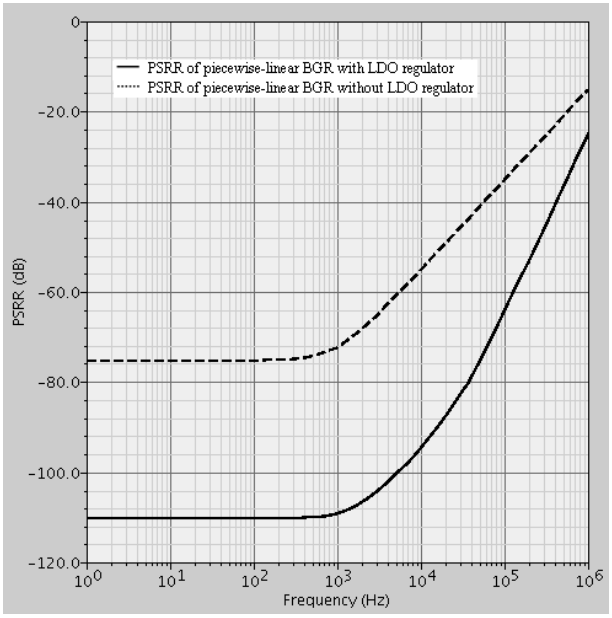

Figure 7. Simulated PSRR of piecewise-linear BGR with- and without- LDO regulator

of transistor M_7. Transistors M_{10} and M_{11} are entirely the same, so it is derived as

$$i_{11} = \alpha g_{m1} \frac{1}{1+A_d g_{m1}\beta} v_{reg} - g_{m3} \frac{1+A_d g_{m1}\beta + A_d g_{m1} r_b}{(1+A_d g_{m1}\beta)(1+A_d g_{m4} R_2)} v_{\text{reg}} \tag{30}$$

To simple the analysis, it is assumed that $A_d g_{m1}\beta >> 1$ and $A_d g_{m4} R_2 >> 1$. According to (28) ~ (30) and KCL at the output of BGR, it is derived as

$$\frac{v_{ref}}{v_{\text{reg}}} \approx R_3 \frac{\beta + r_b}{\beta A_d R_2} + \frac{R_3 + (1+\alpha)R_4}{A_d \beta} \tag{31}$$

where, v_{ref} is the output voltage variation of piecewise-linear BGR with LDO regulator. Therefore, the PSRR of the designed piecewise-linear BGR with LDO regulator can be written as

$$PSSR_{dB} = 20\lg\left|\frac{v_{ref}}{v_{vdd}}\right| = 20\lg\left|\frac{v_{ref}}{v_{reg}} \times \frac{v_{reg}}{v_{dd}}\right| = 20\lg\left|\frac{v_{ref}}{v_{reg}}\right| + 20\lg\left|\frac{v_{reg}}{v_{dd}}\right| \tag{32}$$

According to (24), (31) and (32), it is concluded that the PSRR of the designed piecewise-linear BGR will be improved significantly by adopting the LDO regulator.

IV. Simulation Results

To confirm the circuit of the designed piecewise-linear BGR in this paper, the piecewise-linear BGRs with- and without- LDO regulator are designed and simulated in SMIC 0.18μm CMOS process with 1.35-V power supply voltage.

Fig.6 shows the output voltage V_{REF} of piecewise-linear BGR with- and without- LDO regulator as a function of temperature T with 1.35-V power supply voltage. Simulation results show that the temperature coefficient of the piecewise-linear BGR without LDO regulator is 2.89ppm/ºC when temperature varying from -50 ºC to 125 ºC. And, the output voltage V_{REF} of piecewise-linear BGR with LDO regulator has only the temperature coefficient of 1.65ppm/ºC.

The simulated PSRR of piecewise-linear BGR with- and without- LDO regulator is shown Fig.7. The piecewise-linear BGR with LDO regulator at 10Hz, 100Hz, 1kHz, 10kHz and 100kHz achieves , respectively, -110.42dB, -110.41dB, -109.18dB, -94.65dB and -64.51dB. And the piecewise-linear BGR without LDO regulator at 10Hz, 100Hz, 1kHz, 10kHz and 100kHz achieves, respectively, -75.35dB, -75.31dB, -72.28dB, -55.19dB and -35.23dB. Compared to the piecewise-linear BGR without LDO regulator, the designed high PSRR piecewise-linear BGR with LDO regulator has an improvement of PSRR with about 35dB, 36.9dB and 29.28dB at 10Hz, 1kHz and 100kHz respectively. Therefore, the PSRR improvement is achieved by adopting LDO regulator.

Fig.8 shows the simulated line-regulations of piecewise-linear BGR with- and without- LDO regulator. When power supply voltage V_{DD} varies from 1.2V to 7V, the output voltage deviation of piecewise-linear BGR without LDO regulator is 3.83mV, but the output voltage deviation of piecewise-linear BGR with LDO regulator is only 98.23μV. Compared to the piecewise-linear BGR without LDO regulator, the piecewise-linear BGR with

TABLE I.
PERFORMANCE SUMMARY OF BANDGAP REFERENCE

		Reported BGR				Designed BGR in this paper	
		[4]	[5]	[16]	P[17]	without LDO regulator	with LDO regulator
Process		0.5μm BiCMOS	0.13μm CMOS	0.25μm BiCMOS	0.09μm CMOS	0.18μm CMOS	0.18μm CMOS
Power supply voltage (V)		1.6	0.9	2.7	2.7	1.35	1.35
Output voltage		1.285 V	0.615 V	1.26 V	213.982 mV	0.68 V	0.68 V
Temperature coefficient (ppm/ ºC)		7.2	6.5	276.67	6.071	2.89	1.65
Temperature range (ºC)		-40 ~ 100	-50 ~ 150	0 ~ 100	-20 ~ 120	-50 ~ 125	-50 ~ 125
PSRR@ 25 ºC	10Hz	-70 dB			-82.7 dB	-75.35 dB	-110.42 dB
	100Hz			-82 dB		-75.31 dB	-110.41 dB
	1kHz	-69 dB		-79 dB		-72.28 dB	-109.18 dB
	10kHz			-64 dB		-55.19 dB	-94.65 dB
	100kHz	-35 dB		-48 dB		-35.23 dB	-64.51 dB

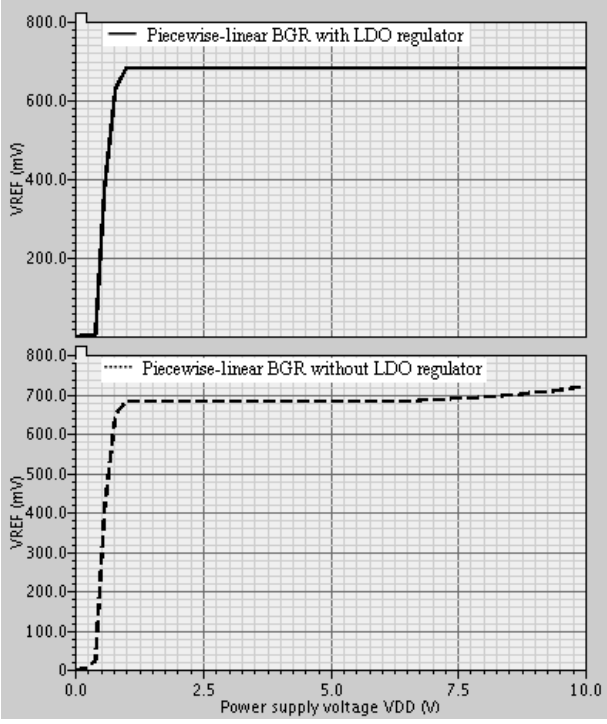

Figure 8. Simulated line-regulation of piecewise-linear BGR with- and without- LDO regulator

LDO regulator has a well line regulation. Finally, to provide an evaluation on the designed high PSRR BGR with LDO regulator in this paper, comparison of some reported BGR is shown in Table I. As shown in Table I, the designed piecewise-linear BGR with LDO regulator has a well performance.

V. CONCLUSIONS

A CMOS high PSRR piecewise-linear BGR, which has an output below 1V, has been designed and analyzed in this paper. Compared to piecewise-linear BGR without LDO regulator, the designed high PSRR piecewise-linear BGR achieves high PSRR performance by adopting LDO regulator. Simulation results shows that the designed high PSRR piecewise-linear BGR with LDO regulator provides an output voltage with excellent stability, a low temperature coefficient, and high PSRR performance. It is well suited for analogue and mixed signal systems.

ACKNOWLEDGMENT

This work was supported in part by a grant from National Science Foundation of China (Grant No. 61102075, and 61301124), Natural Science Foundation Project of CQ CSTC (Grant No. CSTCJJA40011 and CSTC2010BB2412), Science and Technology Research Project of Chongqing Education Commission (Grant No. KJ120503, KJ120507, and KJ120533), Dr. Start Fund of Chongqing University of Posts and Telecommunications (Grant No.A2010-09), 2013 University Innovation Team Construction Plan Funding Project of Chongqing, and Special Project of Internet of Things from Ministry of Industry and Information Technology, Chongqing Development Plan of Innovative Young Talents (Grant No. cstc2013kjrc-qnrc0126).

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