Researching and optimizing key technology of HDR analog signal chain in the satellite communications

Shuai Zhang
School of Electronic Information, Wuhan University, Wuhan, China, 430072
E-mail: shuai173@whu.edu.cn

Shilei Sun*   Yongqiang Cui   and   Dexiang Deng
Institute of Microelectronics and Information Technology, Wuhan University, Wuhan, China, 430072
School of Electronic Information, Wuhan University, Wuhan, China, 430072
School of Electronic Information, Wuhan University, Wuhan, China, 430072
E-mail: sunsl@whu.edu.cn, cuiyq@whu.edu.cn, whuddx@gmail.com

Abstract— **Due to the low dynamic range of the analog front end, low respond speed, bad flatness of the Amplitude-frequency characteristics and the poor noise suppression capability of the signal conditioning in the analog signal chain of the traditional digital down converter (DDC) system, an improved analog signal chain scheme used in high data rate receiver (HDR) of the satellite communication system has been put forward. This scheme has 55dB dynamic range, high respond speed and good noise suppression capability. Moreover, it has been realized on the platform of the ground terminal HDR for demodulator system. 720MHz and 1.2GHz intermediate frequency conversion is an important component of the satellite ground monitoring X-band data channel receiver system. The scheme consists of a band-pass filter module, a digital control variable gain amplifier (VGA), a low noise amplifier (LNA), a radio or intermediate frequency gain block and an ADC which has 1.7GHz input bandwidth. It realizes sampling and conditioning of the 720MHz and 1.2GHz intermediate frequency signal and automatic gain control (AGC). Experimental results show that the scheme has the characteristics: automatic and fast gain control, wide dynamic range and good amplitude-frequency characteristics of the gain points in the pass-band, low power consumption and good noise suppression capability.**

Index Terms— Down conversion system, digital down converter, Analog signal conditioning, Automatic gain control, High speed ADC sampling

I. INTRODUCTION

With the rapid development of the world communication standards and protocols, flexibility and adaptability has become one of the most important characteristics of modern communication. Designing more efficient architectures which support multiple communication protocols and enhancing the data transmission speed and the data capacity amount have become an inevitable trend. To reduce the restrictions of the analog signal chain in the communication system, researchers have to introduce greater amounts of digital signal processing and optimizing algorithms. Future development of the communication system will face great challenges [1]. In addition, with the rapid development of the semiconductor technology, analog integrated circuits, signal processing technology and the production process of the analog chips and printed circuit boards, key parameters of low noise amplifier (LNA) and analog digital converter (ADC) in RF and IF filters have been improved significantly. It provides reliable technical support for us to improve the traditional analog front-end of receiver circuit.

The design of UWB receivers exposes to unique challenges [2]. According to the related material of the aerospace remote sensing, when the ground resolution of the image approaches 1 meter, the real-time data capacity reaches 1.7Gbps. Considering compression ratio is 1:5, real-time pure data transmission from satellite to ground is 340Mbps. In USA, the 300Mbps satellite transmission system has been instantiated. 650Mbps and 1Gbps satellite high data rate transmission system is being researched or experimented. In 2002, NASA proposed to use OFDM system to achieve a 622Mbps modem system [3]. Japan is also researching on the 1.2Gbps data transmission system.

In terms of the current situation of space data transmission, the transmission rate from satellite to ground or between satellites is far from enough. HDR technology has been used in satellite communication navigation and monitoring communication network. In recent years, satellite ground demodulation receiving system of 720Mbps and 1.2Gbps IF have been researched or experimented. Based on the key technology of front-end analog chain of the traditional HDR system, improved scheme is proposed and the result is shown in this paper.

Figure 1 shows the structure diagram of the traditional ground demodulation receiving system. The scheme consists of three parts: RF down converter, IF analog signal conditioning and digital down converter in Field Programmable Gate Array (FPGA). Part 1: RF down

converter. The antenna receives the C / X / Ku / Ka band satellite signal and send it to the down converter. Then the down converter gets the expected IF signal. This part is separated from the HDR system and composes RF down converter. In the traditional satellite communication, the data rate of down converter is generally no more than 375Mbps. Rear-end analog signal chain and digital data processing are based on this data rate. However, in recent years, in the research of higher rate satellite communication, research and optimization on traditional key technology for higher speed transmission needs to be done.

   Part 2 and Part 3 compose HDR demodulator system (this paper focuses on research and optimization analog signal chain in these two parts). Part2: IF analog signal conditioning. IF signal connects to the conditioning circuit of the analog front-end signal through dedicated coaxial interfaces, such as SMA or BNC. IF signal is output by different satellite down converters. To sample the IF signal, the LNA module conditions it by fixed gain and sends it to ADC in single-ended signal or

differential signal.   In the traditional receiver, the ADC performance is more dependent on the power and SNR of IF signal in the down converter. It may leads to many problems, such as too low signal amplitude, low resolution, signal saturation and distortion. In addition, the analog signal chain that is composed of a fixed gain amplifier and an ADC has narrow signal bandwidth and poor anti-jamming capability. Part 3: Digital down converter in FPGA. After sampling the signal entering the FPGA platform-based DDC processing module. The traditional DDC system consists of a local oscillator (NCO), a mixer, filter, a half-band filter (FIR&HBF) and a extractor (CIC). Its main function is to change the IF signal to zero-IF signal and to reduce the sample rate [4]. The spectrum shows that the digital down converter transforms the signal sampled by ADC from RF signal to baseband. It is completed by two steps: Firstly, the quadrature carrier multiplies the input signals. Then the digital filter eliminates the unwanted frequency components. If the sampling rate is higher than 600MHz, it is difficult to do real-time processing in FPGA [5].
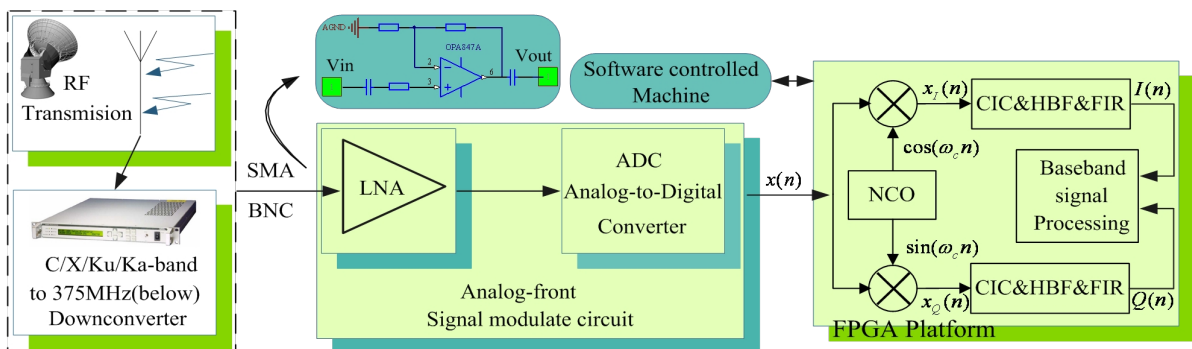

Figure 1.   Traditional ground demodulation receiving system

The traditional DDC system has the shortcomings of large amount of computation, low utilization of logical resource and is difficult to process the RF signal simultaneously. Though many researchers have proposed improved schemes of the multi-channel digital down conversion to solve these problems, huge challenge still exists due to the rapid development of demodulation rate

[6]. This paper presents an optimization of the analog front-end signal chain to reduce the difficulty of the back-end FPGA processing. It significantly reduces resource consumption of the back-end digital AGC and FIR in FPGA. It also reduces the error rate brought by multipath transmission and deep fading and demodulation loss of the receiver.
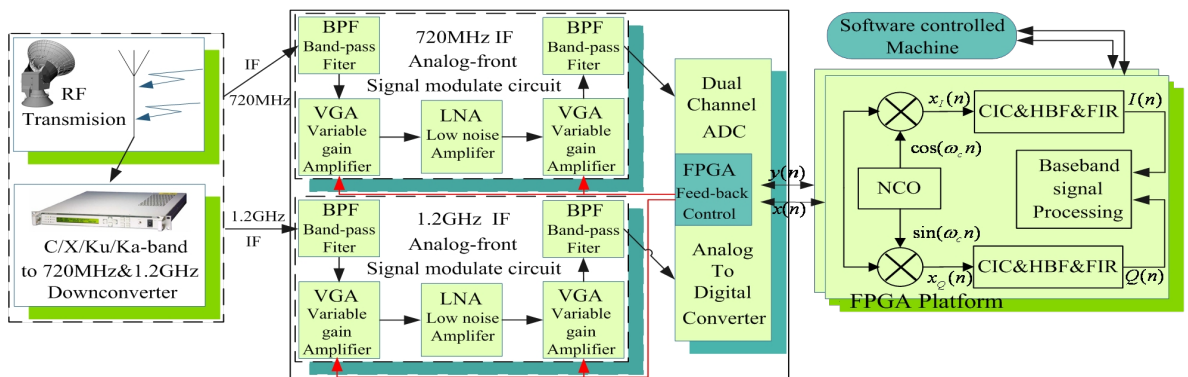

Figure 2.   Ground demodulation receiver system

II. SYSTEM STRUCTURE OF THE HDR RECEIVER

Traditionally, the signal is digitized at a low frequency. However, with the rapid development of the fields such

as radar, communication and electronic instruments, the frequency has gradually changed to IF and even to RF [7]. For example, the improvement of data transmission rate, carrier frequency and IF signal frequency has higher demand for the HDR system.

For the 720Mbps and 1.2Gbps IF satellite ground demodulation receiving system that was proposed recently, this paper puts forward an improved scheme of the key technology of the analog signal chain. Figure 2 shows the design diagram of the demodulation system. Compared with the third parts of the traditional receiver, the front-end IF signal in part1 increases from 375MHz to 720MHz and 1.2GHz. Two channels $x(n)$ and $y(n)$ are processed simultaneously on FPGA-based platform in part3. The analog signal chain is an improved scheme proposed in this paper. Through BPF, variable gain amplifier (VGA), LNA and high-speed ADC, the scheme realizes automatic gain control of IF signal, band-pass filtering and high-speed ADC sampling [8].

III. COMPARISON OF THREE HDR FRONT-END ANALOG SIGNAL CHAIN SCHEMES

The output IF frequency of the RF down converter (in door) is 720±200MHz or 1.2GHz±300MHz. The impedance of it is 50Ω. The first scheme uses RF/IF Gain Block. For example, the ADL5542 integrates channel impedance matching circuit and 20dB fixed gain amplifier circuit. This scheme has simple structure and good amplitude-frequency characteristic. Its fluctuation from 500MHz to 1.5GHz is less than 1dB. However, the fatal defect is that it cannot adjust the amplitude of the IF signal, which may leads to the problems of too low amplitude of the IF signal, bad resolution signal saturation and distortion. It makes an unrecoverable effect on the subsequent ADC sampling and FPGA processing [9]. In the second scheme, discrete AGC module is used to automatically adjust the gain according to the amplitude of the input signal, so that the output voltage of this module maintains in the optimum range of the ADC's input power [10]. Figure 3 shows the structure diagram of the second scheme. The core module is the gain controlled amplifier adjusted by the voltage signal. The voltage signal is automatically generated by a loop that is composed of an electric level detector (peak value detection circuit), a low pass filter, a DC amplifier, a voltage comparator and a control voltage generator.

The input signal of the discrete AGC $u_i = \cos \omega t$. The output signal $u_o = U_{im} \cos \omega t$. The gain $A_u = U_{om}/U_{im}$. The gain A_u is controlled by the control voltage u_c. The control voltage is obtained after the conversion of the error voltage generated by the voltage comparator via a control voltage generator. Independence is the advantage of discrete AGC. The internal closed-loop control amplitude of the output signal adjusts the IF signal to the most suitable power for ADC sampling. However, the structure is complex and has too many discrete components. In addition, when the processing analog signal is around 1 GHz, the amplitude-frequency characteristic within the pass band has high jitters and the different gain characteristics have poor consistency.

Considering the advantages and disadvantages of the first two schemes, this paper proposes a new analog channel conditioning scheme. Figure 2 shows the design of analog signal chain. This scheme has the advantages of low structure complexity and improves the jitter performance of the amplitude-frequency characteristic and the consistency under different gain. In addition, it realizes automatic gain control, solving the problems in the first scheme that the amplitude of the IF signal cannot be controlled flexibly. Moreover, this scheme has the advantages of wide dynamic range of gain, high respond speed of conditioning, low power consumption and good capability of noise suppression [11].
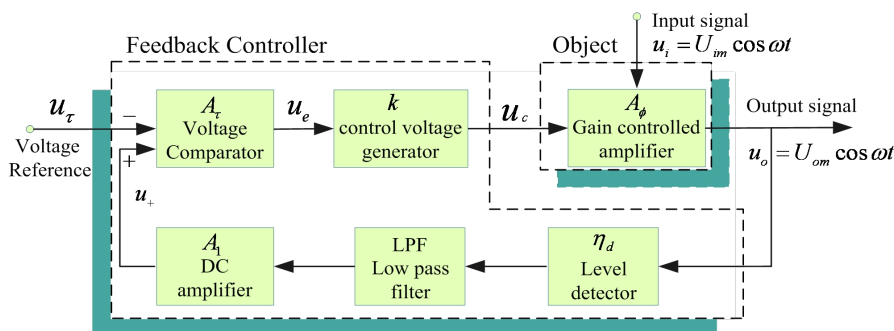

Figure 3.   Structure diagram of discrete AGC

To support synchronous demodulation of dual-channel satellite data, the scheme uses two different center frequencies and bandwidths of the BPF and handles IF signal of two channels. In terms of one channel, when the IF signal enters the HDR demodulation system, firstly, the IF signal filters the low frequency and high frequency interference through a BPF. Secondly the output signal enters the next level of digital control VGA. Its gain is controlled by FPGA signal processing end, realizing 30dB gain conditioning [12]. Thirdly, it realizes fixed gain of 20dB through the LNA. Then the HF noise and external interference that is brought in the

front-end analog chain are filtered through VGA and BPF. Finally, it is changed to differential signal through the 30~1800MHZ RF transformer and enters dual-channel 8-bit ADC. The ADC supports dual-channel simultaneous sampling.   The maximum speed of the inside sample-and-hold element reaches 1.7Gbps in the case of dual-channel sampling and reaches up to 3.4Gbps in the case of single-channel sampling. The digital signal sampled decreases its speed by 1:2 inside the ADC. Then it is sent to FPGA as level mode of 32

pairs differential LVDS signal. Considering that the maximum transfer rate of the 32 pairs of LVDS signal is still around 1.5Gbps, to maintain synchronization and low crosstalk between signals, a differential serpentine long wire is often used for connecting FPGA when designing the PCB. To better match with the differential bank receiver end of FPGA, 100Ω characteristic impedance is used for designing transmission wire Figure 4 shows the circuit of the scheme.
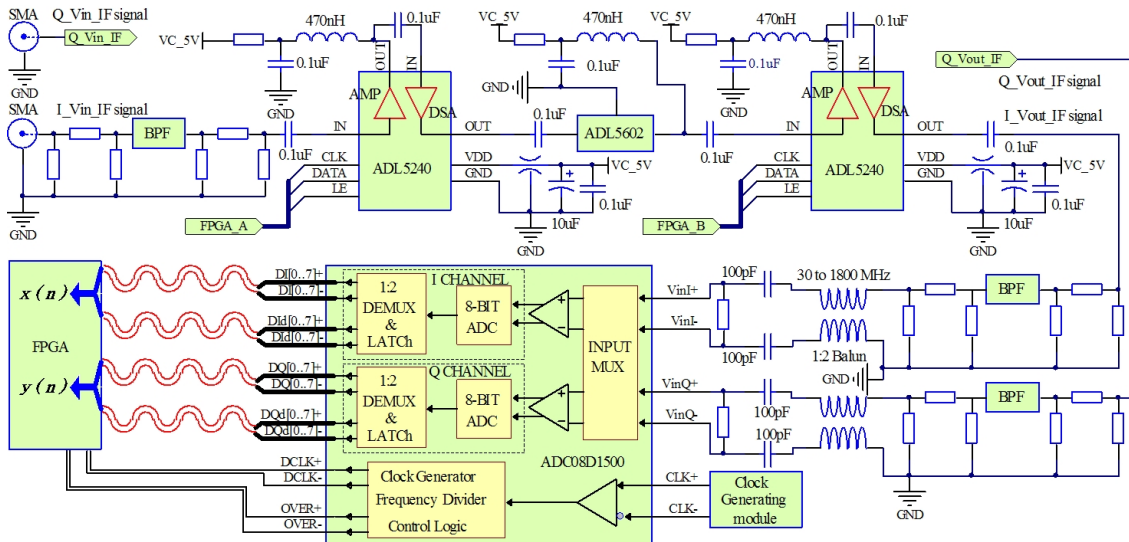

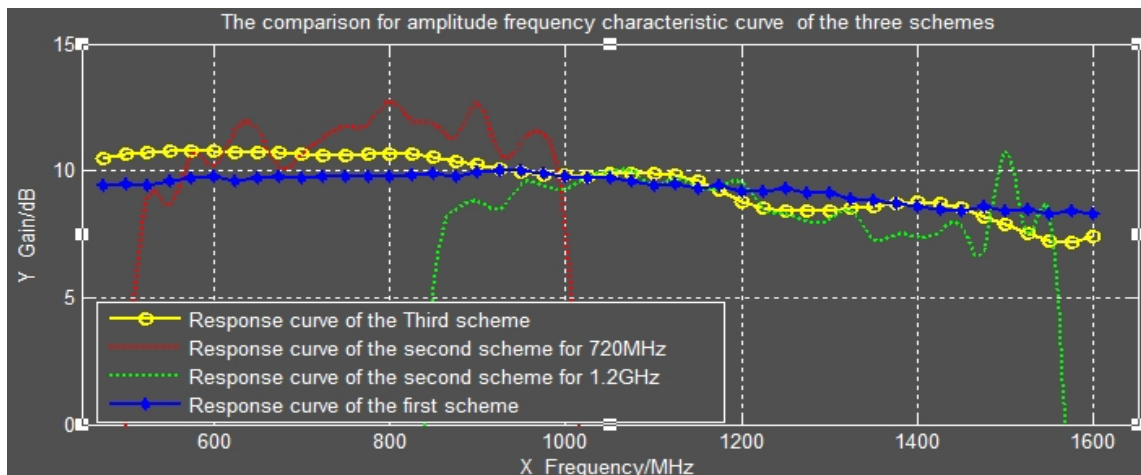Figure 4.   New scheme diagram of analog channel conditioning

Figure 5.   The amplitude-frequency characteristics of these three schemes

Through PCB test of these three analog signal chains, the comparison chart of the key indicators of the analog signal chain is achieved by simulating actual data. Figure 5 shows the response curves of the amplitude-frequency characteristics of these three schemes. The input signal is -10 dBm and the frequency ranges from 500MHz ~ 1.6GHz. Simulate and compare the gain of these three schemes in MATLAB. It can be seen clearly that the blue curve that stands for the first scheme has the best flatness within the pass band, only 1.7dB. The third scheme also has good flatness within the pass band. In particular, within the band range of 720 ± 200MHz or

1.2GHz ± 300MHz, its fluctuations are less than 0.73dB or 2.07dB. Fluctuation within the pass band of the third scheme is the largest and irregular. Within the band range of 720 ± 200MHz or 1.2GHz ± 300MHz, its fluctuation is 4.1dB or 3.9dB. From the spectral response, the third scheme overcomes the defects in the first scheme that the amplitude cannot be adjusted flexibly. Furthermore, it improves the intolerable band jitter in the second scheme. So it is the best analog signal chain for HDR demodulation system.

For HDR demodulation system, consistency of the respond curve under different gain is also very important.

Figure 6 shows the respond curve of the amplitude under different gain. Set different power of the input signal. The gain of the analog front-end ranges from -5dB to 50dB. The frequency ranges from 500MHZto 1.6GHZ. Simulating data is achieved by MATLAB. Good consistency of the respond curve under different gain is shown clearly. Conclusion can be made that the max actual dynamic range measured reaches 55dB. Consistency under different gain is good.
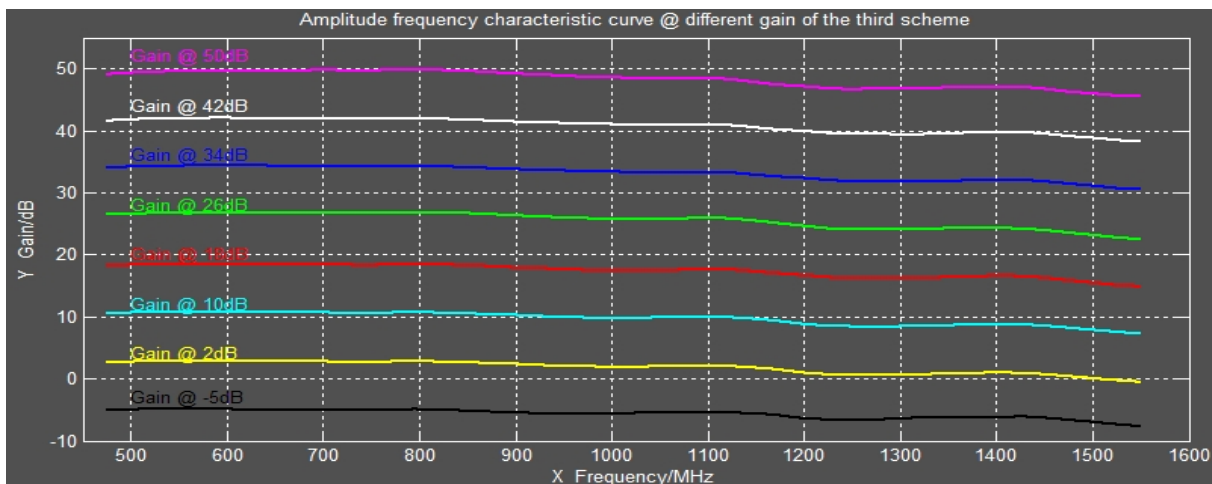

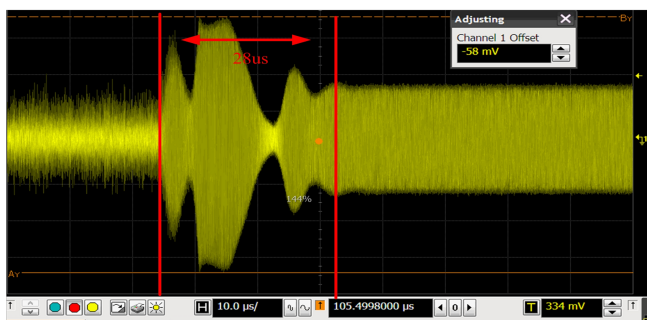Figure 6. Amplitude-frequency characteristic curves under different gain in the third scheme

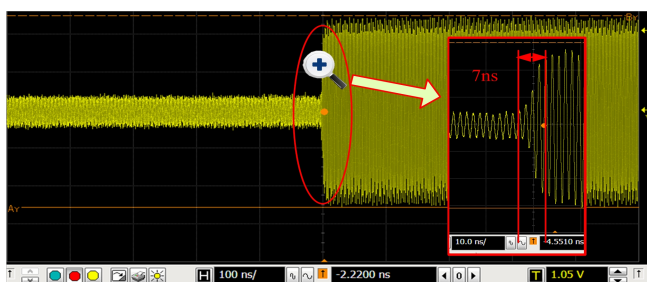Figure 7. Respond time of AGC in the second scheme

Figure 8.   Respond time of AGC in the third scheme

In wireless communication, due to the impact of various factors such as climate, environment and distance, the amplitude of the received signal fluctuates randomly [13]. For a better conditioning of the signal of analog front-end, the chain is required to have a quick response characteristic of the AGC. Figure 7 and Figure 8 show the comparison figures of the respond time in the second and third scheme. There is a big difference between them. The respond time of the second scheme is 28us, which has an obvious process of adjusting signal output. The process is an inevitable result of co-adaptation of the inside peak detection circuit of Figure 3, voltage comparator and control voltage generator. While the third scheme controls the gain of digital signal directly and has high sensitivity. In addition, the respond time is only 7ns. So it has more advantages than the second scheme.

The third scheme has 2.9dB noise figure at 2.14 GHz, single supply operation from 4.75 V to 5.25 V, low quiescent current of 275mA and power consumption of 1.4W. The second scheme has actual test data of supply from 12V to 15V, working current 810mA and power consumption 19.7W.

However, the AGC in the third scheme is not a pure combination of analog circuits. It has digital peak detection of ADC. Therefore, the third scheme can be used in the HDR system or similar systems, other systems without ADC are not appropriate.

The test results show that the new scheme can automatically adjust the signal gain. It has 55dB wide dynamic range, 7ns respond time, and only 1.7dB amplitude-frequency characteristics of the gain points in the pass-band.

IV. Research of several key points in the PCB designing for high-speed analog signal chain

It is known that circuit design and detection of high-speed analog signal chain has great difference with that of the low-speed analog signal chain, especially when supporting a maximum 1.5GHZ analog chain band. In this paper, research and exploration are done from three directions.

(1). How will the material of PCB impact on the high frequency characteristic

(2). Impedance matching, 90° and R wiring of PCB

(3). Split of the power supply and ground

Dielectric constant of FR4(R-1766) @ 1MHz is 4.7.

In the type of low dielectric constant, dielectric constant of R-5715J and R-5755 @1MHz is 3.8 and 3.5 respectively. The smaller the dielectric constant tangent ($\tan \delta$) is, the more suitable for wiring in HF and high-speed circuit. The bigger dielectric constant of the material is, in the same frequency the more blunt the eye diagram is. This difference is obvious when the frequency is 2.5GHz and 10GHz [14].

The impedance design of the analog signal chain is key to signal integrity. Any impedance mutation can cause the signal reflection and distortion [15]. Characteristic impedance Z_0 of the micro strip line is

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln(\frac{5.98h}{0.8w + t}) \qquad (1)$$

In formula (1), ε_r is the material dielectric constant. h is the dielectric thickness between the wire and the base level. w is the width of the wire. t is the thickness of the wire. Each RF trace on our test board has a characteristic impedance of 50 Ω and is fabricated on FR4(R-5755) material. In addition, each trace is a coplanar waveguide (CPWG) with a width of 25 mils, a spacing of 18 mils, and a dielectric thickness of 10 mils. Then Z_0 =50.16Ω, which matches well with single-ended analog channel transmission.

PCB wiring of the key signal chain is very important

to impedance matching. Figure 12 shows the TDR wiring for two kinds of wiring [16]. Conclusion can be made that impedance of R wiring almost has no change. So all of the analog signal-chains adopt R wiring on the test PCB, reducing the uncertain signal reflection brought by impedance change.

When designing the test PCB, the impact of power supply and segment of signal grounds on analog signal chain has been considered carefully [17]. Power supply of the analog chain and ADC digital supply circuit should be independent of each other in the spatial layout of the circuit board and the current path. The module of power supply single-point common ground a used. To get better test results, cellular shield shell and full shielding are used. In addition, the architecture of daughter board and the mother board is designed to reduce the interference between the external environment and the power supply. Figure 13 shows the two test PCBs that are used to test the analog signal chain. The lower half part is the physical picture described in the second scheme and the upper half part is the physical picture described in the third scheme. After the test, we draw the conclusion that R wiring reduces the in-band fluctuations by 2.3 dB compared with the 90 ° wiring.
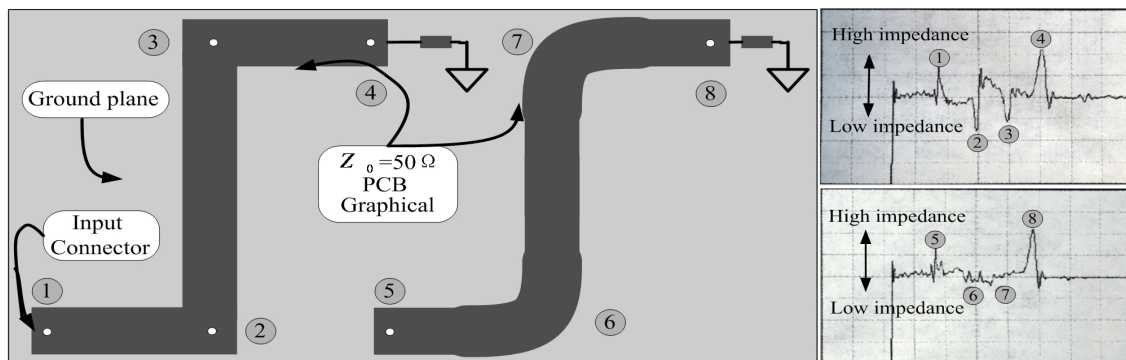

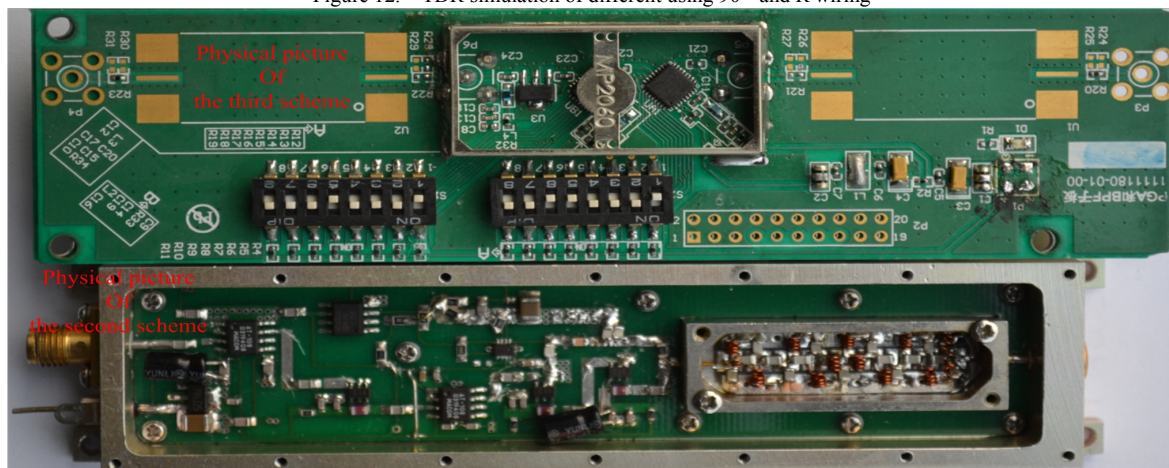Figure 12.   TDR simulation of different using 90 ° and R wiring

Figure 13.   Physical pictures of the two schemes

V. CONCLUSION

In this paper, an optimization scheme of analog signal chain that has wide dynamic range, high respond speed

and good noise suppression capability is realized. Sampling, conditioning and automatic gain control (AGC) of the 720MHZ and 1.2GHZ IF analog signal is achieved through a band-pass filter module, a digital control variable gain amplifier (VGA), a low noise amplifier (LNA), a RF and IF gain block and 1.7GHZ wide input band. The amplifier can be controlled fast and automatically. It has wide dynamic range, good amplitude characteristic at the gain point within the pass band, low power and good noise suppression capability. Moreover, the scheme can be extended to the satellite broadband signal receivers and the analog signal chain of related application of signal detection, modulation, demodulation and identification.

REFERENCES

[1] Paolo Zicari, Emanuele Sciagura, Stefania Perri, Pasquale Corsonello, "A programmable carrier phase independent symbol timing recovery circuit for QPSK/OQPSK signals", Microprocessors and Microsystems, vol. 32, pp.437-446, 2008.

[2] Y. Vanderperren, Geert Leus, W. Dehaene, "An approach for specifying the ADC and AGC requirements for UWB digital receivers", IET Seminar on Ultra Wideband Systems, Technologies and Applications, vol. 10, no. 4, pp.169-200, 2006.

[3] MuliKifeThoms P. Bizon Dale J. Mortensen IMPLEMENTATION OF A 622 MBPS OFDM DIGITAL MODEM 20th AIAA International communication satellite Systems Conference and Exhibit 12-15 may 2002 Montreal, Quebec, Canada

[4] Zhang Qingxiang, Su Xiaoxiao, "The Design of Digital Down Converter Based On FPGA", 2012 International Conference on Wireless Communications, Networking and Mobile Computing, WiCOM 2012, Conference article (CA).

[5] Deng Xiaoping, Tian Mao, Luo Yijun, Wang Yuhao，"Optimization and implementation of universal multi-channel digital down-converter", Chinese Journal of Scientific Instrume t, vol. 32, no. 9, pp.1993-1997, 2011.

[6] Xiaoting Chen, Guodong Zhao, Ping Jin, Wenbin Gong, Huijie Liu, Xuwen Liang, "QPSK/OQPSK signal detection with IFAGC on LEO satellite", IEEE 2007 International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, MAPE, pp.1179-1182, 2006, IEEE 2007 International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications.

[7] Chang Liu, Yue-Peng Yan, Wang-Ling Goh, Yong-Zhang Xiong, Li-Jun Zhang, Mohammad Madihian, "A 5-Gb/s automatic gain control amplifier with temperature compensation", IEEE Journal of Solid-State Circuits, vol. 47, no. 6, pp.1323-1333, 2012.

[8] Park Jeong I.L, Park Hwa Se, "A study on demodulation system design of the VOR receiver", Communications in Computer and Information Science, vol. 184 CCIS, no. Part I, pp.343-349, 2011.

[9] Lu Hao, Wang Zhen-Zhan, "Design of 1.2GHz bandwidth digital-correlator in fully polarimetric microwave radiometer", 2011 International Conference on Electric Information and Control Engineering, ICEICE 2011 - Proceedings, pp.4084-4087, 2011,   2011 International Conference on Electric Information and Control Engineering.

[10] Deng Qing, Wu Jian-Hui, Shi Long-Xing, Sun Wen, Yun Ting-Hua "007 9th International Symposium on Signal Processing and its Applications", ISSPA 2007, Proceedings, 2007.

[11] Xuejun Li, Ke Wang, Lingli Jiang, "The Application of AE Signal in Early Cracked Rotor Fault Diagnosis with PWVD and SVM", Journal of Software, vol. 6, No.10, pp.1969-1976, 2011.

[12] Zhang Dawei, Huang Fengyi, Tang Xusheng, Sun Xiaopeng,"Design of VGA for 6 GHz radio frequency communication system", IEEE MTT-S International Microwave Workshop Series on Millimeter Wave Wireless Technology and Applications, IMWS 2012 - Proceeding, p 32-35, 2012.

[13] Wenxian Xiao, Zhen Liu, Wenlong Wan, Xiali Zhao, "Research on the Expected Synchronization of Autonomous System", Journal of Software, vol. 8, No.1, pp.85-92, 2013.

[14] Tadashi Kubodera, Fen Jie, Gai Qiang, Pan Dong, "Kousoku Digital Kairo Jissou Knowhow", CQ Publishing Co., Ltd., Tokyo, pp.4-9, 2002.

[15] Zhou Xiang, Liu Xue-Guan, Guo Hui-Ping, Shao Lv-Xia, "Design of broadband impedance transformer using coupled microstrip transmission lines", Proceedings - 2009 3rd IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, MAPE 2009, p 994-997, 2009.

[16] Umenyiora Chidubem Andrew, Druce R.L, Curry Randy D., Norgard Peter, McKee T., Bowders J.J., Bryan D.A, "Dielectric constant of sand using TDR and FDR measurements and prediction models", IEEE Transactions on Plasma Science, vol. 40, no.10 PART 1, pp.2408-2415, 2012.

[17] Hui Feng, Zeqi Yu, "The Correction Method for Power Noise in Digital Class D Power Amplifiers", Journal of Software, vol. 8, No 2, pp.488-494, 2013.

Shuai Zhang, Inner Mongolia, 1987, School of Electronic Information, Wuhan University, Wuhan, China, Ph.D Candidate.
Interest research: Signal Process, High Speed Circuit

Shilei Sun, Hubei, China, 1981, Institute of Microelectronics and Information Technology, Wuhan University, Wuhan, China, Associate Professor.
Interest research: Signal Process, Artificial Intelligence

Yongqiang Cui, Shanxi, China, 1988, School   of Electronic Information, Wuhan University,   Wuhan, China, Ph.D Candidate.
Interest research: Signal Process, Satellite Communications

Dexiang Deng,   Electronic Information School, Wuhan University, Wuhan, China, Professor, Ph.D. supervisor.