Design of A High-speed Parallel LDPC Encoder

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***Abstract*—In this paper, the traditional BP decoding algorithm of LDPC code is investigated in detail. The large computation load is a shortcoming of traditional BP decoding algorithm, and an improved BP decoding algorithm is then proposed to deal with the problem. In the iterative decoding process, the wrong bit information only needs to be updated for the decoding algorithm, which consequently improves the efficiency and reduces time-delay of decoding. According to the improved BP decoding algorithm, the high-speed parallel encoder is designed, which can be used in various distributed sensor network applications. Furthermore, the error correction performance of this high speed parallel encoder in the Gaussian channel is studied. The simulation is provided to illustrate that the improved high speed parallel encoder has lower computational complexity and higher decoding speed based on the premise of a little decoding performance loss.**

***Index Terms*—LDPC Code, BP decoding arithmetic, AWGN channel, high-speed Parallel decoder, iterative decoding algorithms**

I. INTRODUCTION

LDPC is a class of linear block codes which is a research focus in recent years. It was found by Gallager at first, and then also known as Gallager codes. With the development of computer hardware and its related theory, MacKay and Neal rediscovered LDPC. T J Richardson proved that LDPC combining with iterative decoding which was based on BP(Belief Propagation), had the approximation Shannon limit performance [1]. Due to its simple structure of the decoder, it can do parallel computation in theory and use fewer resources consumed to get high throughput, therefore it is considered to be one of the main channel coding in the future communication field. In recent years, internation on LDPC theory research and engineering applications and realization of the research on VLSI(very large scale integrated circuit) have made significant progress. The DVB-S2 standard channel coding, launched by European Telecommunications Standards Institute (ELSI), has adopted LDPC [2]. CCSDS131.1-O-2(EXPERIMENTAL SPECIFICATION), which was proposed to the Adivisory Committee of Space Data Systems by NASA, proposed different LDPC programs respectively according to the near earth business and deep space business. The WiMAX[3] and other communications standards have been successively adopted LDPC as channel coding. Therefore, LDPC will be widely applied to the field of communication in the near future [4-17].

Although LDPC decoding algorithm is linear complexity, the check matrix is usually random structure formation, and the corresponding decoder structure is relatively complex. Different application environment on decoder decoding rate and resource consumption have different requirements. in order to adapt different situations, it has appeared in three different hardware structures: full parallel structure, the serial structure and part of the parallel structure. The literature [18] used the cyclic shift matrix of the unit matrix as the basic unit, and constructed a parity check matrix of the LDPC to reduce the decoding complexity of the LDPC in the sum-product algorithm. Taking the encoding complexity of the LDPC into consideration, this paper presents one structure which can simplify the encoding.

According to the scheme of structure LDPC, we propose the method to eliminate its short loops on bipartite graph. The literature [19] proposed two termination criterions with low-complexity to reduce the decoder computation of PCGC (parallel cascade gallagercode, parallel concatenated gallercode). In full compliance with Digital Television Terrestrial Multimedia Broadcasting(DTMB), the literature [20] achieved a non-regular LDPC decoder which supports three kinds of bit rate (0.4, 0.6, 0.8) simultaneously with a code length 7493 bit. In this design, the use of a new memory call control strategy case than single bit rate only up to an increase of less than 5% of the memory to achieve the three kinds bitrate memory multiplexing. The literature [21] proposed a decoding algorithm on the basis

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of belief propagation algorithm according to the check matrix contains ring to the influence of the decoding algorithm. By promptly cut off the message on the ring retransmission loop, the algorithm, to eliminate the impact of the decoded ring return to the original information in the parity check matrix, to ensure the quality of the original information as possible to spread to the node can spread, thereby enhancing the performance of the LDPC decoding.

Aiming at the BP algorithm of LDPC in every iteration process that all bits and check information must be update, there is large amount of calculation and decoding inefficient problems. The article proposes a kind of improved BP decoding algorithm. According to the improved BP decoding algorithm, a high speed parallel decoder is designed, and a high speed parallel decoder is studied in Gaussian channel of error correction performance.

II. LDPC CODE

LDPC code is a thin linearity group code for sparse checking matrix. The same as all linearity group codes, LDPC code , with K information bit and N code length, can be determined by computing matrix H of (N-K)*N. Every code word "u" can be obtained by HuT=0, where H is a thin matrix constructed by certain means. Just as this thin capability, it realizes encoding and decoding [18] without much complexity. LDPC code can be illustrated by bipartite graph, which includes bit node muster and checkout node muster. The relationship between bit node and checkout node is corresponding to "1" in H. Binary vector u = [u1 , u2 … uN], only if all the constraint equations of checkout nodes satisfies that u is a code word. In the present work, LDPC code with N = 8, 1/2 code rate is illustrated. Assuming that checkout matrix of the code is given by *Equation 1*.

$$H = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 \end{bmatrix} \quad (1)$$

The bipartite graph is given in Figure 1 according to *H*. Bit node *u* is on the left side, which represents bit location after coding and accords with corresponding arrange in *H*. Checkout node is at starboard, which is the checkout equation and is constituted by decoding bit and accords with corresponding row in *H*. Bipartite graph of LDPC codes is shown in Figure 1. According to the figure 1, the link lines denote left one bit which appears in dextral one checkout equation and accords with "1" in *H*. The number of "1" is called as the checkout node degree dc in rows of *H*, and the bit node degree dv in arranges of *H* respectively, which are separately corresponding with the limbic numbers and then connect checkout codes and bit codes. LDPC code is a regular code if dc and dv are the constants, or else is a non-regular one [19]. The example in equation 1 is a regular code.

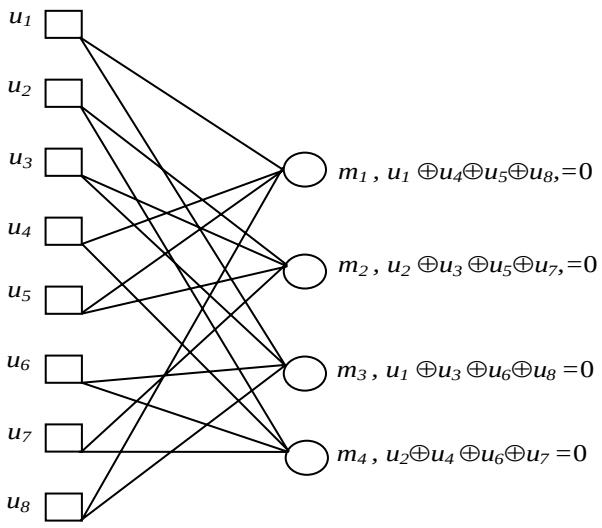

Figure 1. Bipartite graph of LDPC codes

III. LDPC CODE BP CODING ALGORITHMS

Traditional BP coding can be divided into two steps of each iterative decoding: checkout node and checks node. All checkout nodes can obtain information from the check node nearby, by disposing, and then return to check node nearby, while all check nodes are carried through the same process. All the used information can be finally obtained by check node to judge. During LDPC code is carried through coding, every checkout (or check) node may be regarded as a processor. All disposals of checkout or check nodes may process at the same time. Due to the parallel structure, the encoder of high-speed LDPC code can be constructed. Convenient for describing, all symbolic meanings involved in BP coding algorithms are explained.

$N(m)$ denotes all bit nodes aggregate which is connected with checkout point, namely $N(m) = \{x_n : Hmn = 1\}$, $N(m) \backslash m$ represents that $M(n)$ aggregate except S_m bit. $M(n) = \{S_m : Hmn = 1\}$, $M(n) \backslash m$ denotes aggregate except S_m checkout node.

q_{mn}^x is the probability of bit $x_n = x$. The bit is achieved by checkout point aggregate $M(n) \backslash m$ message and receiving signals. Therefore $x \in \{0,1\}$, $q_{mn}^0 + q_{mn}^1 = 1$, the information about q_{mn}^x is considered, where bit *n* can be transmited to checkout node *m*.

r_{mn}^x denotes when bit $x_n = x$ and bit probability $q_{mn'}(n' \in M(n) \backslash m)$ in $M(n) \backslash m$, the established probability of checkout node m corresponds to the

checkout equation. r_{mn}^{x} can be considered as that transfers message from *m* to n.

The whole BP algorithms: *m, n* perform the following steps when $Hmn = 1$.

(1)Initialization

If $P_n^0 = P(x_n = 0)$ (priori probability $x_n = 0$),

$$P(x_n = 1) = 1 - P_n^0,$$

then $q_{mn}^0 = P_n^0, q_{mn}^1 = P_n^1$

(2)Checkout node renew, commanded

$$\delta q_{mn} = q_{mn}^0 - q_{mn}^1, \delta r_{mn} = \prod_{n' \in N(m) \backslash n} \delta q_{mn'},$$

$$r_{mn}^0 = 0.5(1 + \delta r_{mn}), r_{mn}^1 = 0.5(1 - \delta r_{mn})$$

(3)Bit renew

$$q_{mn}^0 = \alpha_{mn} P_n^0 \prod_{m' \in M(n) \backslash m} r_{mn'}^0,$$

$$q_{mn}^1 = \alpha_{mn} P_n^1 \sum_{m' \in M(n) \backslash m} r_{mn'}^1$$

thereinto select α_{mn} ,bring $q_{mn}^0 + q_{mn}^1 = 1$.

(4)Renew false posteriori probability q_n^0 and q_n^1.

$$q_n^0 = \alpha_n P_n^0 \prod_{m \in M(n)} r_{mn}^0, q_n^1 = \alpha_n P_n^1 \prod_{m \in M(n)} r_{mn}^0$$

Thereinto select α_n , bring $q_n^0 + q_n^1 = 1$.

(5)Bit judge

If $q_n^0 > 0.5$,judge α_n =0; else, judge α_n =1, n=1, 2, …, N. If HTX=0 or iterative times reach the largest number of iterations, then stop. X is used as coding, else return to Step (2).

IV. IMPROVED BP CODE ALGORITHMS

The two shortcomings of BP algorithms are great computation quantity and low coding efficiency, although the capability of BP algorithms is good. In every iterative process. An each computation quantity is therefore identical. With the increasing iterative times, the quantity of corrective bits reduces gradually during each iterative process. The improved BP coding algorithms with low complexity and high efficiency is presented in this paper. The bit reliability is judged by both nonregular checkout count and combining the difference of bit node pseudo-posterior probability. Based on above-mentioned judge rule, the ahead iterative calculation is terminated by partial nodes. The implementation procedure is shown by:

(1)Initialization

If $P_n^0 = P(x_n = 0)$ (priori probability $x_n = 0$), $P(x_n = 1) = 1 - P_n^0$,则

$$q_{mn}^0 = P_n^0, q_{mn}^1 = P_n^1, \varphi = \phi$$

(2)Compute each bit lawless checkout number $U(l)$.

$$U^T \times [(H \times r)^T] \bmod 2 \times H = Z^T \times H$$

(3)Checkout node renew,order

$$\delta q_{mn} = q_{mn}^0 - q_{mn}^1,$$

$$\delta r_{mn} = \prod_{n' \in N(m) \backslash n \text{且} n' \notin \varphi} \delta q_{mn'},$$

$$r_{mn}^0 = 0.5(1 + \delta r_{mn}), r_{mn}^1 = 0.5(1 - \delta r_{mn})$$

(4)Bit renew

$$q_{mn}^0 = \alpha_{mn} P_n^0 \prod_{m' \in M(n) \backslash m} r_{mn'}^0,$$

$$q_{mn}^1 = \alpha_{mn} P_n^1 \sum_{m' \in M(n) \backslash m} r_{mn'}^1$$

thereinto select α_{mn} ,bring $q_{mn}^0 + q_{mn}^1 = 1$

(5)Renew false posteriori probability q_n^0 and q_n^1

$$q_n^0 = \alpha_n P_n^0 \prod_{m \in M(n)} r_{mn}^0, q_n^1 = \alpha_n P_n^1 \prod_{m \in M(n)} r_{mn}^0$$

(6)Compute received *l* reliable message provided by posteriori probability: $S(l) = \left| q_n^0 - q_n^1 \right|$.

(7)Note no necessary for renewing *l* during next process, *l* satisfy $U(l) > 0, S(l) > M$,then put *l* into aggregation φ.

(8)Bit judge

If $q_n^0 > 0.5$,judge α_n =0, else, judge α_n =1,n=1, 2 ,…, N. If H^TX=0 or iterative times reach the largest number of iterations, the calculation is finished, *X* is used as coding, or else return to Step (2).

V. DESIGN OF HIGH-SPEED PARALLEL ENCODER BASED ON IMPROVED BP CODE

Checkout nodes and check nodes can not run simultaneity. The node in encoder is the basic units of running coding calculation, which is mainly account for logic resource of encoder. Two kinds of calculation unit can not be effectively combined because the checkout nodes deal with comparative algorithms, whereas the check nodes deal mostly with addition algorithms. In this way, if Checkout nodes and Check nodes are run simultaneity, which led to the improvement in efficiency of logic resource. According to above-mentioned analysis, the novel encoder realization model is proposed as shown in Figure 2.

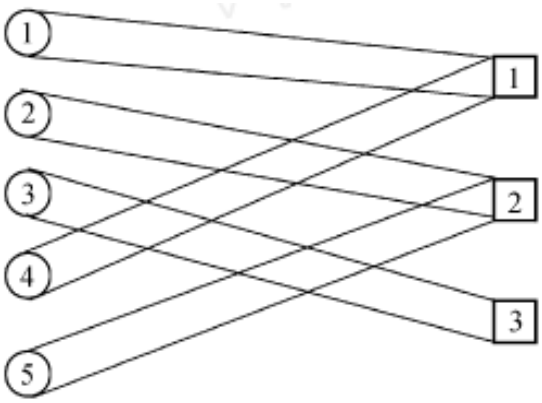

Figure 2. Model of improved decoder

Compared with uniline connects between check nodes and checkout nodes in traditional encoder, the check nodes and checkout nodes in the present model are connected through bifilar, which is significant and unique difference. The middle result of code A is treated and stored through one sideline, and middle result of code B is treated and stored by other sideline. The confidence of code B is updated by checkout nodes when confidence of code A is calculated by check nodes. All nodes are always to work due to alternate coding of two codes, which results in that the calculation efficiency of the present encoder is increased to double compared with tradition model. The double increase in storing-demand of the present encoder is feint disadvantage because the logic resource is reduced to half under comparative quantity of calculation based on the calculation efficiency of the projects of two encoders.

For LDPC code to parallel coding, *H* matrix is established in order to be fit for parallel-coding operation. Constructed LDPC code suits to parallel-encoder and realizes coding by limiting checkout matrix when the matrix constructs LDPC code. So that *H* matrix of LDPC code is designed as [22-24]:

$$H=\begin{bmatrix} I(p_{0,0}) & I(p_{0,1}) & I(p_{0,2}) & \cdots & I(p_{0,n-1}) \\ I(p_{1,0}) & I(p_{1,1}) & I(p_{1,2}) & \cdots & I(p_{1,n-1}) \\ I(p_{2,0}) & I(p_{2,1}) & I(p_{2,2}) & \cdots & I(p_{2,n-1}) \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ I(p_{m-2,0}) & I(p_{m-2,1}) & I(p_{m-2,2}) & \cdots & I(p_{m-2,n-1}) \\ I(p_{m-1,0}) & I(p_{m-1,1}) & I(p_{m-1,2}) & \cdots & I(p_{m-1,n-1}) \end{bmatrix} \quad (2)$$

where $I(p_{i,j})$ denotes p×p unit matrix whose circle shift offset is $p_{i,j}$. if offset $p_{i,j}$ is positive infinitude, then it denotes a full zero-matrix. LDPC code of such structure is called Block LDPC code.

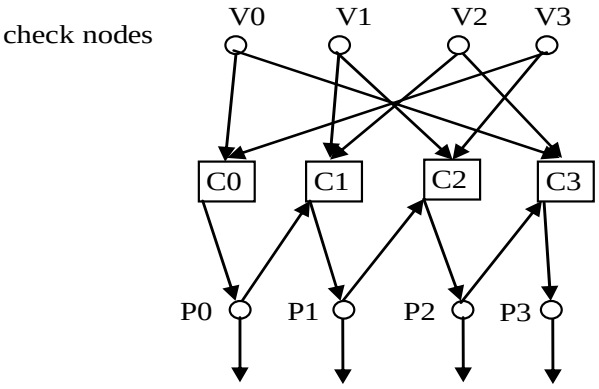

Figure 3. Structure based on iterative decoding algorithm

Paralleling-unit of LDPC code is divided into Check Node and Check Node coding by iterative means. The structure based on the iterative decoding algorithms is shown in Figure 3. Checkout Node is checked by Check Node and then the checked result as the initialization of next step is inputted. The iterative process proceeds when the iterative times are achieved.

Checkout nodes and check nodes can not run simultaneity during decoding algorithms. Storing space of the present encoder is expanded to double times. The original data of Check Node and middle calculated results are stored by RAMc. The original data of Checkout Node and middle calculated results are stored by RAMv. RAMc and RAMv are connected by EMS mapping circuit in order to reduce complex degree of the present encoder and to avoid possibility of odd point overturning. The data of mapped unit in RAMv are changed as the data in RAMc are changed, and the structure of parallel-encoder is given in Figure 4.

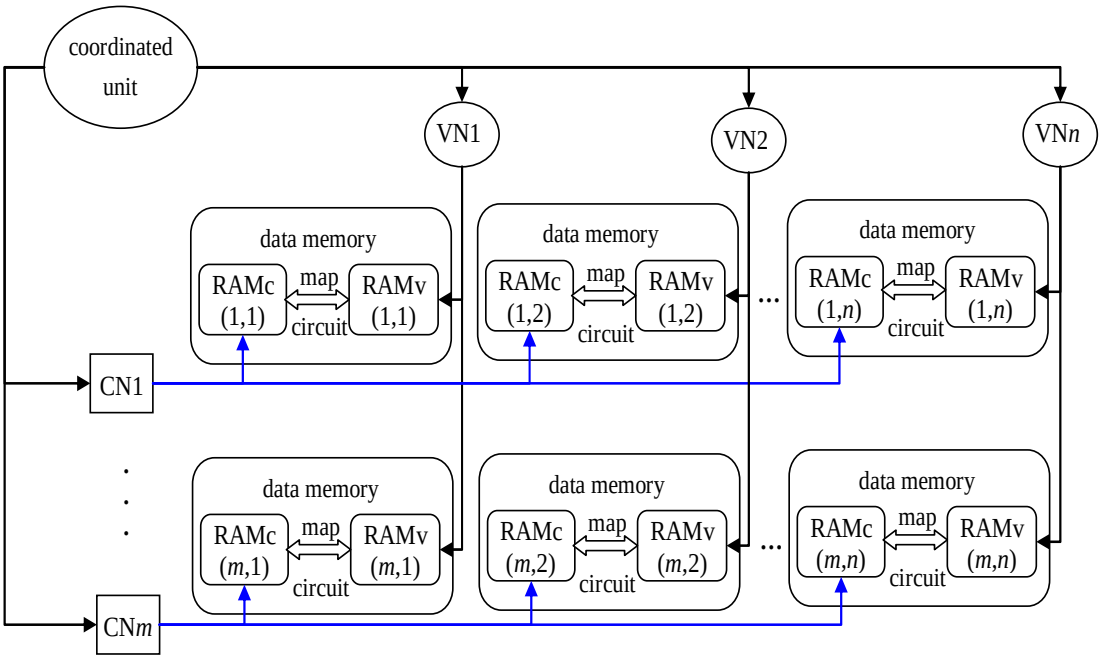

Figure 4. The structure of parallel decoder

Each iterative decoding is given as follows:

(1) The prior probability of given channel fore-setup message bit is provided by Harmonious unit initialization, RAMv and RAMc, and two laters are correlative to Communication Node and Check Node.

(2) The posterior probability of Checkout Node is given through confidence transmitting algorithms using prior probability of Communication Node.

(3) The posterior probability of Communication Node is calculated by Posterior probability of Check Node.

(4) Every bit in code is directly judged after finish of calculation.

Communication Node and Check Node can accomplish in parallel, although Parallel-encoder needs add RAM module amount. The storing space of the present encoder is enhanced to double, which enhances LDPC code applications in diversified fields.

VI. RESEARCH ON SIMULATION CAPABILITY OF HIGH-SPEED PARALLEL LDPC ENCODER

Simulation System diagram is presented in Figure 5. In the formation of small satellite spread spectrum communication system, using BPSK modulation, spread spectrum Direct Sequence Spread Spectrum, spread spectrum code using GOLD code, channel model with Gaussian channel. Select a code length of 512,256, and 64, and a code rate of 1/2 non-regular LDPC for system simulation.The most of LDPC coding iterative number is fifty if channel SNR is *Eb/No*=1.6dB.

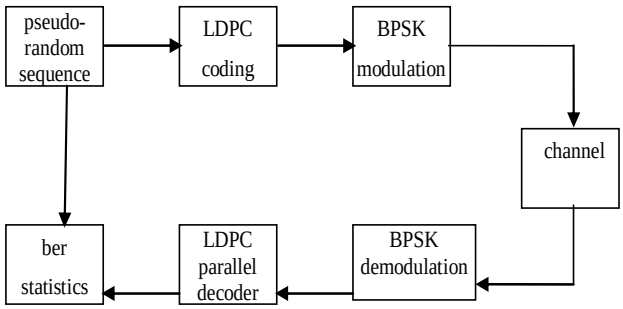

Figure 5. System simulation diagram

Figure 6 and Figure 7 respectively show the calculation loads of each iteration process for traditional BP coding algorithms and improved BP coding algorithms in the text. The vertical coordination is normalization calculated load. The calculation load of each iteration process for improved BP coding algorithms in the text is obviously reduced as the iterative times increased.

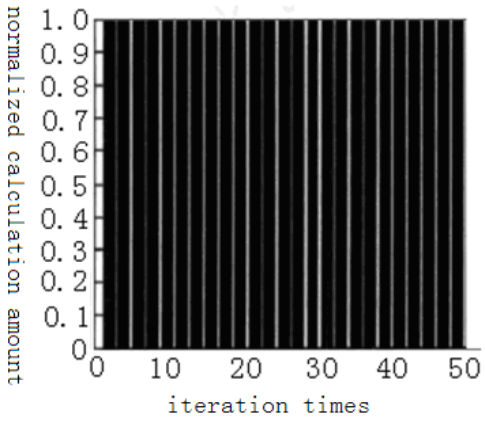

Figure 6. Calculation load of traditional BP algorithms each iteration process

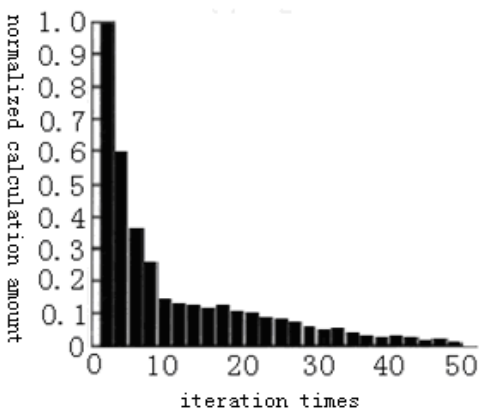

Figure 7. Calculation load of improved BP algorithms each iteration process

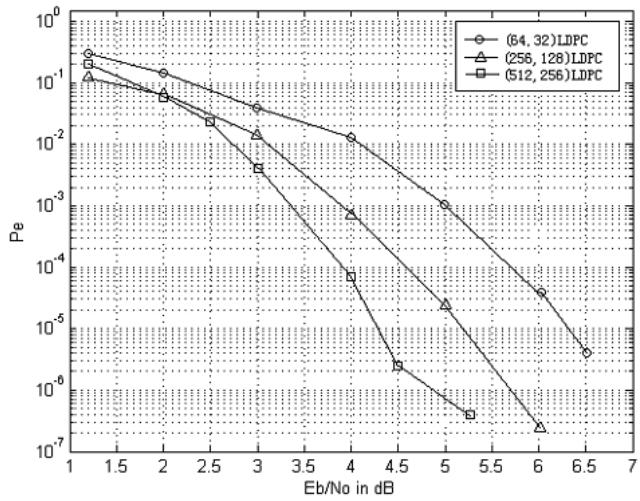

Figure 8. Performance Comparison of Different LDPC Codes Length

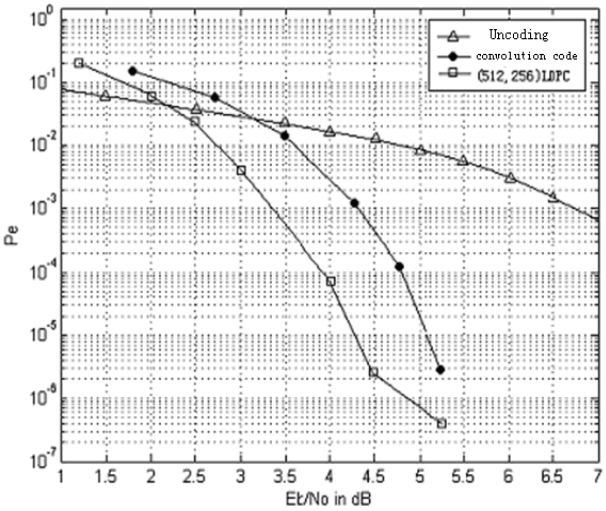

Figure 9. BER Comparisons between LDPC Code and Convolutional Code

The LDPC can be obtained by changing the value of the channel in the different values of the BER values. The simulation result is show in Figure 8.

From figure 8, we can see that based on LDPC parallel high-speed decoder of formation small satellite spread spectrum communication system can achieve good performance. The error correction performance of the 512 code length LDPC encoding is better than 256 code length LDPC encoding. The Bit Erroe Rate is 10-4 while the coding gain is 0.7dB,however this gain begins to decrease when Eb/No is greater than 4.5dB. This is because the irregular LDPC has low degree of variable node, to correct these low degrees variable node error is more difficute relative to high degree node.

Meanwhile, the spread spectrum communication system using (2,1,7) convolutional code encoding, and let its performance simulation results compared with LDPC , as shown in figure 9 to the comparison results.

From the simulation result of Fig 9:(1)The correct capability of(512,256)LDPC codeis better distinctively than (2, 1, 7) convolution code. When error rate is 10^{-5}, the plus is 0.9dB. But the plus begins to decrease, when Eb/No exceed 4.5dB.(2)When E_b/N_o exceed 2dB,with the increasing E_b/N_o, Error-coding Rate will be improved prominently.

In order to further examines the designed LDPC parallel decoder, we choose code length of 512, code rate for 1/2 of the LDPC code, to simulate the system error correction performance in the iteration limit of 2,5,10,50,100 respectively, the simulation results are shown in Figure 10.

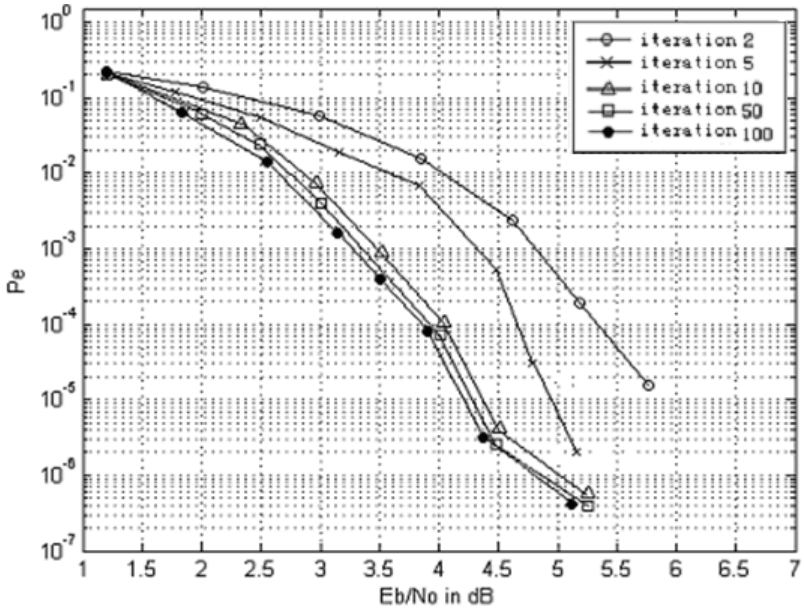

Figure 10 Performance Comparison of LDPC with Different Decoding Iterations

From figure 10, it can be concluded that decoding performance is the worst if the times of LDPC code iterations upper limit is two. With the times increasing of LDPC code iterations upper limit, the coding performance could be greatly improved.

VII Conclusion

To deal with the problem of great calculation load and low coding efficiency of traditional BP coding, the novel BP coding algorithm model is proposed. The new algorithm only updates the wrong bit information but does not update the highly reliable bit information. Based on the improved BP coding algorithm, a high-speed parallel encoder is designed. The error performance of the high-speed parallel encoder is studied under Gauss channel. Simulation results indicate that the improved BP coding algorithm is much more effective than the traditional one, which greatly reduces calculating load of each iteration and increases coding efficiency and convergence speed at the fewer cost of loss on error performance. The proposed high-speed parallel encoder, based on improved BP coding algorithm, has lower computational complexity and higher decoding speed.

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