Design and Experiment of SINS/GPS Integrated Navigation System

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***Abstract*—To meet the requirements of SINS/GPS integrated navigation system such as high accuracy, low power consumption and small size, an embedded navigation computer system based on DSP and FPGA was designed. At first, the overall structure of the navigation computer system was demonstrated. The navigation computer hardware module was consists of two sub modules i.e., the navigation information processing sub module, and the data acquisition and communication sub module. Secondly, Kalman integrated filter scheme was designed and then system software work flow was introduced. Finally, the prototype verified experiment was made. The experimental results showed that the system can effectively accomplish the missions of navigation sensor data acquisition, real-time navigation solution, running of Kalman filter algorithm and peripheral equipment instruction fetch. The requirements of the navigation computer for SINS/GPS integrated navigation system can be totally met.**

***Index Terms*—integrated navigation, embedded computer, SINS, GPS, Kalman filter**

I. INTRODUCTION

The SING/GPS integrated navigation system [1], [2] consists of strapdown inertial navigation system (SINS) [3] and global positioning system (GPS) [4]. The navigation computer is an integrated navigation system serves two functions (a) to complete a large number of real-time data processing operations, e.g., inertial measurement unit (IMU) raw data preprocessing, GPS receiver message preprocessing, inertial navigation solution and integrated filtering operation; (b) to complete the task of data communication with external navigation sensors and navigation application equipments, e.g., acquisition of raw data of gyroscope, accelerometer and other inertial sensors and GPS receiver message, command reading of navigation application equipments and output of the navigation results[5], [6].

Traditional navigation computers are mostly based on PC104 architecture [7] and have some shortcomings as follows. They usually have larger volume, higher power consumption and complex operating system. There are always difficulties in hardware maintaining. The operational performances of a traditional navigation computer are limited to the CPU dominant frequency and the real-time performance is relatively lower. Thus, the traditional navigation computers are not suitable for the integrated navigation system [8].

In this work, an embedded integrated navigation computer with digital signal processor (DSP) and field programmable gate array (FPGA) was designed as the core architecture of an integrated navigation computer in order to reach the performances of high real-time, low power consumption and small volume. The navigation computer, IMU and GPS compose the prototype platform of a SINS/GPS integrated navigation system. A Kalman filter [9], [10] for GPS speed and position measurement was designed according to the characteristics of the SINS/GPS integrated navigation system. The navigation accuracy of integrated navigation system cannot be guaranteed during GPS outages. Hence, the intelligent switch between integrated navigation mode and pure inertial navigation mode was designed in the working mode of the system to effectively avoid the above-mentioned disadvantage.

II. DESIGN OF NAVIGATION COMPUTER HARDWARE

Navigation computer needs to complete navigation sensor data acquisition, real-time navigation solution, navigation results output, etc. According to the functions,

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the navigation computer system designed in this work consists of two sub modules for navigation information processing and data acquisition and communication. The navigation information processing sub module, and the data acquisition and communication sub module. Figure 1 shows the navigation computer system structure.

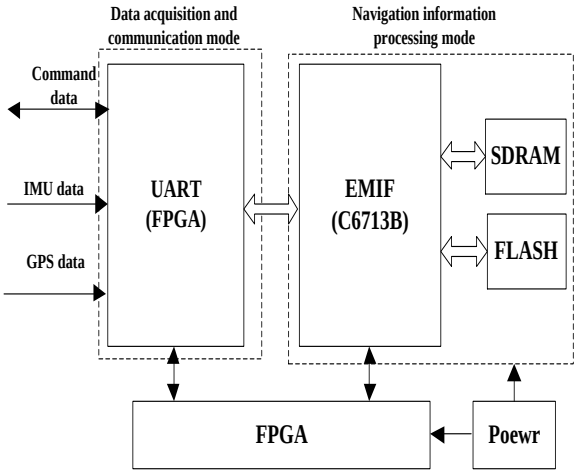

Figure 1. Note how the caption is centered in the column.

A. Design of navigation information processing module

The navigation data processing module is mainly composed of DSP, SDRAM, FLASH, clock circuit, bus driving circuit and FPGA-implemented logic control circuit. The DSP mainly completes the various navigation algorithms; the SDRAM is mainly used to expand the memory space required for system operation; the FLASH is mainly used to expand the external ROM and solidify the system program code; the main function of the clock circuit is to provide a stable clock reference for the navigation computer system; the bus driving circuit and the logic control circuit mainly coordinate the DSP chip to complete reading-writing of external memory data and I/O port.

Both strapdown algorithm and integrated filtering algorithm, which have high computational complexity and high requirements on real-time performance, involve a large number of matrix operations and finite impulse response (FIR) filters. The DSP is a new digital signal processor which can achieve real-time, fast and effective numerical operations. And DSP has integrated internal integrated FIR filters [11]. When selecting navigation information processor, this design takes into account the factors such as power consumption, volume and cost, while in order to meet the requirements on real-time navigation operations of the integrated navigation system, and finally uses TMS320C6713B (C6713B) chip of Texas Instruments (TI) as the core processor of the navigation computer.

Taking into account the factors such as power consumption, volume and cost, DSP was selected as the navigation information processor in this design. Further, in order to meet the requirements on real-time navigation operations of the integrated navigation system, TMS320C6713B (C6713B) chip of Texas Instruments (TI) was used as the core processor of the navigation computer.

Due to limited internal RAM memory space of the DSP chip, it is required to use an external SDRAM chip as the data memory of the DSP. HY57V561620BT-H chip of Hynix with the memory space of 256Mbit, an the operating temperature range of -55~+125 ℃, a the working voltage of 3.0~3.6V and a clock frequency of 133MHz was selected as the SDRAM chip to fully meet the data storage requirements of the navigation information processor. The memory space, operating temperature range, working voltage and clock frequency of the HY57V561620BT-H chip are 256 Mbit, -55 ~ +125 ℃, 3.0~3.6 V and 133 MHz, respectively. In this design, the SDRAM memory occupies the CE0 memory space of the DSP. The HY57V561620BT-H chip with chip select (CS) signal is connected with pin TEC0 of the DSP chip. The Bank address buses BA0 and BA1 of the chip are connected with the address signal lines A15 and A16 of C6713B, respectively. The address signal buses A0~A12 of HY57V561620BT-H are connected with the address signal lines A2~A12 of C6713B, respectively. And the data signal lines of HY57V561620BT-H are respectively connected with the data signal lines D0~D15 of C6713B, respectively.

Because the internal ROM memory space of the C6713B chip is limited and cannot meet the program storage requirements of the navigation system, it is necessary to expand the external FLASH memory to store navigation programs and initialization data. After the system is powered on, the DSP runs the secondary bootloader to load programs and initialization data stored in the FLASH into the RAM in the DSP chip to make program running [12]. SST39VF800A chip of SST with a memory space of 8 Mbit, a working voltage of 3.0~3.6 V, a running current of 20mA and a standby current of 3 uA was selected as the FLASH chip to meet the demands of the navigation information processor. Figure 2 shows the interface design of the DSP chip and the peripheral storage chip.

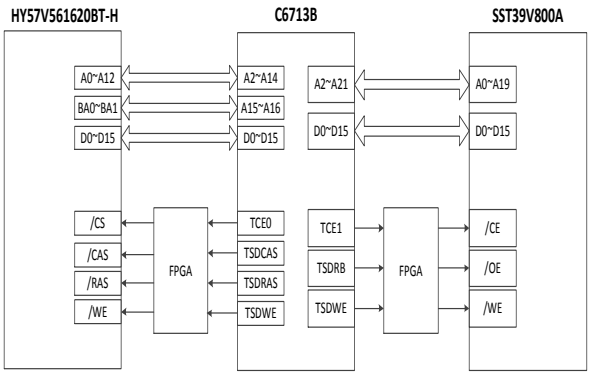

Figure 2. Design of peripheral storage chip interface

In this design, the FLASH memory occupies the CE1 memory space of the DSP, the SST39VF800A chip which with chip select (CS) signal is connected with TEC1 of the DSP chip. The address signal lines A0~A19 are connected with A2~A21 of C6713B, respectively, and

the data signal lines D0~D15 are connected with D0~D15 of C6713B., respectively.

The address signal lines A0~A19 and the data signal lines D0~D15 of the FLASH chip are correspondingly connected with A2~A21 and D0~D15 of C6713B, respectively.

The chips with chip select (CS) signal and read-write signal of the peripheral storage devices are accessed to the FPGA and then connected with the DSP. It can simplify the circuit diagram PCB layout and the circuit system debugging, as well as improve the system stability.

B. Design of data acquisition and communication module

The data acquisition and communication module mainly completes external navigation sensor information acquisition, upper computer command reception and navigation results output. Integrated navigation system used Universal Asynchronous Receiver/Transmitter (UART) as the data communication interface of the navigation computer with external devices to meet the RS-232 and RS-422/485 standards. Since the DSP chip is not integrated the UART function internally, it is required to expand multi-channel UART externally. This design uses FPGA, MAX3232 and MAX3490 chips supplemented by a few other circuits for the data acquisition and communication sub module. Thus, FPGA, MAX3232 and MAX3490 chips supplemented by a few other circuits were used in this design for the data acquisition and communication sub module. This design not only makes the whole system more compact, stable and reliable, but also allows the flexibility to set the size of the FIFO memory and can meet the seamless connection between different navigation sensors and the navigation computer system [13]. By this design, the whole system could be more compact, stable and reliable; the size of the FIFO memory can be set as required; the seamless connection between different navigation sensors and the navigation computer system could be realized. Figure 3 shows the structure of the data acquisition and communication module.

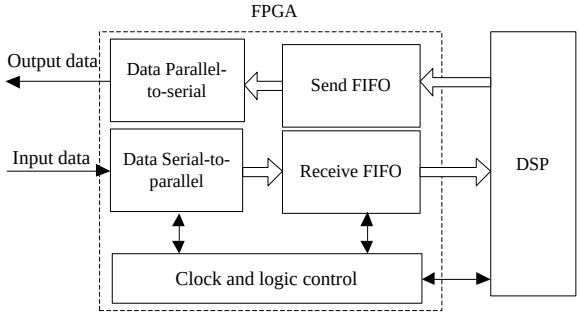

Figure 3. Structure of the data acquisition and communication module

III. SYSEM SOFTWARE DESIGN

In this design, the SINS/GPS integrated navigation system adopts the position and speed integrated mode. The filter uses the SINS error equation as the state equation. The position and speed navigation information differences between the SINS and GPS as the filter measurement information, was used to correct the SINS state vectors after Kalman filtering to improve the navigation accuracy. The simple integrated mode introduces the GPS speed and position information and improves the redundancy of the navigation system. The system is capable of intelligent switching between the SINS working mode and the SINS/GPS integrated working during GPS outages for guarantying navigation accuracy and facilitating engineering implementation.

A. Kalman filter design

The linear state equation of the system is as follows:

$$\dot{X}(t) = F(t)X(t) + G(t)W(t) \tag{1}$$

East-north-up geographic coordinate is applied as navigation coordinate in the system. Since the vertical channel of the SINS system is unstable and has little compensation effect for the system error, the vertical speed and position vectors are negligible in the state vectors of the filter. The state vectors of the filter are 12-dimensional. The state vector model of the system is as follows:

$$X(t) = [\delta V_E \ \ \delta V_N \ \ \phi_E \ \ \phi_N \ \ \phi_U \ \delta L \ \ \delta\lambda \ \ \nabla_{bx} \nabla_{by} \ \ \varepsilon_{bx} \ \ \varepsilon_{by} \ \ \varepsilon_{bz} \ ] \tag{2}$$

where, δV_E, δV_N are the east and north speed errors of the navigation system, respectively; ϕ_E, ϕ_N, ϕ_U are the platform misalignment angles of the navigation system, respectively; δL、$\delta\lambda$ are the latitude and longitude errors of the navigation system, respectively; ε_b is the gyro drift; ∇_b is the accelerometer bias.

The noise vector of the system:

$$W(t) = [\omega_{gx} \ \omega_{gy} \ \ \omega_{gz} \ \ \omega_{rx} \ \omega_{ry} \ \ \omega_{rz} \ \ \omega_{ax} \ \omega_{ay} \ \ \omega_{az}]^{\mathrm{T}} \tag{3}$$

where, ω_g is the random white noise drift of the gyroscope; ω_r is the first order Markov process driving white noise of the gyroscope; ω_a is the random white noise drift of the accelerometer.

The noise variance matrix of the system $Q(t)$:

$$Q(t) = \mathrm{diag}[\sigma_{gx}^2 \ \ \sigma_{gy}^2 \ \ \sigma_{gz}^2 \ \ 2\frac{\sigma_{\mathrm{rx}}^2}{T_{rx}} \ \ 2\frac{\sigma_{\mathrm{ry}}^2}{T_{ry}} \ \ 2\frac{\sigma_{\mathrm{rz}}^2}{T_{rz}} \ \ \sigma_{\mathrm{ax}}^2 \ \ \sigma_{\mathrm{ay}}^2 \ \ \sigma_{\mathrm{az}}^2 \ ] \tag{4}$$

where, $\sigma_{gx}^2, \sigma_{gy}^2, \sigma_{gz}^2$ are the random white noise drift variances of the gyroscope; $2\frac{\sigma_{\mathrm{rx}}^2}{T_{rx}}$, $2\frac{\sigma_{\mathrm{ry}}^2}{T_{ry}}$, $2\frac{\sigma_{\mathrm{rz}}^2}{T_{rz}}$ are the first order Markov process driving white noise variances of the gyroscope; σ_{ax}^2, σ_{ay}^2, σ_{az}^2 are the random white noise drift variances of the accelerometer.

The measurement equation of the system:

$$Z(t) = \begin{bmatrix} V_{ie} - V_{ge} \\ V_{in} - V_{gn} \\ (\lambda_i - \lambda_e)R_N \cos L \\ (L_i - L_e)\ \mathrm{R}_M \end{bmatrix} = HX(t) + V(t) \tag{5}$$

where, V_{ie}, V_{in} are respectively east and north speed output from the SINS; V_{ge}, V_{gn} are east and north speed outputs from the GPS receiver, respectively; λ_i, L_i are longitude and latitude position outputs from the SINS, respectively; λ_g, L_g are longitude and latitude position

outputs from the GPS receiver, respectively; R_N, R_M are the radius of curvature in prime vertical and meridian of the location of the SINS/GPS integrated navigation system, respectively.

The measurement noise vector:

$$R(t) = \mathrm{diag}[\sigma^2_{ve}\ \sigma^2_{vn}\ \sigma^2_{\lambda}\ \sigma^2_{L}] \quad (6)$$

where, $\sigma^2_{ve}, \sigma^2_{vn}$ are the east and north speed measurement error variances, respectively; $\sigma^2_{\lambda}, \sigma^2_{L}$ are the longitude and latitude position measurement error variances, respectively.

After discretization of the state equation (1) and measurement equation (5) of the system, the random linear discrete system Kalman filter is used to update recursively, and the data output from the filter are used to correct navigation parameters from the SINS to obtain the navigation results. Figure 4 shows the Klaman filtering algorithm [14].

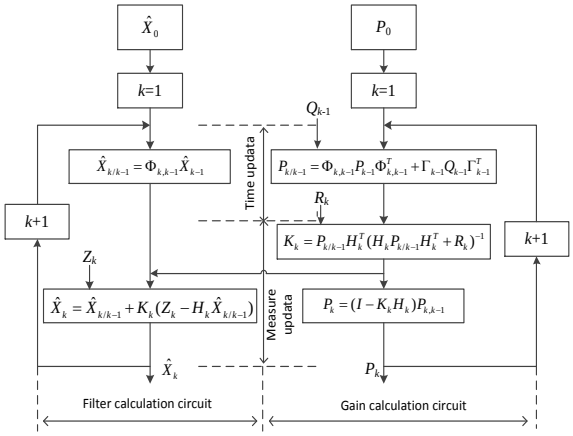

Figure 4. Discrete Kalman filter flow chart

B. System software workflow

Initial strapdown algorithm and integrated navigation algorithm are included in the system algorithm. Initial alignment of inertial navigation system algorithm uses self-alignment algorithm, which is divided into coarse alignment and extractive alignment [15]. Solidification algorithm is proposed to complete coarse alignment, extractive alignment using the compass method and the method of least squares to complete time-varying parameters. Strapdown attitude updating tactics is quaternion algorithm. SINS/GPS integrated navigation system uses the speed, position combination. The system algorithm flow chart is shown in figure 5.

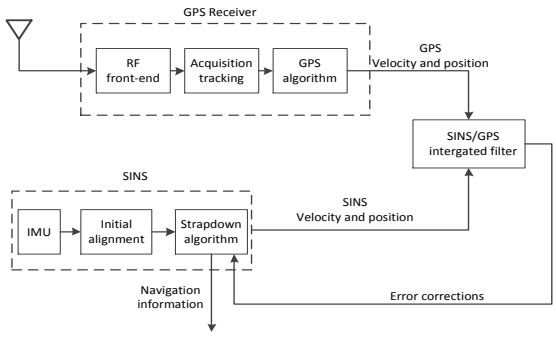

Figure 5. Flow chart of navigation system

Ⅳ. Experiment

In order to evaluate the performance of the SINS/GPS tightly integrated navigation system, the prototype land vehicle experiment was done. Inertial navigation system iXSea PHINS [16], [17] is selected as the attitude reference datum. The Novatel GPS receiver is selected as the positioning reference datum. Test of system land vehicle setup of the prototype and PHINS as the figure 6.

Figure 6. Navigation system photo for land vehicle

The figure 7-9 show that the attitude error of the land vehicle experiment. The land vehicle experiment shows that the alignment accuracy was 0.05 degree (1σ) for horizon attitude errors, and 0.12 degree (1σ) for heading errors.

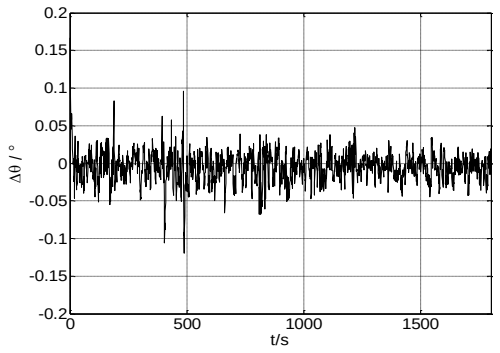

Figure 7. The curve of the pitch angle error

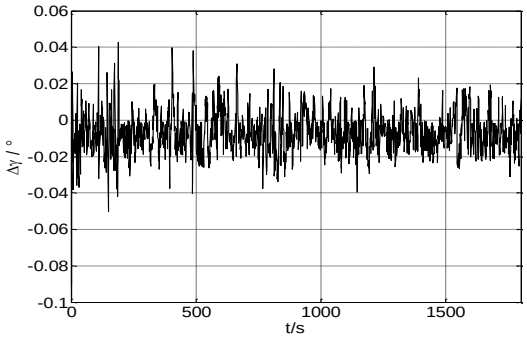

Figure 8. The curve of the roll angle error

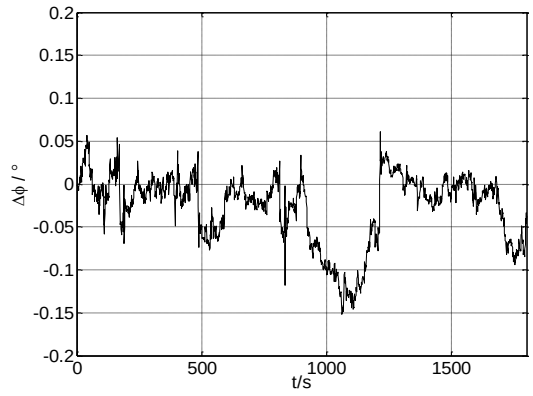

Figure 9. The curve of the heading angle error

The figure 10-11 show that the velocity error of the land vehicle experiment. The land vehicle experiment shows that the system accuracy was 0.03 m/s (1σ) for east velocity errors, and 0.06 m/s (1σ) for north velocity.

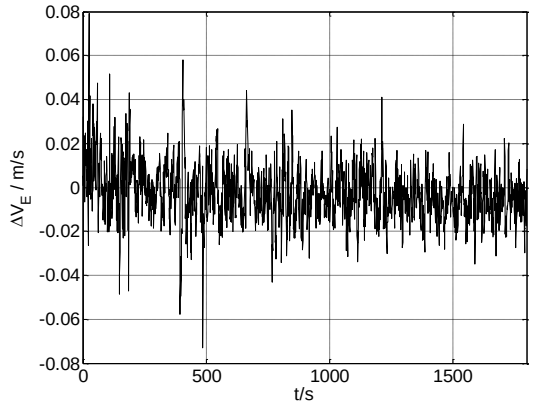

Figure 10. The curve of the east velocity error

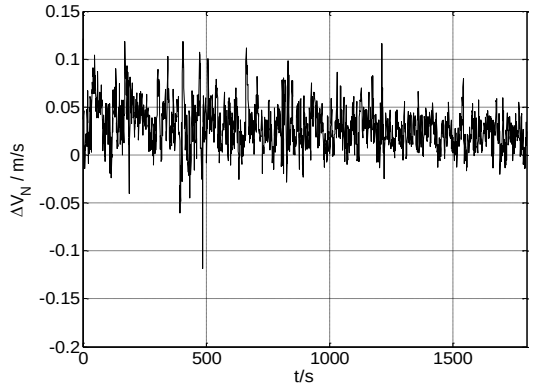

Figure 11. The curve of the north velocity error

The figure 12-13 show that the positioning error of the land vehicle experiment. The land vehicle experiment shows that the system accuracy was 1.2 m (1σ) for latitude positioning errors, and 1.1 m (1σ) for longitude positioning errors.

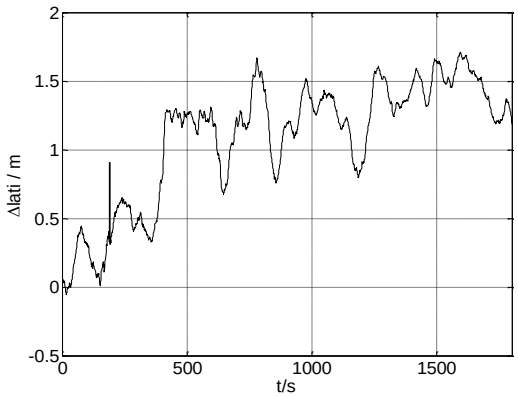

Figure 12. The curve of the latitude positioning error

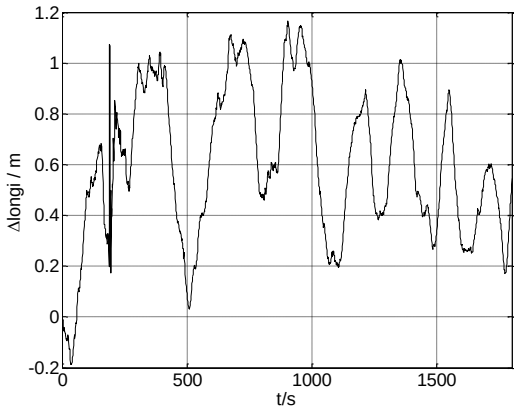

Figure 13. The curve of the longitude positioning error

Ⅴ. CONCLUSION

The paper presents a SINS/GPS integrated navigation computer system based on DSP and FPGA structure. The design realizes the integrated navigation system embedded design, the design concept fully embodies the real-time information processing and real-time control phase separation, information distributed parallel processing design thought, hardware and software combined to realize the system's target of high speed data acquisition and high speed information processing, satisfies the system's requirements of small volume, high precision, high real-time performance, low power consumption etc., which has practical engineering significance in the widely applications of integrated navigation system in low cost, low power consumption system areas.

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