A Reconfigurable FIR Filter System

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***Abstract*—Introduced a practical reconfigurable FIR filter system. According to the filter specialties, the filter coefficients are calculated by the computer. And the configured coefficients of the multistage FIR filter are downloaded to the chip. The filtering computing is completed by the FPGA. All these make virtual value of voltage and current more accurate and steady, so reseach on FIR filter Algorithms is the emphases and difficulty. The performance testing and application examples are given to verify this system.**

***Index Terms*—finite impulse response digital filter, reconfigurable coefficient, Data-sampling**

I. INTRODUCTION

In digital signal processing, digital filter occupies a very important role, which involves a very wide area, such as communication systems, system control, biomedical engineering, mechanical vibration, remote sensing, geological exploration, aerospace, power systems, fault detection, automated instruments. In order to improve immediacy and flexibility, now many universities and research institutes are using FPGA to realize FIR filters design. In an integrated view, multiplier structures and distributed algorithms are commonly used. A common problem of filter design is that filter coefficients cannot be adjusted dynamically according to the characteristics of signal that is to be filtered, which means that filters can only complete filtering work with singular characteristics, thus technological superiorities[1-3] of digital filters such as adjustability and flexibility cannot be fully brought into play. Based on this, this text designed an FPGA-USB2.0-computer FIR digital filter system, combining the rapidity of FPGA with the flexibility of computers organically through the USB2.0 bus to realize the acquisition[4-8], filtering and display of signals. And the filter coefficients can also be dynamically adjusted to adapt to different filtered signals.

The quality of digital filter has a great influence on related engineering and technical fields. A good digital filter will be effective in promoting technological transformation and subject development of many technical fields. Therefore, working on the principle of the digital filter, hardware structure and ways of implementation of research is quite meaningful.

With the development of programmable logic devices and EDA technologies[8-15], FPGA can meet the needs of miniaturization of electronic systems, low-power, high-reliability , and short development cycle, low software development investment, and lower and lower chip prices, therefore FPGA is more and more chosen by the market, especially applied in low-volume, multi-species products. And the FPGA devices are of hardware parallel organization, and the parallel iterative algorithm of digital filters is very suitable for FPGA to achieve. Nowadays, many universities and research institutes are using FPGA to implement FIR filters design. In general multiplier structures and distributed algorithms structure are commonly used.

II. FIR DIGITAL FILTERS

For FIR filters, the system unit impulse response h (n) is non-zero in a finite number of values n; System function H (z) is convergent at |z|>0, and it only has zero point while |z|>0; there are only zero points finite z-plane, and all poles are at z = 0(causal systems); And the structure is primarily non-recursive structure, and there is no output-to-input feedback[15-18].

Suppose the unit impulse response h (n) of FIR filters is an N-point sequence, 0≤n≤ N-1, and the filter system function is as follows:

$$H(z)=\sum_{n=0}^{N-1}h(n)z^{-n} \tag{1}$$

That is, it has (N-1)-fold pole at z = 0, and there are (N-1) zero points at any location of finite z plane.

Linear phase of FIR filter is very important. Because both the data transmission and image processing require a system with linear phase, while for FIR filter, the impulse response is finite, which may be made to strict linear phase.

If the unit impulse response h (n) of FIR filter is a real number, $0 \le n \le N-1$, and meets the following conditions:

even symmetry:

$$h(n)=h(N-1-n) \tag{2}$$

odd symmetry:

$$h(n)=-h(N-1-n) \tag{3}$$

In other words, the symmetric center $n=(N-1)/2$ which means this kind of FIR filters has a strict linear phase.

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When N is odd

$$H(z)=\sum_{n=0}^{\frac{N-1}{2}} h(n)\left[z^{-n}\pm z^{-(N-1-n)}\right]+h\left(\frac{N-1}{2}\right)z^{-\frac{N-1}{2}} \quad (4)$$

Of which, "+" in square brackets indicates h (n) is even symmetric, and "-" indicates h (n) was odd symmetry. When h (n) is odd symmetry, there must be h [(N-1) / 2] = 0 (see equation (3)). The flow graph of the direct structure of FIR filter with linear phase can be drawn from equation (4) when N is odd, shown in Figure 1.

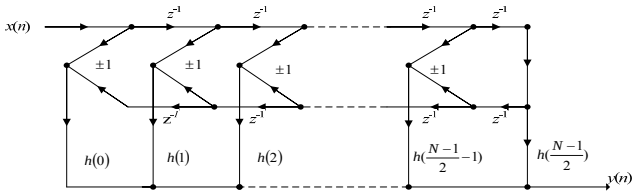


Fig. 1 The direct structure of the linear FIR filter (*N* is odd)

When N is even

$$H(z)=\sum_{n=0}^{(N/2)-1} h(n)\left[z^{-n}\pm z^{-(N-1-n)}\right] \quad (5)$$

Of which, "+" in square brackets indicates h (n) is even symmetric, and "-" indicates h(n) was odd symmetry. The flow graph of the direct structure of FIR filter with linear phase can be drawn from equation (5) when N is even, shown in Figure 2.

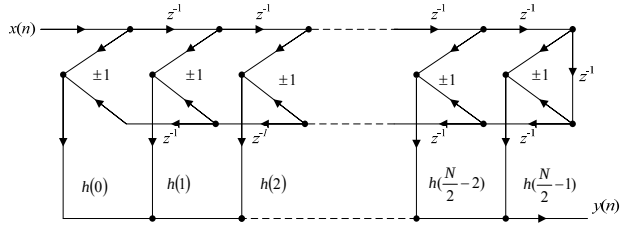


Fig. 2 The direct structure of the linear FIR filter (*N* is even)

III. DEFECT PROCESSING ALGORITHM

The system adopted in this paper is Quartus II, which provide a fully integrated designing environment with no confinement of the structure. It enables the easy design inputting, fast processing and device programming for a series of Altera products. The internationally used VHDL language is used to design most logic modules. VHDL(Very High Speed Integrated Circuit Hardware Description Language), has been the industry standard for the description, modeling and comprehension for the electronic system. It possess a strong language structure which make it possible to use the simple and clean code to design a complex controlling logic. It possess a multi-level designing description function .It is supportive of design library and capable of generating reusable components.

A. A/D Controlling Unit

The A/D controlling unit is FPGA design is used to provide the controlling signal for the A/D acquisition module. From the above introduction of A/D conversion circuit, we know that AD9203 needs a clock impulse for the pin CLK and controlling signals for pin STBY and 3-STATE.

The Quartus II 6.0 assigns the pins to the I/O ports of FPGA, and get to AD9203 through connectors. Some notices should be given to the assignment: first , try to avoid the assigning the special I/O to the input output pin of the designed circuit. Second is to take the practical PCB layout and alignment into account.

The specific configuration is as follows:

(1) assign the 4MHz clock generated by PLL to pin 131

(2)set the STBY low power, normal mode, and assign to pin 125.

(3) set the 3-STATE low power, normal output mode, and assign it to pin 127.

All the pins are set for output , and are linked to CLK, STBY, and 3-STATE in AD9203 through the connectors.

In order to extract the defect information, there needs to be a reference power level under which is thought to be the defect. The halogen light source fluctuations and the uneven thickness of the detected film can result in the amplitude change in the output signal. Therefore, the threshold should be able to adjust itself dynamically according to the CCD output signal. In this paper, the 75% of the power level of the former line CCD output signal is used as the threshold of the next line output signal, known as the pipeline designing method.

2048 data are sampled in each line under the sampling frequency of 4MHz. However, the accurate computing of the average of the 2048 data requires 2047 adders which can take up most of the FPGA resources, thus making it very difficult to perform in practice. The practical approach is to compute the average of the CCD output signal by sampling under the premise of accurate dynamic threshold. The specific approach is to compute the sum of the 64 sampled data uniformly spaced among the 2048 data. Then realize the function through VHDL programming with the threshold obtained as the 75% of the average.

Based on the above analysis, first of all we need to calculate the sum of the 64 data, the processing of which meets the demands of the unilateral lines. The design is quite simple due to the same operating times of the former level and the next level adders.

The specific approach is as follows: firstly uniformly extract the data according to the counter 2, then divide the data into 8 groups, each of which has 8 data. Through the eight-way data selector, the 8 data will be sent to the adder array to be computed to get the sum S1.By this analogy, we can easily obtain S_2, S_3, …, S_8. Then again S1, S_2, S_3, …, S_8 are sent to the adder array 2 to be computed

by the shift operation for the sum S of the 64 data. Shift S to the right by 6 bit, we get S_{ave}, we can also get the 50% and 25% of the S_{ave} by shifting the S_{ave} . to the right by 1 bit and 2bit respectively. The sum of the two is thus the threshold.

The simulation result of the dynamic threshold is shown in figure 3.The simulation period is 250ns. CLK is the clock impulse and ITRIIN is the trigger signal SH and ADDATA for the input data. The simulation is 0, 1, …, 1023, 0, 1…, 1023, all together 2048 data. The threshold is 383.625 through specific computation and the obtained threshold yuzhi in the simulation figure is 382. with an error as small as 0.4%.

B. The Simulation Result of the Overall Performance

The designing requirements for the system is to replace the traditional digital circuit chips and at the same time to complete a possible number of time temporal logic control, storage and transmission tasks. Using the macro function resources in the FPGA, we get the PLL、FIFO module; using the programmable logic resources and the self-designed VHDL code , we fulfill the function of counter, logic control and State machine, thus integrating all the digital parts in the FPGA which used to call for several separate chips. On account of this, it is much easier to design the hardware board and the operations of controlling, predicating, verification, extending and adjusting.

Realize and simulate the above function on Quartus II 6.0, and the results are shown in figure 4. The FPGA in use is the EP1C6Q240C8 of the Cyclone series by Altera Corporation. It has a logic cell utilization of 13%, pin utilization of 96% and memory cell utilization 71%.

The timing simulation results of the defect are shown in figure 5. The simulation results are all hexadecimal data. ADDATA is the input data. The defects are stored in FIFO after they are detected and bite-marked. FFFF is the line flag, 8005, 8006, 8007, 8008, 8009, 800A, 800B, 800C, 800D, 800E are the value stored in FIFO of the defects 005, 006, 007, 008, 009, 00A, 00B, 00C, 00D, 00E, and 0711 is the bottom position of the defect.

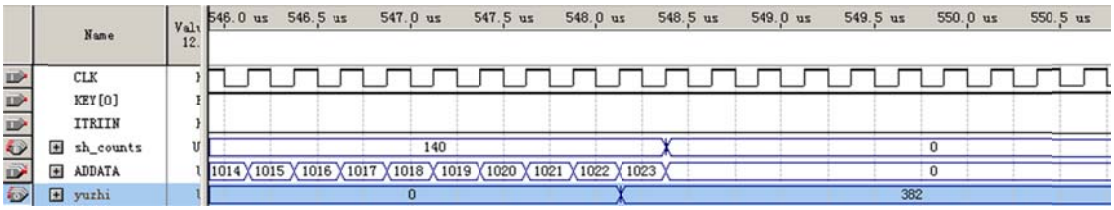


Fig. 3 Thresold simulation results

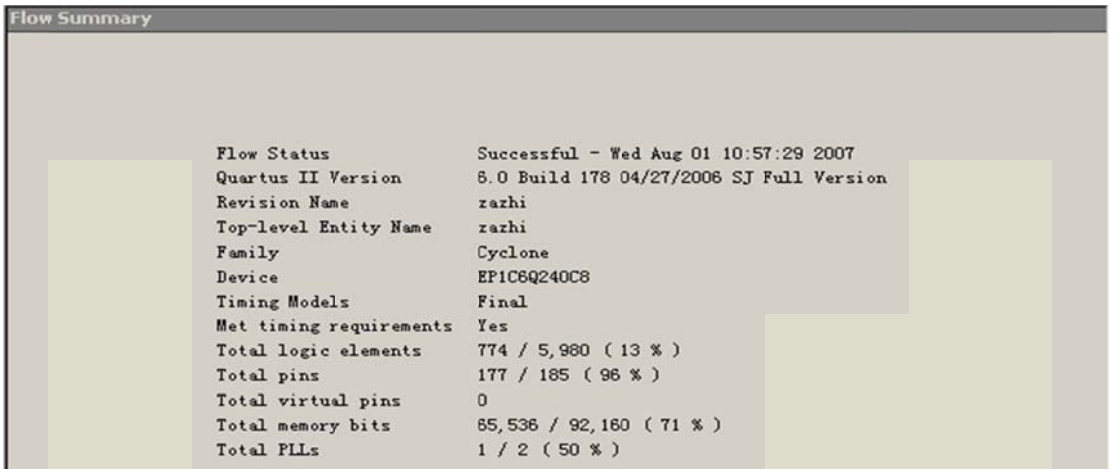


Fig. 4 Compiling results

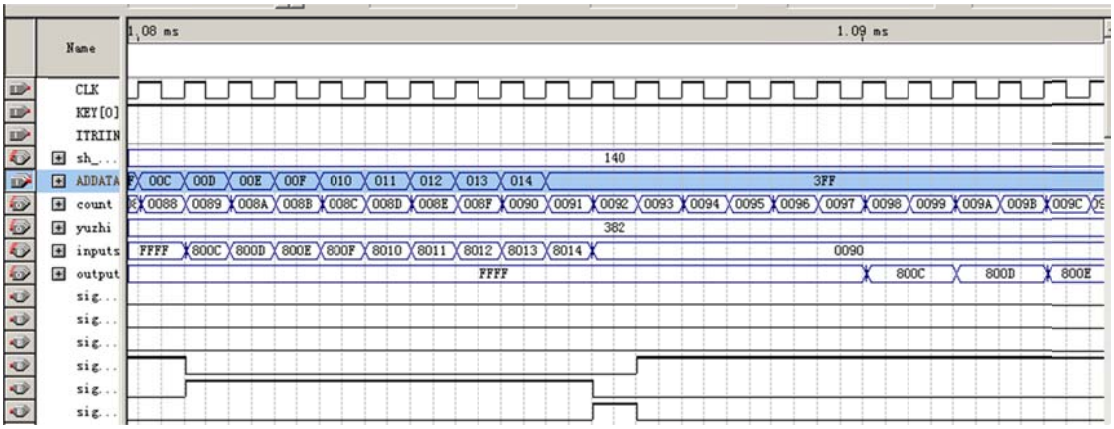


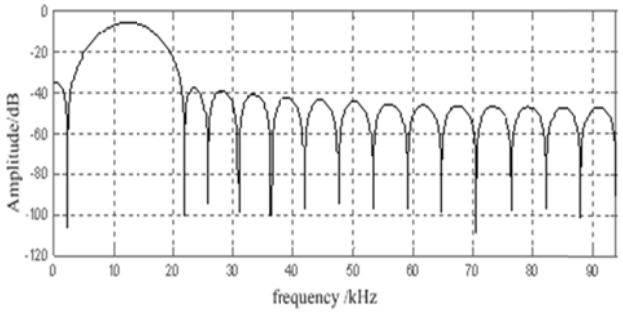
Fig.5 Simulation results

IV. FILTER PERFORMANCE VERIFICATION TEST

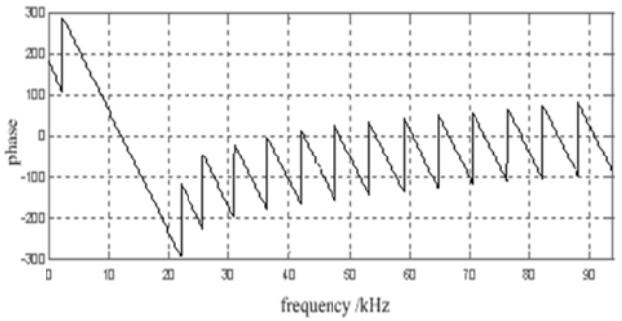
Using EP1C6Q240C8 chip of Altera's Cyclone series, we designed a 32-order FIR filter system of variable parameters, taking up 75% of on-chip logic cells and 71% of RAM after compilation. The filter uses the signal generator to generate a variety of input signals; the computer derives each order of factors according to given filter indicators and then configure the FPGA; FPGA and then uploads filtered data to the computer for displaying.

Specific experiments and analysis are as follows:

(1) Filter indicators: Window function is the Kaiser window, β=3.4, sampling frequency is 187.5kHz, cut-off frequency is 35kHz, and filter amplitude-frequency characteristic and phase-frequency characteristic are as shown in Figure 6; Input signal is a mixed-signal of 1.5kHz and 10kHz sine wave; oscilloscope signal is shown Figure 7 a); the filtered signal is shown Figure7 b). It can be seen from Figure 7 b) that since cut-off frequency of this low-pass filter is 35 kHz while the frequencies of mixed-signal of the input are all lower than 35 kHz, so the filtered signal waveform has not changed.

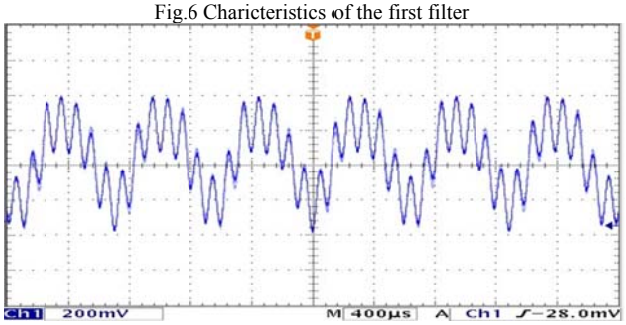


a) Amplitude-frequency characteristic

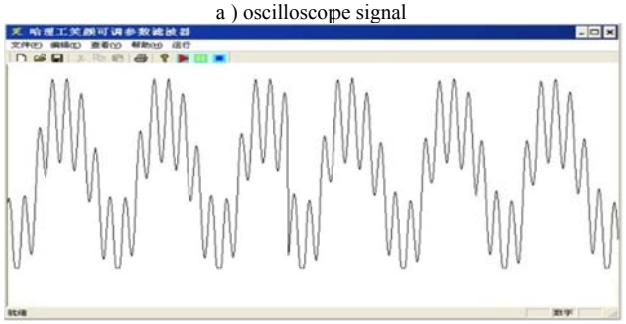


b) Phase-frequency characteristic

Fig.6 Charicteristics of the first filter



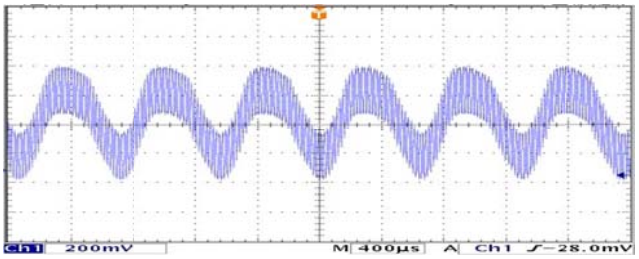
a) oscilloscope signal



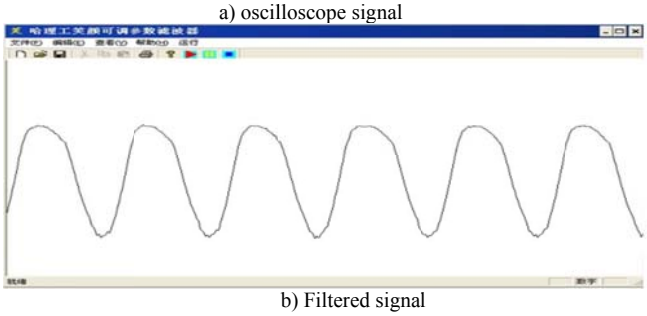
b) Filtered signal

Fig. 7 Results of the first filter experiment

(2) Filter indicators are the same as (1); Input signal is a mixed-signal of 1.5kHz and 50kHz sine wave, oscilloscope signal is shown in Figure 8 a) and the filtered signal is shown in Figure 8 b). The results can be seen that the low-pass filter filtered out 50kHz sine wave that is over cutoff frequency and it basically retained the 1.5kHz sine wave signal.



a) oscilloscope signal



b) Filtered signal

Fig. 8 Results of the second filter experiment

The filter performance verification test is shown above. Through experiments (1) and (2) we validated the low-pass filtering performance of the filter. The filter is with a good filtering effect.

V. The Practical Applications of Parameter-adjustable Filtering System

Through performance testing filtering performance of the filter is verified in this design. To verify the effect of the parameter-adjustable FIR filter system in practical applications, the parameter-adjustable FIR filter system is applied in CCD defects inspection system to be verified.

In CCD scanning defects detecting system, the electronic spectrum sampled by the CCD and converted time spectrum are shown in Figure 9, in which is the pulse cycle of signal.

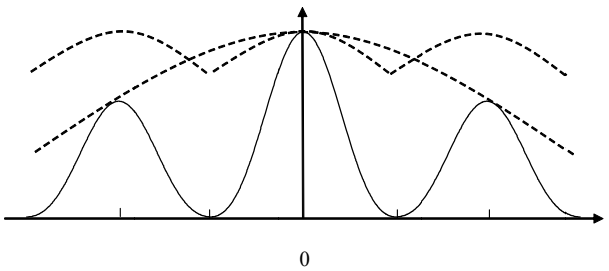


Fig. 9 Spatial and temporal spectrum of the image

From Figure 9 we can see that CCD sampling resulted in spectrum continuation. In order to prevent image spectral overlapping and to retain the image details, under ideal circumstances, CCD output signal should be filtered through a low-pass filter with a cut-off frequency of $\frac{\pi}{t_d}$. However, in practice, the high-frequency information of measured image has lost and bandwidth has become narrower through lens with a nature of low-pass filter. When the image frequency bandwidth is less than $\frac{2\pi}{t_d}$, filter with a cut-off frequency of $\frac{\pi}{t_d}$ cannot meet the system requirements. At this point, we want the filter to choose an appropriate cut-off frequency based on the actual spectrum of the image. Not only does it ensure the high-frequency information of useful signal of the image signal, but also it can filter different noises and obtain optimal system discrimination and signal signal-to-noise ratio. Therefore, for the detection system, designing a low-pass filter with adjustable parameters has important practical significance.

In addition, in material defect inspection system of linear array CCD, if the driving pulse frequency of CCD can be adjusted, the horizontal resolution and vertical resolution of the system can be adjusted according to actual requirement. But the problem is that if the driving pulse frequency of CCD is adjusted, to adjust the driving pulse frequency of CCD. The spectrum of measurement signal to the same target as well as the follow-up signal processing circuit will be changed. If we use a low-pass filter with a fixed cut-off frequency to filter the CCD sampled signal, the filtering effect is not good. Therefore, to ensure good filtering effect, the cut-off frequency of low-pass filter should also be adjustable.

VI. Conclusions

Along with the development of science and technology, digital filters, acting as a key technology of digital signal processing, directly impacts on the performances of many electronic systems. In this text, aiming at the requirements of real-time and flexibility of signal processing, based on FPGA as the core and on the basic theory of FIR digital filters, we designed an FPGA + USB2.0 + computer parameter-adjustable FIR filter system, combining the speed of FPGA and the flexibility of computer organically through USB2.0 bus.

Based on Modular design concept, the core module FPGA of this filtering system is divided into several functional modules and VHDL hardware description language is used for each module design. First, the designed modules are simulated through the timing simulation, and then low-pass filtering and band-pass filtering are verified through validation tests, which proved that the filtering effects are fine.

Acknowledgements

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