# The Hardware Design of Parameter-Adjustable FIR Filter System

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***Abstract*—This design using FPGA parallel architecture, high computing speed and high-speed reliability of USB2.0 interface, designed an FPGA + USB2.0 + computer FIR digital filter system, organically combining the speed of FPGA and flexibility of Computer through USB2.0 bus. The results demonstrated that the coefficients configuring of the system is easy, which can adjust the filter coefficients flexibly according to the actual demand, that it can effectively filter out the noise signals.**

***Index Terms*—finite impulse response digital filter, reconfigurable coefficient, hardware design**

## I. INTRODUCTION

In digital signal processing, digital filter occupies a very important role, which involves a very wide area, such as communication systems, system control, biomedical engineering, mechanical vibration, remote sensing, geological exploration, aerospace, power systems, fault detection, automated instruments. In order to improve immediacy and flexibility, now many universities and research institutes are using FPGA to realize FIR filters design. In an integrated view, multiplier structures and distributed algorithms are commonly used. A common problem of filter design is that filter coefficients cannot be adjusted dynamically according to the characteristics of signal that is to be filtered, which means that filters can only complete filtering work with singular characteristics, thus technological superiorities[1-3] of digital filters such as adjustability and flexibility cannot be fully brought into play. Based on this, this text designed an FPGA-USB2.0-computer FIR digital filter system, combining the rapidity of FPGA with the flexibility of computers organically through the USB2.0 bus to realize the acquisition[4,5], filtering and display of signals. And the filter coefficients can also be dynamically adjusted to adapt to different filtered signals.

## II. 2 THE HARDWARE DESIGN

This design using FPGA parallel architecture, high computing speed and high-speed reliability of USB2.0 interface, designed an FPGA + USB2.0 + computer FIR digital filter system, organically combining the speed of FPGA and flexibility of Computer through USB2.0 bus. Structured flowchart is shown in Figure 1. On one hand, the computer will download the calculated configuration parameters to FPGA through USB2.0 bus[6-10], in order to achieve FIR filters of different windows, different cut-off frequencies. On the other hand, 10-bit A/D converter is used for signal conversion. Digital signal is input to the FPGA device, FIR filtered in the FPGA devices, and the filtered data is transferred to computer through USB2.0 bus.

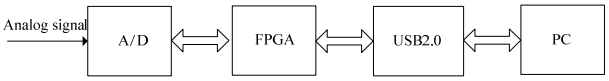


Fig. 1 Structure of the filter system

### A. A/D Conversion Module

A/D converter module main function is to digitize the analog signal, and then transfer it into the FPGA for digital signal processing. A/D converter module structure is shown in Figure 2. First analog signals are being conditioned, and then A/D converter, under the control of FPGA, will convert the conditioned signals to digital signals; power supply module provides the chip with 5V and 3.3V power.

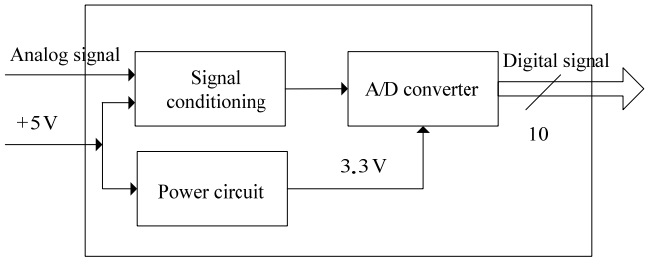


Fig. 2 Diagram of A/D converter circuits

### B. Signal Conditioning Circuit

System uses the A/D conversion chip; the peak-to-peak voltage analog input signal is +2V. For some requirements that the output range of analog signal does not comply with the A/D conversion chip, in order to expand the application of the system, signal conditioning is needed conversion before A/D conversion. Conditioning is to amplify, buffer, or calibrate analog signals to make it suitable for the input of analog / digital converter (ADC). The key is to choose the op-amp.

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During the design process, the signal conditioning circuit is double-voltage-follower circuit, using low-power voltage feedback amplifier AD8052. Signal conditioning circuit is shown in Figure 3. The input voltage range of this amplifier is -0.2V ~ 4V. Pin 8 is working voltage, using a single +5 V power to work properly. Input signal is Signal. According to the circuit connection as shown, the output voltage range of the signal AD Sigin enables A/D conversion chip work correctly.

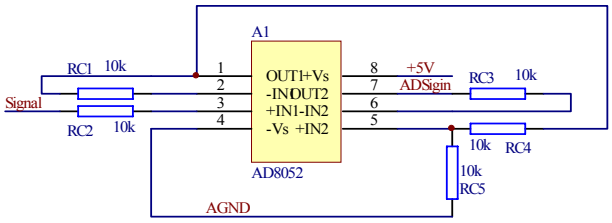



Fig.3 Conditioning circuit

## C. A/D Conversion Circuit

A/D conversion circuit, according to pre-selected sampling period, collects the analog signal inputting to the system. Taking into account the need for system flexibility and future upgrades, in this text, A / D conversion chip uses AD9203 chip with 10-bit accuracy and sampling rate from minimum 20kHz , up to 40MHz.

AD9203 is a high-speed A/D conversion chip with single channel and low voltage of AD Company. It has a stable and reliable accuracy. Within the whole range of sampling bandwidth, in the whole sample within the bandwidth, it always remains a 10-bit accuracy; fewer than 40MHz sampling rate, the significand can still reach 9.55; the differential non-linearity is ± 0.25 LSB; SNR and distortion remain at around 59dB. The working voltage of AD9203 is more flexible. It allows changes among 2.7V ~ 3.6V, especially suitable for portable devices to work in a high speed under low voltage. A/D circuit is shown in Figure 4. Analog signal ADSigin is inputted from pin 25; the conversion clock ADCLK provided by FPGA is inputted from pin 15;, the converted 10-bit digital signals ADD0 ~ ADD9 are inputted from pin 3 to pin 12 to FPGA and are being digitally processing in FPGA. This serial is completed by configuration devices such as the enhanced configuration device (EPC16, EPC8, and EPC4)[10-14].

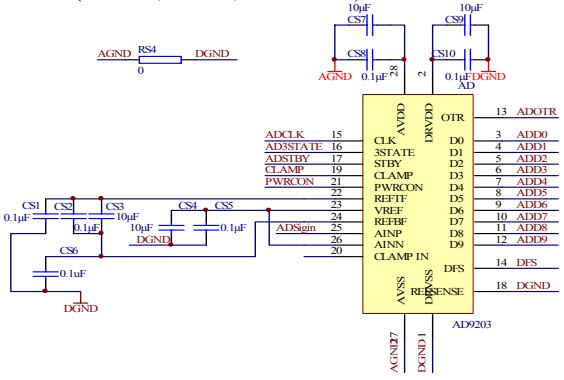



Fig. 4 A/D convert circuit

## D. Power Source Circuit

The voltage conversion circuit is designed to convert the source voltage of 5V to the A/DC chip and I/O of FPGA voltage of 3.3V. The adopted voltage conversion chip is LT1587CM-3.3 and the circuit is shown as figure 5. The inserted fuse is to protect the circuit from over flow of current .

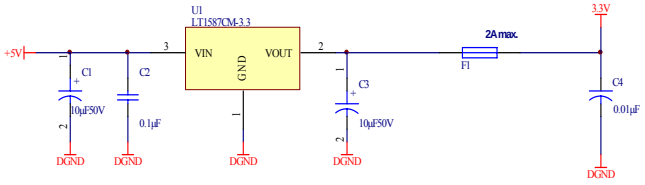



Fig. 5 Voltage convert module

## E. Peripheral Circuit Design of FPGA

The connection of Peripheral Circuit Design of FPGA is shown in Figure 6. Crystal oscillator provides 48MHz master clock, to realize clock conversion through the internal PLL, and VHDL programming of FPGA , providing working clock for the system; port JTAG , is used for configuring FPGA chip through downloading cable during program debugging stage; serial FPGA confabulates chip EPCS4, used for solidifying the program to the chip after program debugging, so that the system power can work; it is connected with the USB controller to achieve communications with the computer; In addition, an external conversion circuit is provided to switch 1.5V to 3.3V, as shown in Figure 7, providing FPGA with core working voltage.

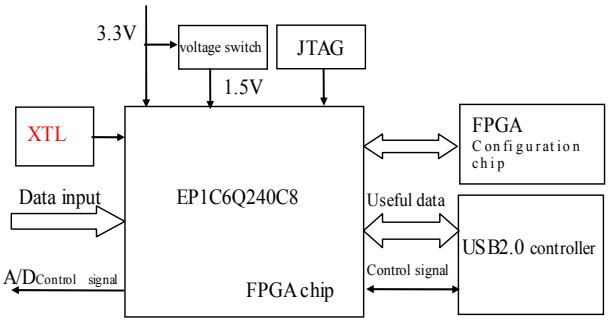



Fig. 6 FPGA periphery connection

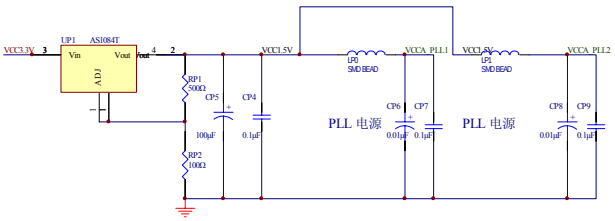



Fig. 7 Voltage transition circuit

## F. FPGA Configuration Mode

Configuration, also known as loading or downloading, is a process of programming the content of FPGA. In FPGA, there are many programmable multiplexers, logic, interconnecting contacts and RAM initialization contents and we need configuration data to control them. At present, there are three FPGA configuration and downloading patterns provided by Altera Corporation:

(1) AS (Active Serial): FPGA is in the initiative, led by FPGA device to complete boot configuration, which

controls the external memory and the initialization process. EPCS series such as EPCS1, EPCS4 configuration devices are designed for the AS model, which currently only support the Cyclone series. The Altera serial configuration device is used. Configuration data is transferred into FPGA through pin DATA0. Configuration data is synchronized at the input of DCLK and 1 bit of data is sent in one clock cycle.

FPGA is in a passive position, and the configuration process is controlled by an external computer or a controller. Smart host may be a microcontroller (MCU), configuration chip of Altera, PC, or even a CPLD.

JTAG Serial: JTAG interface is an industrial standard, mainly used for chip testing and other functions. It uses the IEEE Std 1149.1 joint boundary-scan interface pin and it can be completed by using the Altera download cable, or master controller.

Two kinds of configuration are used in this system, namely, AS mode and JTAG mode; AS configuration mode is shown in Figure 8; JTAG port circuit is shown in Figure 9.

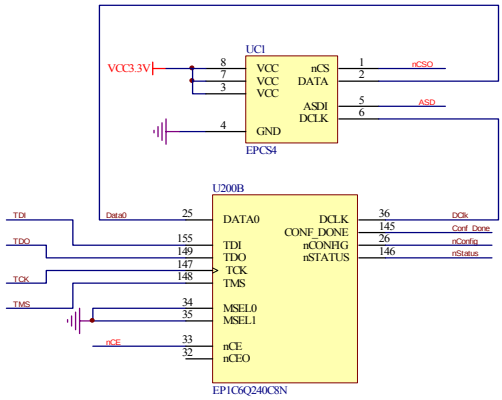



Fig. 8 AS configuration mode

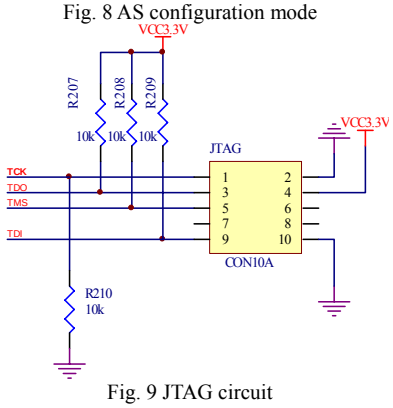



Fig. 9 JTAG circuit

In the programming process, first download debugging program in JTAG mode, after program debugging, then solidify the program into configuration chip EPCS4 in AS mode. The capacity of EPCS4 serial FPGA configuration chip is 4 times larger than EPCS1, fully meeting the design requirements. Moreover, it has a clear advantage that when downloading is not available in the AS model，we can use the tool that can create a .jic file which can be used in JTAG mode to verify whether configuration chip is damaged. When Cyclone is downloading and configuring, the download mode of JTAG corresponds .sof file and the download mode of AS corresponds .pof file.

### *G. USB Interface Module Design*

Since USB interface is of application of low price and good compatibility, hot-swappable, plug-and-play, saving system resources and more flexible, the range of applications and is becoming wider and wider. After the introduction of USB2.0, up to 480Mbps transmission speed has been able to meet current requirements that computers transmit data with periphery. In terms of cost advantages and reasonable performances, using USB2.0 interface to transfer data to a computer is the future trend of development. The USB2.0 interface chip in this design is CY7C68013A of Cypress's EZ-USB FX2 Series. it mainly Includes USB2.0 transceiver, serial interface engine (SIE), enhanced 8051,8.5 KB RAM, 4KB-FIFO memory, I / O ports, data bus, address bus and a General Programmable Interface (GPIF).

In order to facilitate data buffer of endpoint 2, endpoint 4, endpoint 6 and endpoint8 of USB2.0 controller 8 to better communicate with peripheral circuits, EZ-USB FX2 provides two interface modes: Slave FIFOs and GPIF (General Programmable Interface), which is controlled by register IFGFG.

(1)Slave mode "Slave FIFO"

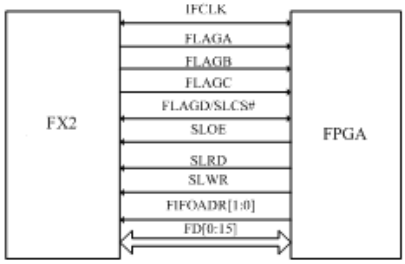



Fig. 10 Pin Connection of USB and FPGA

When EZ-USB FX2 is working in slave FIFO mode, the external circuit can read and write the data buffer of endpoint 2, endpoint 4, endpoint 6 and endpoint 8 of FX2 like common FIFO. Figure 10 shows in slave FIFO mode, the connection of FX2 and FPGA pin. FX2's IO pin and Slave FIFO pin are public, and by default, these pins are acting as ordinary IO pins, but to set as Slave FIFO mode, IFCONFIG [1:0] must be set to 11.

IFCLK is the interface clock, which can be generated by the chip (30MHz/48MHz), or by external input (5MHz ~ 48MHz); FLAGA-FLAGD is the FIFO standard pin, used to map the current state of FIFO; SLCS # is the chip selection signal slave FIFO, low level effective; SLOE acts as the output enabler, controlling the output of FIFP data terminal; SLRD is a FIFO data reading control terminal. In asynchronous mode, data reading and writing are controlled by high-low level outputted from the FPGA; SLWR is the FIFO writing control terminal, in asynchronous mode, also controlled by from pin level of the FPGA; FD [15:0] is the FIFO data bus, whose bit wide can be 8 bits, or 16 bits, decided by firmware program; FIFOADR [1:0] is the working mode selection terminal of the chip. When the chip is working in the Slave FIFO mode, high level can be sent to the two ports from FPGA. Configuration data is sent by terminal EP8 and sampled data is received by terminal EP2.

(2) Host mode "GPIF Master"

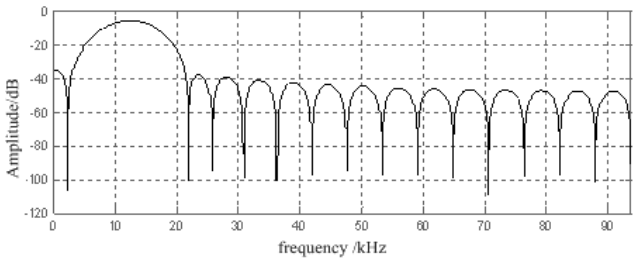
In the GPIF mode, EZ-USB FX2 software can be programmed to output read and write control waveform. Meanwhile, it can almost access any universal bus interface.

## III. Characteristics Of Filter

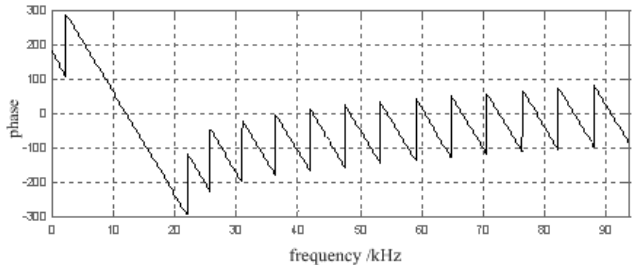
Using EP1C6Q240C8 chip of Altera's Cyclone series, we designed a 32-order FIR filter system of variable parameters, taking up 75% of on-chip logic cells and 71% of RAM after compilation. The filter uses the signal generator to generate a variety of input signals; the computer derives each order of factors according to given filter indicators and then configure the FPGA; FPGA and then uploads filtered data to the computer for displaying.

Specific experiments and analysis are as follows:

(1) Filter indicators: Window function is the Kaiser window, $\beta$=3.4, sampling frequency is 187.5kHz, pass-band frequency is between 10kHz ~ 15kHz, filter characteristics is shown in Figure 11; input signal is a mixed-signal of 27kHz and 10kHz sine wave, oscilloscope signal is shown in Figure 12 a ) and filtered data is shown in Figure 12 b). Through the filtered image it can be seen that this band-pass filter filtered out the 27 kHz sine wave signal which are over the pass-band frequency and basically restored 10 kHz sine wave signal.

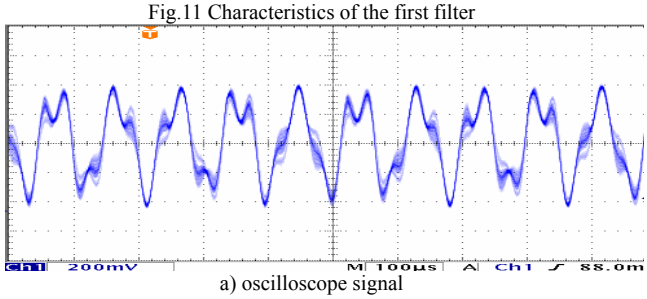



a) Amplitude-frequency characteristic

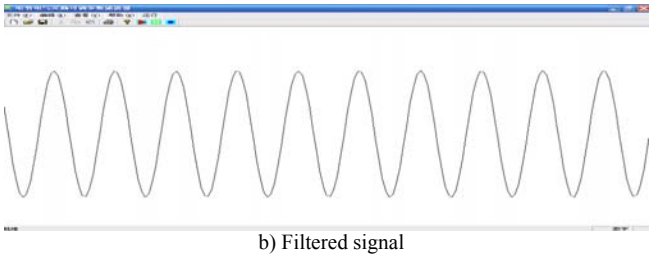



b) Phase-frequency characteristic

Fig.11 Characteristics of the first filter



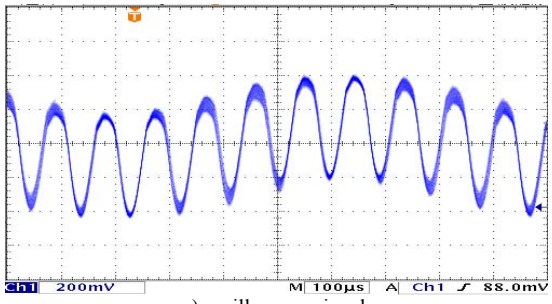

a) oscilloscope signal



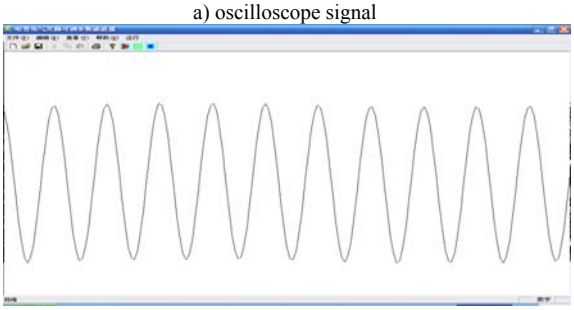
b) Filtered signal

Fig.12 Results of the fourth filter experiment

(2) Filter indicators: Filter indicators are the same as (1); Input signal is a mixed-signal of 1 kHz and 50 kHz sine wave, oscilloscope signal is shown in Figure 13 a) and the filtered signal is shown in Figure 13 b). The results can be seen from Figure 13 b) that the band-pass filter filtered out 1 kHz sine wave that is over cutoff frequency and it basically retained the 10 kHz sine wave signal.




a) oscilloscope signal



b) Filtered signal

Fig. 13 Results of the fifth filter experiment

The filter performance verification test is shown above. Through experiments (1) and (2) we validated the band-pass filtering performance of the filter. The filter is with a good filtering effect.

## IV. Conclusions

Along with the development of science and technology, digital filters, acting as a key technology of digital signal processing, directly impacts on the performances of many electronic systems. In this text, aiming at the requirements of real-time and flexibility of signal processing, based on FPGA as the core and on the basic theory of FIR digital filters, we designed an FPGA + USB2.0 + computer parameter-adjustable FIR filter system, combining the speed of FPGA and the flexibility of computer organically through USB2.0 bus.

This system uses USB2.0 to communicate with the computer. Through USB firmware programming, a both-way communication between computer and lower

computer FPGA is realized. In the parameter configuration mode, filtering parameters calculated by computer is downloaded to FPGA; parameter configuration is carried out in the internal FIR filter in the FPGA chip to realize the adjustable parameters of digital filters. In the filtering condition, the filtered data will be collected through USB2.0 bus, transferred to the computer to be displayed, analyzed and stored for further processing. It fully brought the flexibility of filtering system into play.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] Q. Z. Li, M. H. Wang and W. K. Gu, "Computer Vision based System for Apple Surface Defect Detection". Computers and Electronics in Agriculture, Vol. 36, No. 3, pp. 215-223, 2002.

[2] Z. A. Yanuar, A. Hussein and H. Masayuki, "Partial Discharge Characteristics of XLPE Cable Joint and Interfacial Phenomena with Artificial". *The 2nd IEEE International Conference on Power and Energy*, Malaysia, pp. 1581-1523, 2008.

[3] V. Piuri, F. Scotti and M. Roveri, "Visual inspection of particle boards for quality assessment". *IEEE International Conference on Image Processing*, Genova, Italy, pp. 521-524, 2005.

[4] Q. G. Miao and B. S. Wang, "Novel image fusion method using contourlet transform". *IEEE Transactions on Image Processing*, Vol. 6, pp. 548-552, 2006.

[5] H. Zhao, Y. Liu, C. L. Li. "XLPE insulation compound purity evaluation based on contam inant particlemapping technology", *Chinese Journal of Scientific Instrumen*, Vol 29, May. 2008, pp. 1035-1039.

[6] G. S. XU. "RHEOTENS Detection and Control System Based on Virtual Instrument Technology", Instrument Technique and Sensor, May. 2008, pp. 107-109.

[7] C.M. LI, J. H. WU, Y. J. ZHAO. "Development of Flat Field Holographic Concave Gratings with High-resolution", Journal of Optoelectronics, Laser, Vol 17, Jul. 2006, pp. 828-831.

[8] K. Z. Lin, J. Shi, H. Zhao. "Edge detection of one-dimension image onmulti-scale", Electric machines and control, Vol 111, Mar. 2007, pp. 287-291.

[9] M. Arulampalam, R. Ristic, N.Gordon, and T. Mansell, "Bearings-only tracking of maneuvering targets using particle filters," Journal of Applied Singnal processing, vol. 15, pp.2351-2365, 2004.

[10] G. S. XU. Sub-pixel Edge Detection Based on Curve Fitting [C]. The Second International Conference on Information and Computing Science, No. 2, 2009, pp.373-375.

[11] H. Zhao, D. T. Tu. Holograph Sizing of Contaminants in XLPE Cables[J]. IEEE Trans on EI, Vol. 4, 1991, pp. 217~221.

[12] Scholz J. Investigations on Fabrics Coated with Precious Metals Using Magnetron Sputter Technique with Regard to Their Antimicrobial Properties [J]. Surface and Coatings Technology, Vol. 192, 2005, pp. 252-256.

[13] Y. Yoshito, M. Horoshi and A. Shiro, Binocular Robot Vision System with Shape Recognition. International Conference on Control, Automation and Systems, Korea, 2007, pp. 2299-2301.

[14] G. S. XU. Linear Array CCD Image Sub-pixel Edge Detection Based on Wavelet Transform[C]. The Second International Conference on Information and Computing Science, No. 2, 2009, pp.207-210.