

# Design, Simulate and Development of a Computer Controlled Three-Phase Inverter for Precise Speed Variation of a Three-Phase Induction Motor

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**Abstract**--The speed of a three-phase induction motor can be varied within a wide range other than its rated value if its input parameters (frequency, voltages) are varied properly. For industrial, mainly in knitting and some other sophisticated use of three-phase induction motor, precise and accurate control of the speed of the motor is necessary. The present three-phase inverter is so designed that its input parameters can be easily varied through proper software program and computer interfacing hardware. N-channel MOSFET is used as power device but may be replaced with IGBT. A special one way delay circuit is introduced to ensure non short circuit situation. The input frequency to the inverter can be varied by varying the input voltage to the Voltage Controlled Oscillator (VCO). The proper input voltage to the inverter is set by Automatic Voltage Regulator (AVR) instructed by the computer. Though the frequency of the inverter can be varied between a wide range, the inter phase separation remains always  $120^\circ$  yielding a true pattern of a three-phase power supply. Introduction of microcomputer and associate of software programs in three-phase induction motor control system as proposed is accurate and reliable in terms of accurate and complex speed control of the motor.

**Index Terms**-- inverter, drive, motor, mosfet, vco

## 1. INTRODUCTION

Conventional three phase induction motor drives that are commercially available are Pulse Width Modulation (PWM) type[1,2]. In these cases line voltage is directly rectified and fed at inverter input. High frequency carrier (saw tooth) signals of around 1000 HZ is modulated with sine wave of required frequency. Output of inverter is high frequency square wave of different widths. When imposed across the three phase induction motor, current flows through the motor is almost sinusoidal of modulating frequency. Industrially used inverters are mainly controlled by microcontroller in

combination with Programmable Logic Circuit(PLC) [3,4]. Program is loaded in microcontroller as well as PLC and while running the motor, required speed is set through the buttons of PLC. The whole system is very complicated and not too much scalable and one microcontroller controls only one three phase induction motor at a time. The sections of the discussed inverter are shown in Fig. 1 as block diagram

The main objective of the inverter discussed in this paper is to generate voltage wave form shown in Fig. 2. The major inputs to the inverter are VCO input [5,6,7]. It is fed to the logic circuit to generate required frequency. Computer program sets the required VCO and AVR input as per requirement. A single phase line voltage is varied as required to be rectified for the input of the power section.

The logic circuit shown in Fig. 3 generates required frequency in six-step [5,6] triggering pattern. The delay circuit turns OFF the particular FET instantly and makes delay of 1.6 ms to turn ON the FET connected in the same vertical line as Fig 4. The delay circuit is shown in Fig. 5. This mechanism is to avoid short circuit situation. The triggering circuit sets the FETs ON and OFF when required but maintains electrical isolation between high voltage section and low voltage section(Fig 6). The rectifier section converts the ac voltage of the AVR into plain dc voltage which is then fed to the power section. The power section consists of six power FETs, diodes, capacitors etc. By properly controlling the ON and OFF states of these FETs phase A, B, and C are obtained which are then connected to the three-phase induction motor.

## 2. THE POWER SECTION

The circuit diagram of the power section for three-phase inverter with series FETs is shown in the Fig. 3 and the voltage waveform generated by it is shown in Fig 2. The inverter is the modified three-phase version of McMurray Bedford complementary commutation circuit [2,5,7,11].

Here six N-channel MOSFETs (IRF 740) have been used as power devices. The breakdown drain to source voltage  $V_{DS}$  of this device is 400V and threshold switching voltage is +4V. It can handle 10A at 25°C and 6A at 100°C. The tab is electrically connected with drain and is suitable for connecting heat sink.

FET1 and FET2 are connected in series where drain of FET1 is connected to high voltage lead of +Vdc and source of FET2 is connected to ground[2,5,8]. The source of FET1 and drain of FET2 are connected together and this point is called phase A. Similarly FET3 and FET4 are connected in series and their connecting point acts as phase B. FET5 and FET6 are also connected in series in vertical line where the connecting point of these two FETs acts as phase C. Phase A, B and C are connected to the three-terminals of a Y-connected three-phase induction motor. Each FET[1,3,9,10] is parallelly connected with a diode which by passes back emf of the motor to the voltage source(Fig. 4).

3. THE LOGIC CIRCUIT

The logic circuit (Fig. 3) is responsible for generating six step-triggering pulses for each cycle of the three-phase inverter. It comprises of a voltage controlled oscillator(VCO,4046A), a counter(7493), one 8 channel demultiplexes(4051), six three input OR-Gates(7432), and six three input AND-Gates(7404). The activities of each chip is explained below.

The IC 4046A is a phase locked loop with VCO. For our purpose we used only the voltage controlled oscillator(VCO) section. Pin No. 9 is the VCO input which is set by the computer interfacing circuit. To set the VCO frequency range, a resistor R (3k), and a ceramic capacitor (0.01µf) are connected properly. VCO input voltage has been limited between 1V and 2.5V to attain the oscillation frequency between 400HZ and 3500HZ. The output of VCO is available at pin 4. The output of VCO is fed to pin 10 of a 12- Stage Binary Ripple Counter, 4040 to get divide-by-8 effect and output is obtained from pin 6. This frequency is six times than the output of inverter frequency and is fed in the pin 1 of 4-bit Binary Ripple Counter, 7493. The output of 7493 is pin 9 as Q0, pin 8 as Q1, and pin 11 as Q2. These outputs are used as the input to the next chip, i.e. the demultiplexer. The 4051, is an 8-Channel analogue multiplexer with three digital select inputs ( $S_0$  to  $S_2$ ). Pin 6 is chip enable (E) pin, pin 11, 10 and 9 are select  $S_0$ ,  $S_1$  and  $S_2$  respectively. Pin number 3 (Z) is common input/output to all eight input/output pins. By the proper combination of select pins any of the Y pins can be connected to the common z pin. In the present work select pins of demultiplexer 4051, are connected to the output of counter 7493. When counter 7493 counts zero the output  $Y_0$  goes high and all other Y outputs of demultiplexer remain in floating states with high impedance. With the advent of the count of 7493 the Y output of the demultiplexer also advances to the higher value. As soon as the counter counts six,  $Y_6$  is selected

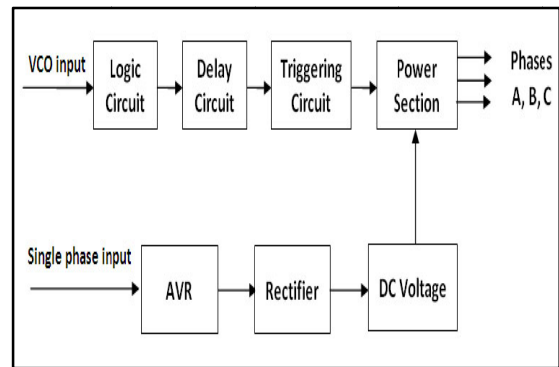


Fig 1. Block diagram of the three phase inverter

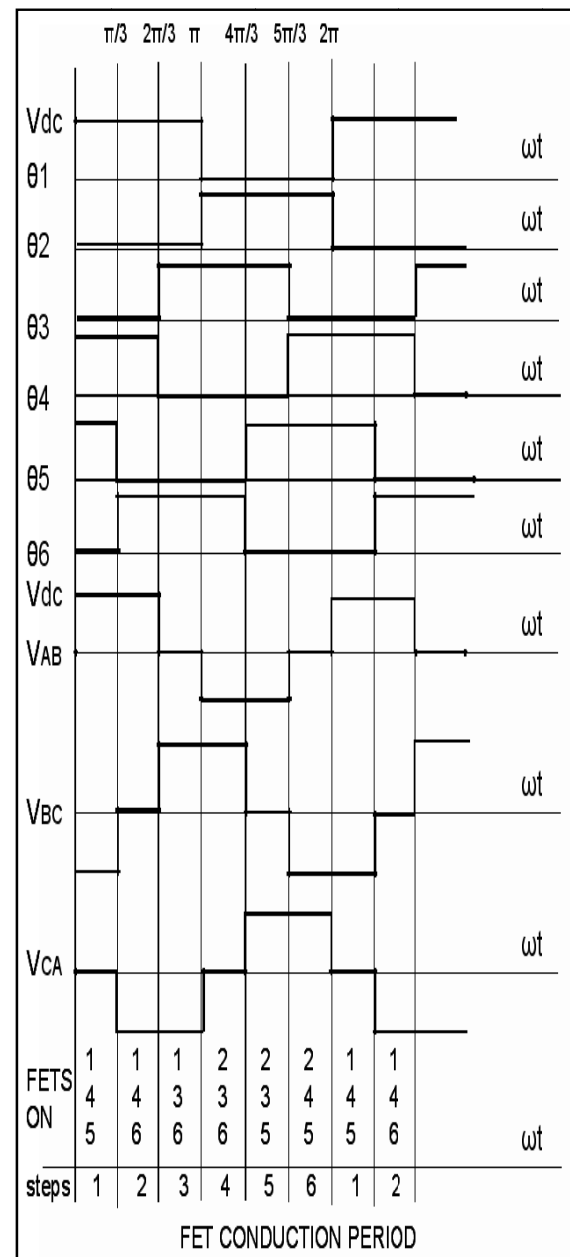


Fig 2. Phase to phase wave form

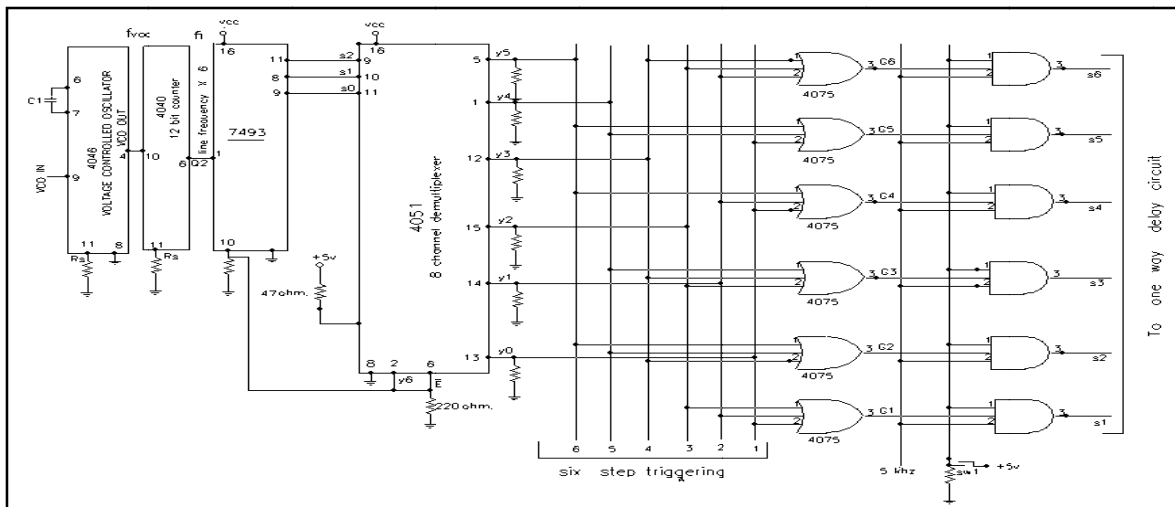


Fig 3. Logic circuit for generating triggering signal for power devices

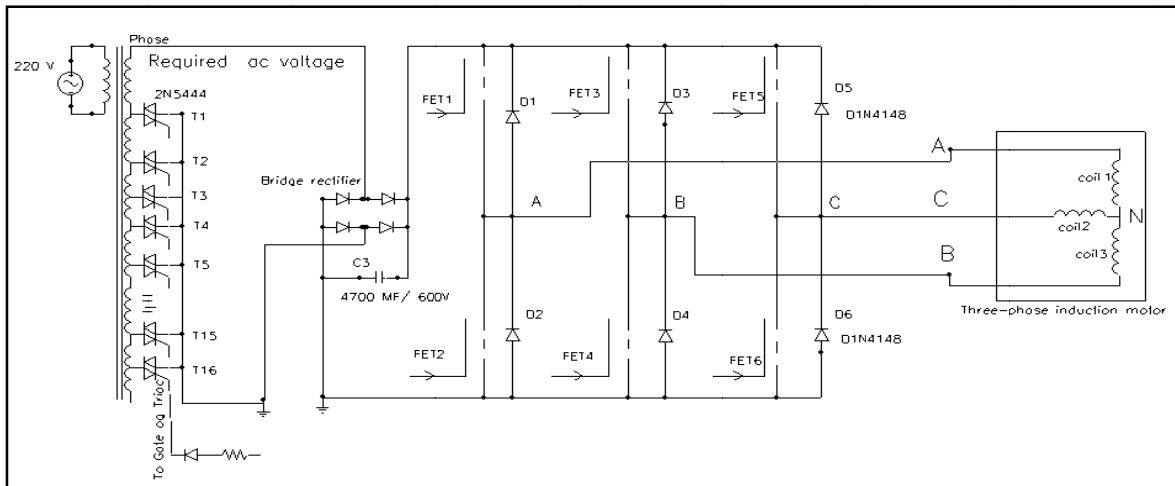


Fig 4. The power section, three-phase bridge inverter

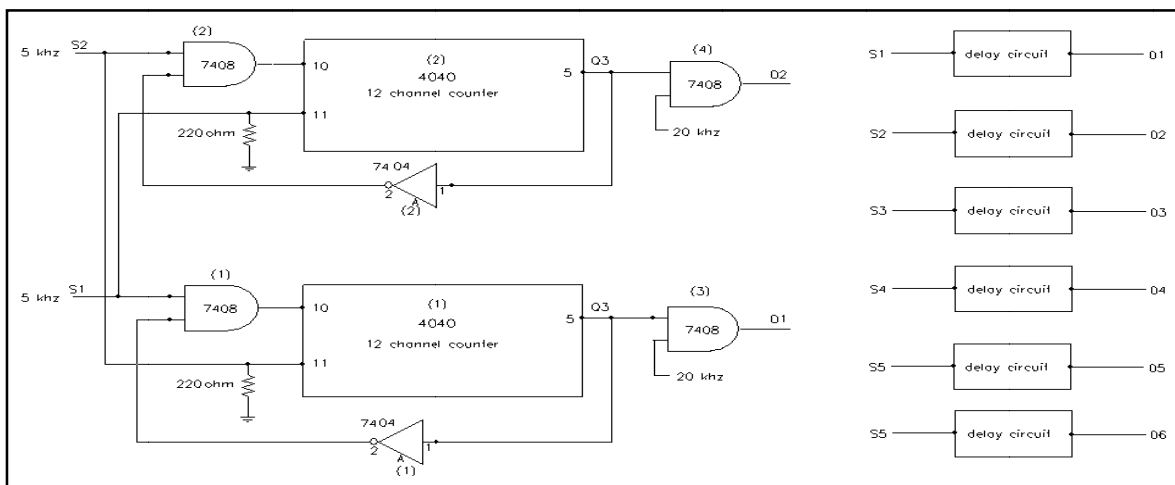


Fig 5. The one way delay circuit

in the demultiplexer and goes high and instantly resets the demultiplexer and the counter 7493. In this way count always goes from 0 to 5 and select always goes from  $Y_0$  to  $Y_5$  respectively. In fact these six outputs  $y_0$  to  $y_5$  are six fundamental steps which govern the fundamental six steps of each cycle of the inverter frequency.

From the Fig. 3 we see that at each of the six steps three FETs remain ON and when transition goes to the next step only one FET turns OFF making the other FET ON on the same vertical line. To ensure the features portrayed in Fig. 2 i.e. the voltage waveform and FETs ON/OFF state we used six 3 input OR-GATEs. They are available in two ICs namely 7432A. In step one  $Y_0$  is high and gate G1, G4 and G5 are high keeping G2, G3 and G6 low. After  $\lambda/6$  cycle time  $Y_1$  goes high and all other  $Y$ s remain low. This is step 2. In this step G1, G4 and G6 are high. So, we see that between step 1 and step 2 G5 and G6 toggle their ON/OFF state. In this way at every interval of  $\lambda/6$  cycle time, one cycle step proceeds toggling between two vertical FETs. But at any instant we get three Gs high and consequently three FETs ON.

Two ICs 7404 are used which provide us six 3-input AND gates, Each G output is fed to one AND gate. Suppose G1 is fed to AND-gate 1 and output is obtained at S1. One input lead of 3-input AND-gate is connected to 5KHz source and other input lead is connected to a switch sw1 which remains either in +5V or 0V. So when sw1 is at +5V AND-gates provide 5kHz frequency at output when respective G inputs are high. So, with the help of AND Gates we converted high G states into 5KHz of S states. At any instant we get three S terminals containing 5KHz pulses and other three S terminals remaining in the low state.

4. THE ONE-WAY DIGITAL DELAY CIRCUIT

In the power section of the present three-phase inverter (Fig. 5) it is observed that two FETs remain in the same vertical line between +Vdc ( $\approx 400V$ ) and Ground ( $\approx 0V$ ). At any instant only one FET of each vertical line remains ON. After each  $\lambda/2$  cycle time of the inverter frequency, FETs of the same vertical line toggle between their ON/OFF states. But due to the capacitance of the triggering circuit at the instant of toggling, two vertical FETs remain ON for a short time. But this is very dangerous because such situation creates short circuit between high voltage and ground causing the FETs and rectifier to burn up. To avoid such dangerous situation we designed a special delay circuit which at the transition moment turns the previously ON FET OFF instantly and turns the other FET ON after a certain interval of time ( $\approx 1.6ms$ ). We call it one way delay circuit for its special one way delay action. In Fig. 5a FET triggering pulses are shown. Two consecutive pulses are for two vertical FETS. +4V is threshold voltage to turn a FET ON/OFF. At the upper edge of the pulses we find a gap of 1.6 ms above +4V, which is the time to keep both the FETs OFF of a same vertical line.

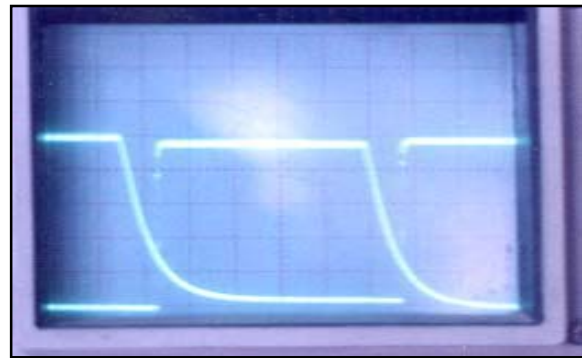


Fig 5a. Photo graph of the triggering

Each delay circuit (Fig. 5) governs the ON/OFF state of two vertical FETs. It consists of two 4040 counter, four 2-input AND-gates and two inverters. Their mutual connections are shown in Fig. 5. Here for ON stage input S1 gets 5 KHZ and output D1 gives 20 KHZ. For OFF stage both input and output are 0 V.

The summary of the activities of delay circuit is  
 At time  $t = 0$ ,  $D1 = 0$ ,  $D2 = 0$ ,  
 result: FET1 = Off, FET2 = OFF  
 At time  $t = 1.6ms$ ,  $D1 = 20kHz$  pulses,  $D2 = 0$ ,  
 results: FET1 = ON, FET2 = OFF  
 At time  $t = \lambda/2$  inverter cycle time,  $D1 = 0$ ,  $D2 = 0$ ,  
 results: FET1 = OFF, FET2 = OFF.

Overall effect of this delay circuit is that we get definite OFF time of 1.6ms at the toggling stage of FETS in the same vertical line in the inverter. Three such delay circuits are needed to govern the three vertical pair of FETs. More generalised equation for setting delay time is

$$T_D = \frac{1 \times 2^{n+1}}{f}$$

Here

$T_D$  = time delay,  $f$  = input clock

$n$  = refers to nth output ( $Q_n$ ) of binary counter

5. THE TRIGGERING CIRCUIT

The threshold voltage [1,5,7] to turn a FET ON/OFF is +4V. So we need at least +4V at the gate or source of FET to turn it ON. When a particular FET is to be turned ON, the respective  $D_n$  lead of the delay circuit keeps 20kHz pulses. These pulses are fed to the base of an NPN transistor through a resistor and a diode (Fig. 6). In a 2" ferrite rod 25 No. wire is wound as N1:N2 = 60:60. One end of the primary coil is connected to the collector of the transistor while the other end is connected to +12V. The secondary coil is connected properly to a bridge rectifier, 0.1 $\mu$ F ceramic capacitor, 4.7V zener diodes and obtained triggering voltage for FET.

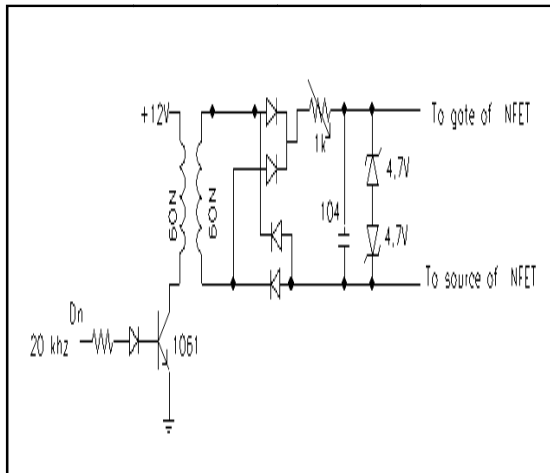


Fig 6. Triggering circuit of N-channel MOSFET

6. COMPUTER INTERFACING

Attempt is made here to explain in detail what has been designed and developed in terms of hardware and software for establishing successful and reliable interfacing between the microcomputer and control circuit[1,4,5,7,8]. The whole work has been divided into two major sections. They are

- a) Design and development of electronic circuit
- b) Design and development of software programs

Obviously the success of the present interfacing relies on the successful coordination of hardware and software operation.

To establish data communication between microcomputer and motor control circuits, an electronic circuit is developed. This circuit board is called as computer interfacing card because it performs the equivalent service as conventional cards do. Fig. 8 is the circuit diagram of the computer interfacing card. The circuits of this interfacing card is divided into three main sections. They are:

- a) Address decoding section
- b) Data reading section
- c) Data writing section

To establish physical connection between I/O slot of microcomputer[1,8,11] and interfacing card we used a 24 wire parallel bus. Among them 10 wires have been used for address, 8 wire for data, 2 wire for Read/Write, 1 for address enable, 1 for system clock, 1 for ground, 1 for +5V

A. Address Decoding section

This section comprises of one magnitude comparator (74LS688), one demultiplexer (74LS138) and one NAND Gate (7403)[Fig. 8]. A brief discussion of the above chips are given below.

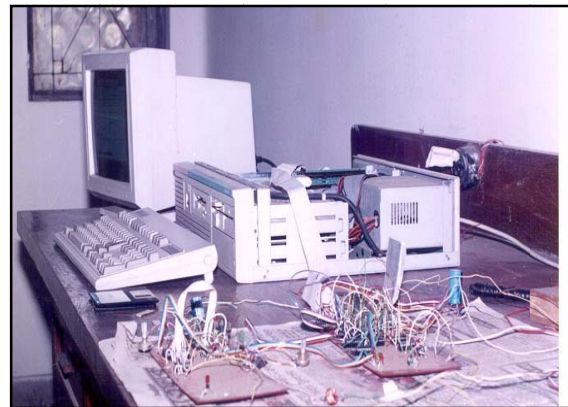


Fig 7. Computer interfaced with inverter



Fig 7a. Motor loading mechanism

74LS688 is a magnitude comparator. It can also be used as a programmable decoder. It is a 20 pin DIP IC. It performs comparison between two eight bit binary or BCD words. Pins 3, 5, 7, 9, 12, 14 and 18 (Q0-Q7) are address inputs and pins 2,4, 6, 8, 11, 13, 15 and 17 (P0-P7) pins are programmed for a desired address. Its output pin 19 will be active (low) only when that desired address appears at the address inputs (Q0-Q7).

A 3 to 8 line decoder/demultiplexer(74LS138) is used and its output becomes active (low) when a specific (1 of 8) memory address is chosen. A Quad 2 input NAND gate(74LS03) is used for Read/Write mode selection

In our present design we can select 8 addresses (320H-327H) though we are using only three. The bit patterns of the address 320H, 321H are given below.

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	1	0	0	0	0	0	= 320H
1	1	0	0	1	0	0	0	0	1	= 321H
1	1	0	0	1	0	0	0	1	0	= 322H
P7	P6	P5	P4	P3	P2	P1				
Q7	Q6	Q5	Q4	Q3	Q2	Q1				
Po = Qo = +5V										

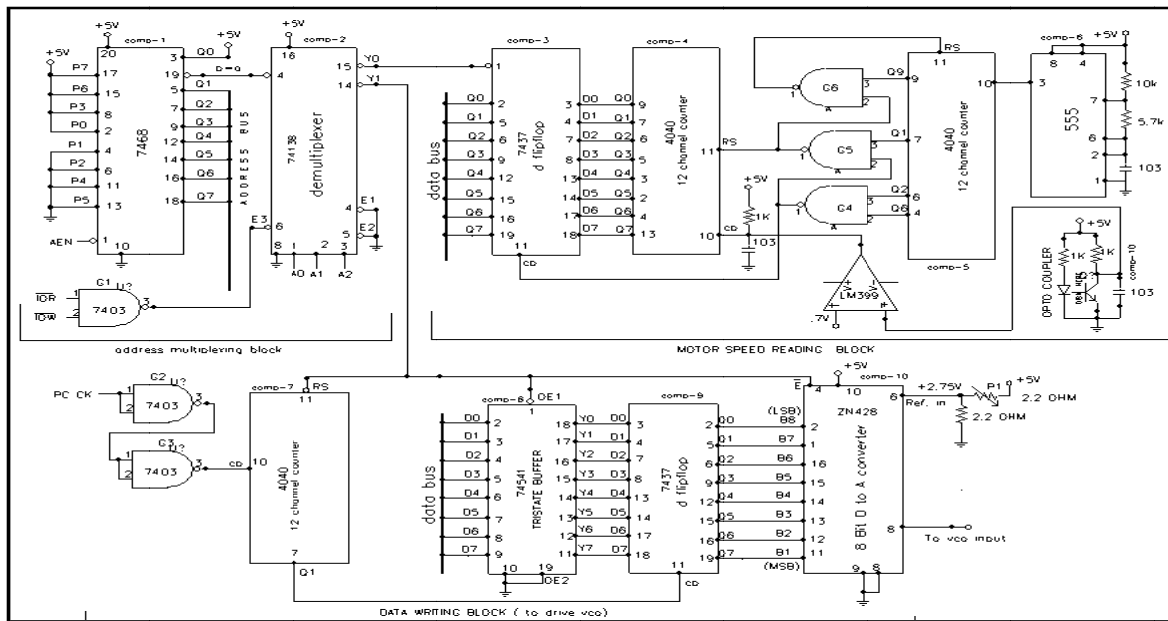


Fig 8. Different section of computer interfacing circuit

To ensure the above bit patterns, wires A0, A1, and A2 of address bus are connected to the encoding inputs( 1,2 and 3) of demultiplexer 74LS138. P0 and Q0 of magnitude comparator 74LS688 are connected to high. Pin P1 to P7 are programmed as per pattern. Q1-Q7 are connected properly to the address bus. Read and write wire are connected to the two inputs of a NAND gates and the output of the NAND gate is connected to the enable pin 6 of the decoder 74LS138. As a result when address 320H and Read /Write action prevails in the bus, Y0 (pin 15) of 74LS138 is active(low), which we use for reading action. Similarly when address 321H and Read/Write action prevails in the bus, Y1(pin 14) of 74LS138 becomes active(low), which we use for write action.

**B. Data Reading Section**

This section comprises of one D-flipflop (74LS37), two counters(4040), three NAND-gates, 3 AND gates one triple five timer(555), and one optocoupler[1,8]

*Working Procedure:* A U shaped infrared optocoupler (component-10 in Fig. 8) is used to count motor speed. A circular disk with 8 slits along its circumference is to ensure the above bit patterns, wires A0, A1, and A2 attached to the rotor of the three-phase motor. The opto coupler is loaded on a stand in such a way that the disk can move between the two wings of the opto coupler when the rotor of the motor moves.

When the open portion of the disk stands before the base of the transistor, infrared from the diode falls on the base of the transistor, the transistor conducts and the collector (10p) of the transistor goes low. But when the opaque portion of the disk stands before the base of the transistor, no infrared falls on the base of the transistor, it does not conduct and the collector (10p) goes high. As a result when one slit of the disk passes between the two wings of the optocoupler, a pulse is generated at the

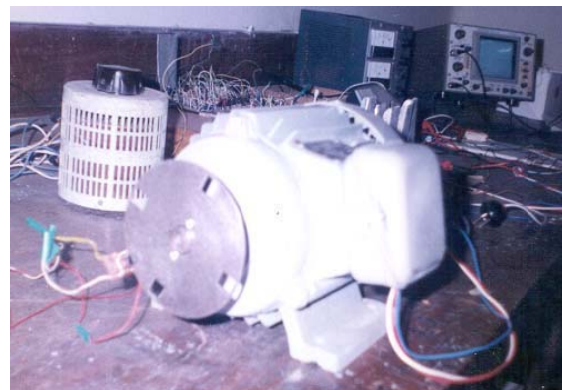


Fig 9. Pulse generation (disk, opto coupler & motor)



Fig 9a. Pulse generated from opto coupler

collector of the transistor(Fig. 9). So, one revolution of the disk, i.e. one revolution of the motor rotor generates 8 pulses. These pulses are further shaped with the help of a comparator LM399 and then fed to the input of the counter 4040 (comp-4).

Simultaneously 200 HZ pulse is generated with the help of a 555 timer. The count stored in the internal buffer of D-flip-flop(comp-3) is 68 pulse duration time. When address 320H is selected by the microcomputer, Y<sub>0</sub> of comp-2 and pin 1 of comp-3 go low. When pin 1

of comp-3 is low, the data in the internal buffer of comp-3 is transparent to the data bus. So setting address 320H in the read mode microcomputer reads the count(Data) and after further calculation the computer displays the motor speed on the monitor.

**Calculations :**

Frequency at the input of counter(comp-5) = 200 Hz  
 Pulse width = 1/200 Hz = 5 ms  
 So, sampling time = duration of 68 pulses  
 =  $5 \times 10^{-3} \times 68 \text{ sec} = 340 \times 10^{-3} \text{ sec}$

Let count stored at the internal buffer of comp-3 is N, which is generated from the optocoupler due to the disk's rotation. Therefore,  
 pulses generated per second =  $( N / 340 \times 10^{-3} )$   
 Rotor rotation per second =  $( N / ( 8 \times 340 \times 10^{-3} ) )$ ; 8 is the No. of slots per disk  
 Motor speed =  $( N \times 60 ) / ( 8 \times 340 \times 10^{-3} ) \text{ rpm}$   
 = 22.05 N rpm

**C. Data writing Section**

This section consists of one counter 4040 (comp-6) one tristate buffer 74541, (comp-8), One D-flip-flop 7437, (comp-9), and two AND gates.

*The working procedure:* When micro computer selects/decodes address 321H at a writing mode, Y1 of comp-2 goes low. This enables tristate buffer comp-8. So, data in the data bus is available at the input of D-flip-flop, i.e. comp-9. Again due to the low level of Y1 as well as reset pin 11 (Rs) of counter (comp-7), it becomes countable. Clock pulses from microcomputer are always available at the input of this counter(comp-7) through NAND gates G2 and G3. As soon as the counter(comp-7) becomes countable due to the low stage of Y1, clock pulse are available at pin 7 of comp-7. These pulses are fed at pin 11 of comp-9 which transfers the data at its input (D0-D7) to the output (Q0-Q7) and remains same until further change. So, instructed by the program, computer writes eight bit data at the output of comp-9. This data is further fed at the input of DAC to set an appropriate voltage level to drive VCO for generating inverter frequency. Following equations and examples shows how to set a particular voltage at VCO input to have particular inverter frequency.

$$f = \frac{f_i}{6}, f_i = \frac{f_{vco}}{2^{n+1}}, f_{vco} = 6 \times 2^{n+1} \times f$$

Here,  $f_{vco}$  = VCO frequency,  $f$  = inverter frequency

$n$  = refers to  $n_{th}$  output of binary counter

For  $Q_n = Q_{11}$

$$f_{vco} = 6 \times 2^{n+1} \times f = 6 \times 2^{12} \times f = 12288 \times f$$

$$\text{Motor Synchronous speed, } N_s = \frac{120 \times f}{P}$$

For 4 pole machine  $P= 4, N_s = 30 \times f$

**8. THE SOFTWARE**

To establish a successful and efficient communication between the microcomputer and the motor control circuit, it needed to write plenty of programs to perform and control a number of activities in real time mode. We had to choose a software to write the required programs which would be able to provide the following facilities:

- efficient computing speed and accuracy
- embedding assembly language command in the program to perform
- chip/register level communication.
- capable of handling graphics display to render visual impression.
- d) capable of dividing the big task into small modules and accumulating them
- under a main program.

In order to fulfill all these requirements C++ software was chosen as the programming language[9,10].

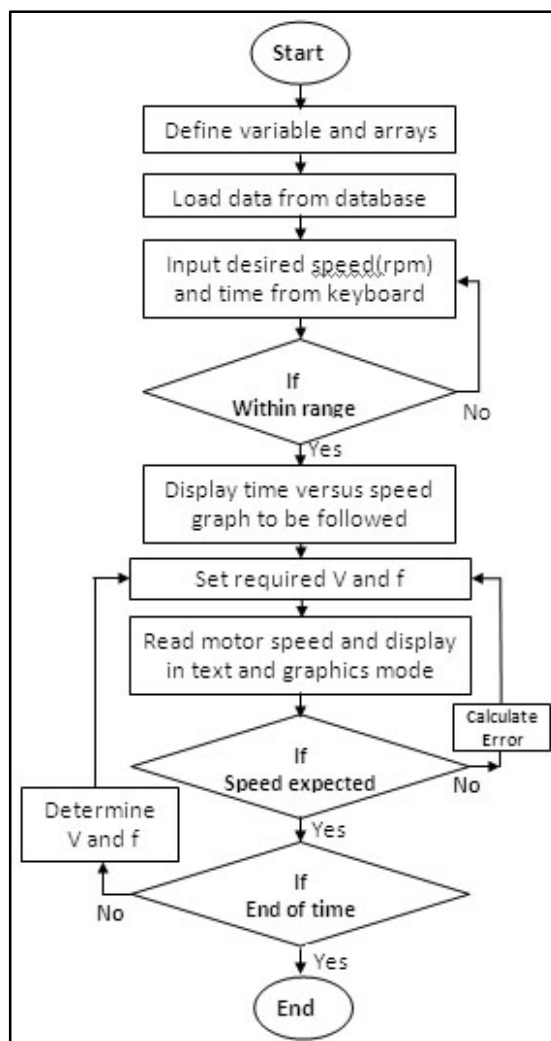


Fig 10. Flow chart of software

A. Working steps of the program as coded in C++

The flow chart is shown in Fig. 10. The whole motor speed range is divided into several steps and associated VCO voltage level, and inverter voltage is predefined and stored in a table of database. Inserting required values and clicking run button as shown in fig 10b, motor begins to start. Throughout the whole set time the program reads the required value from database and set the relevant values through write action. A sample data is shown in fig 10a.

To write 0 level at address 0321H following assembly language is used.

```
-AL = 0; // loads the lower eight bit of Accumulator with zero
asm MOV DX, 0321H; //Loads 0321H in DX register
asm OUT DX, AL; // writes the content of AL register to 0321H address
```

9. SIMULATION

To run an induction motor at different speed other than designed different input voltage and frequency are required. Simulated result obtained from MATLAB SIMULINK TOOLBOX displayed in Fig. 11b and Fig. 11c shows though inverter output is square wave but after proper filtering sine wave is obtained across load. Filtering component as shown in fig 11 and fig 11a, need to vary for different inverter output frequency. Changing inductance and capacitance of filter portion is a very complicated task even the whole system is controlled with microcontroller properly programmed.

In our design output of inverter is quasi square wave, Fig. 10d, directly employed at motor terminals. No filtering is required. Simply triggering a particular triac, fig 3, required voltage is obtained after rectification at inverter input.

Predefined Data in the Database table							
ID	step	voltage	dac_data	dac_voltage	frequency	rpm_sync	rpm_exp
1	1	44	116	1.25	10	300	299
2	1	46	117	1.26	10.39	312	300
3	1	47	118	1.27	10.79	324	322
4	1	49	119	1.28	11.18	335	324
5	1	51	120	1.29	11.58	347	346
6	1	53	121	1.30	11.97	359	347
7	1	54	122	1.32	12.37	371	368
8	1	56	123	1.33	12.76	383	370
9	1	58	124	1.34	13.16	395	392
10	2	60	125	1.35	13.56	407	394
11	2	61	126	1.36	13.95	418	415
12	2	63	127	1.37	14.35	430	416
13	2	65	128	1.38	14.74	442	438
14	2	67	129	1.39	15.14	454	440
15	2	68	130	1.40	15.53	466	462
16	2	70	131	1.41	15.93	478	464
17	2	72	132	1.42	16.33	490	485
18	2	74	133	1.43	16.72	502	487
19	3	75	134	1.45	17.12	514	508
135	16	277	250	2.70	63.02	1891	1858
136	16	279	251	2.71	63.41	1902	1859
137	16	281	252	2.72	63.81	1914	1881
138	16	282	253	2.73	64.2	1926	1882
139	16	284	254	2.74	64.6	1938	1904
140	16	286	255	2.75	64.99	1950	1906

Fig 10a. Stored data in the table

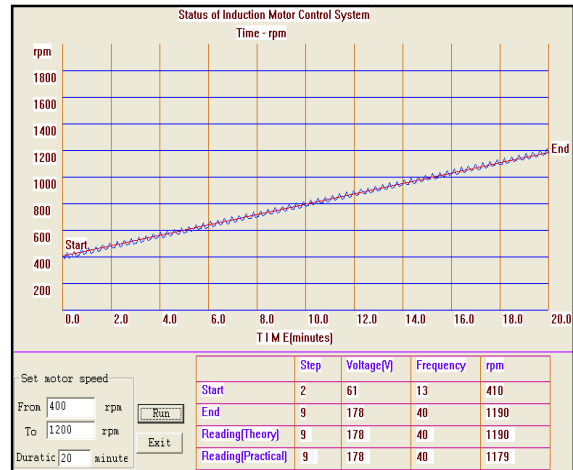


Fig 10b. Computer screen

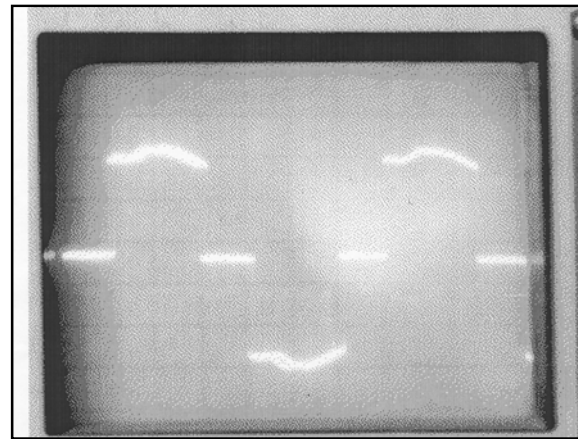


Fig 10c. Inverter output single phase

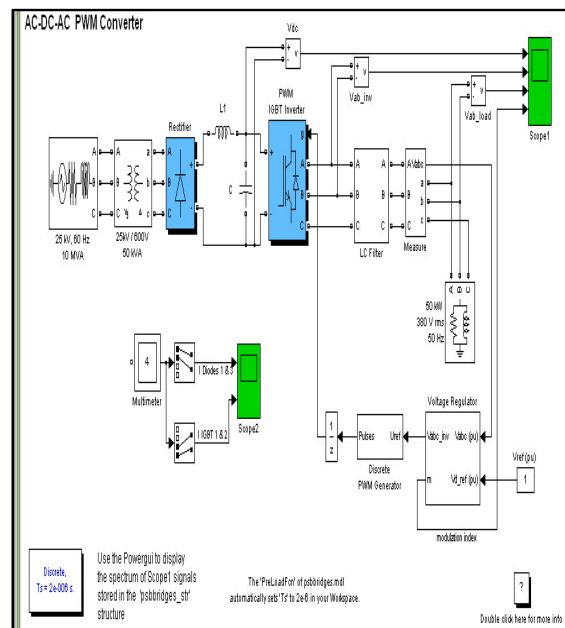


Fig 11. AC-DC-AC PWM converter (Matlab simulink circuit)



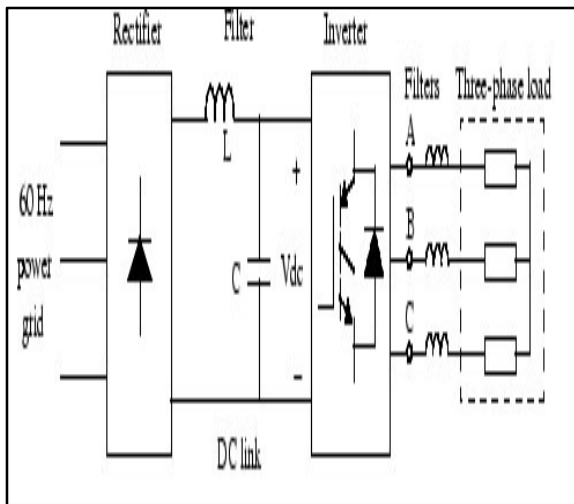


Fig 11a. AC-DC-AC PWM converter

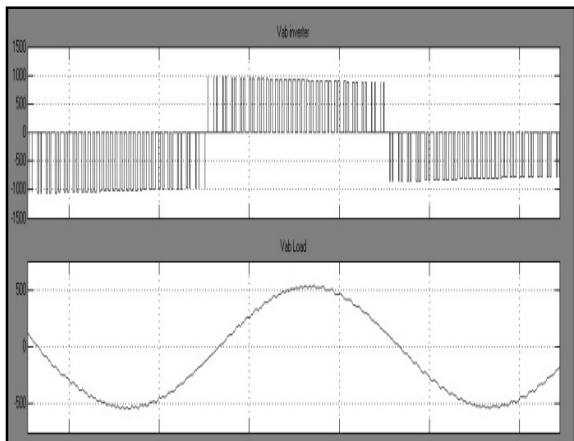


Fig 11b. PWM inverter output 100V, load 500W

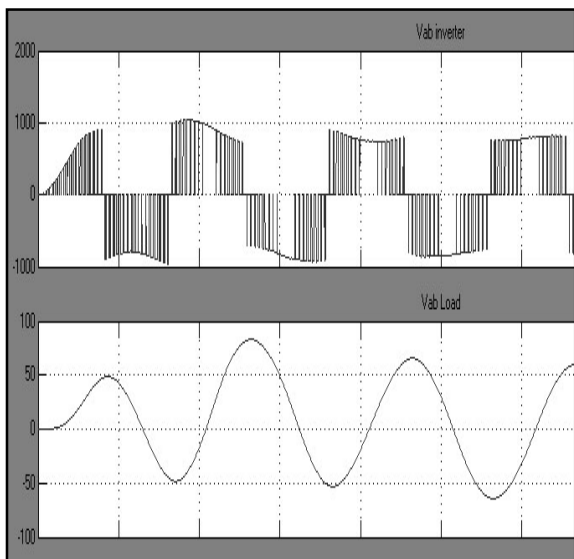


Fig 11c. PWM inverter output 100V, load 50W

10. CONCLUSION

The developed three-phase inverter was used to drive a three-phase squirrel cage induction motor. The rated value of the motor was 620 watt, 1390 rpm, 240 volt and 1.4 Amp at full load . As the motor speed was read and controlled by a microcomputer , the VCO input voltage of the inverter was set and changed by the microcomputer. We found that the inverter was successfully worked from 300rpm to 1900rpm of the motor changing the inverter output frequency from 10Hz to 65Hz. The inverter was used loading the motor sufficiently up to 1000 rpm. As the breakdown voltage of

the power device (IRF740, MOSFET) was 400 V which was not enough to tolerate the voltage required to run the motor at higher speed, the motor was not run at full loaded at the higher speed (1000-1900) rpm . Power devices IGBT with higher break down voltage (> 600 V) is required to be used to run the motor at higher speed. However, setting the appropriate input voltage to the inverter is done with the help of proper program, interfacing circuit and voltage controlling instrument. The inverter was tested (not loaded at > 1000 rpm) with in a wide range of frequency (10Hz-65Hz) and found no triggering failure/disorder of the power device. The logic circuit as well as one way delay circuit acted properly.

The inverter is designed on the basis of McMurray Bedford complementary commutation inverter[2,7]. N-MOSFETs are used in the place of GTO SCRs as power devices to avoid inter device commutation failure and also to avoid extra high voltage source to implement commutation.

Due to the feedback capabilities of the designed control system motor speed can be kept very close to the desired speed with respect to the time. Setting up time and expected speed of motor is very flexible as they are set through the form on the computer screen. A single computer is enough to run, control and monitor the status of multiple three-phase induction motors simultaneously. As the designed three phase induction motor control system is fully computerised, the running condition of the motors at any instant can be stored in the database, can be observed from any place with in the computer network.

11. FUTURE WORK

Further development of the described inverter may be improved by selecting proper devices, improved triggering circuit, signal amplifier/repeater and efficient interfacing algorithms.

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