Design and Optimization of Test Architecture for IP Cores on SoC Based on Multi-objective Genetic Algorithm

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***Abstract*—For system-on-chip (SoC) test based on IP cores integration reuse, the IEEE 1500 Standard has given specific testing architecture. In this paper, we aim at building controllable test architecture for IP cores on SoC based on IEEE 1500 Standard. The technique applied is referred to as test control switch which is configured to the Wrapper of IP cores. We design a switch control register (SCR) to configure the state of the switches, and apply the expanded TAP (eTAP) based on IEEE 1149.1 Standard to control the SCR and the Wrapper of IP cores. In addition, we design the chip level test control architecture which can be widely used for test of SoC based on IP cores. Finally, we apply the software of Modelsim to implement simulation about the control mechanism of the SCR and the eTAP. The simulation results show the effectiveness and controllability of the test architecture**

Besides, the paper builds SoC self-testing architecture through connecting Built-In-Self-Test (BIST) and IEEE 1500 Standard. The technique applied is referred to as Niche Genetic Algorithm (NGA) which is one of Multi-objective Genetic Algorithm, we build Block testing model which is optimization for partition of Testing-Access-Mechanisms (TAM) and IP cores based on NGA. The studies we have performed showed that the NGA can reduce SoC testing time effectively and the Block testing model can achieve testing data sharing for multiple IP cores.

***Index Terms*—IEEE 1500 Standard, SoC, Test Control Switch, Switch Control Register, expanded TAP, TAM, NGA**

I. INTRODUCTION

The system on chip (SoC) is widely used in large amount electronic products nowadays. The appearance and application of SoC due to the advancement of semiconductor technology and the progress of designing technology based on Intellectual Property (IP) cores reuse. The reuse technology improves the designing efficiency immensely, but the increase of SoC complexity brings great challenge for SoC test. Traditional approaches for testing core-based SoC completely relay on additional Design for Testability (DfT) structure. The IEEE 1500 Standard [1] has defined a Wrapper structure for testing of IP cores, and the appearance of the IEEE 1500 Standard facilitates the test process of IP core.

Recent years, for the study of SoC testing, many academic researches focus on the optimization design of Testing Access Mechanism (TAM) and testing Wrapper based on IEEE 1500 Standard. For the study of the TAM, strategies of Test Bus [2] and Test Rail [3] have been proposed for transfers from/to the IP cores under test. The paper of [4] proposes a novel automated synthesis methodology to generate SoC built-in self-test (BIST) in order to test IP and custom logic cores with high fault coverage. The paper of [5] presents new modular logic BIST architecture and pays attention on the design and analysis of BIST-ready IP cores and system integration. Despite the recent progress reviewed in lowering test power, reducing testing time and increasing fault coverage [18, 19, 20], there is no generally accepted test control architecture for IP cores with better controllability and effectiveness.

In this paper, a novel kind of test architecture for IP cores on SoC is investigated. The paper adopts the IEEE 1500 Standard to implement test. The IEEE 1500 Standard has defined a Wrapper structure for IP cores, and the paper configures three kinds of switches for the Wrapper and designs a Switch Control Register (SCR) module to control all the switches. The work mechanism of the SCR and the Wrapper was controlled by the chip level control module. The organization of this paper is as follows. In Section II, we discuss the three kinds of test control switches, which are configured to the Wrapper of IP cores based on IEEE 1500 Standard. In Section III, we present the design of the SCR which is used to enable the switches of the under test IP cores. In Section IV, we address the chip level control module, which is a expand TAP (eTAP) controller based on the IEEE 1149.1 Standard, and the eTAP is a FSM. In Section V, the

This work was supported by the National Natural Science Foundation of China (No: 60861003)

doi:10.4304/jcp.8.2.517-524

whole chip level test structure is illustrated. In Section VI, we examine the test control mechanism of the eTAP controller. Section VII present the united circuit of IEEE 1500 Standard IP core testing architecture and BIST architecture and gives design model and analysis. In Section VIII, we address the $P_{PAW-Block}$ problem, and apply NGA to the partition of IP cores and assignment of TAM ($P_{PAW-Block}$ problem). Section IX examine $P_{PAW-Block}$ through Benchmark circuits. Section X concludes the paper.

II. Test Control Switch for IP Cores

The test access mechanism of IP cores includes serial and parallel mode, the serial access mode is required by IEEE 1500 Standard. In addition, the paper also studies the parallel access mechanism. In order to achieving the flexibly controllability in the test process, the paper designs three kinds of switch circuits for IP cores which has the Wrapper structure.

A. Serial-access Control Switch

The serial-access control switch (SCS) is depicted in Fig.1, it has five data ports. The ports WSI and WSO connect the serial data input and serial data output of the Wrapper respectively. The data input port Si and data output port So connect to the chip level test control module, and the switch enable signal Switch-en (i) come from the switch control register (SCR). In Fig.1, the circuits a and b are accessed when Switch-en is in the higher level, while the circuit c is accessed when Switch-en is in the lower level. The SCS can provide instruction for the Wrapper instruction register (WIR), and can be as the serial test data channel in the serial test process for IP cores. Moreover, the SCS has the bypass function, when the Switch-en (i) is in lower level, the circuit c is accessed, and the SCS make the IP core i be in the bypass situation.

B. Wrapper Interface Ports Control Switch

All the IP cores configured the Wrapper in the SoC are controlled by the chip level test control module. During the test process, different test modes and different test sequence for IP cores need different control signals from the chip level test control module, and the IP cores don't need to be tested also can recessive the control signal, the extra signals will produce extra power consumption, the un-test IP cores with extra signals may be in un-safety situation. So it's important to configure the control switch for Wrapper interface ports (WIP) which recessive the control signals. The paper configured WIP control switch (WIP-CS) for all the IP cores, as shown in Fig.2. The WIP-CS can achieve the orderliness for the IP cores test, it has six one-way access circuits, the access enable signals Switch-en (i) is provided by SCR, the WIP-CS input ports connect to WIP-Controller, and the WIP-CS output signals connect to the Wrapper serial control interface ports.

C. TAM-Bus Reuse Switch

The paper adopted TAM-Bus structure for the parallel test of IP cores. In order to make best use of the TAM-Bus width, the paper applied TAM-Bus reuse switch (TBS) to control TAM-Bus state in the parallel test mechanism. The TBS, shown in Fig.3, will support two kinds of work mode, Function mode and Bypass mode. The TBS concludes selector Mux1 and dispatcher Mux2. The Mux2 is applied in the TAM-Bus test vectors input access, and it controlled the test vectors to apply on the current IP core or next IP core; the Mux1 is applied in the test response access, and it controlled the output of the test response for the tested IP core. The input port TAM_Bus_in of the TBS connect to the Wrapper parallel input (Wpi) or next TBS input TAM_Bus_in (i+1) through Mux2; the output port TAM_Bus_out connect to the Wrapper parallel output (Wpo) or next TBS output TAM_Bus_out (i+1) through Mux1. The enable signal Switch-en (i) of Mux1 and Mux2 come from the Switch Control Register (SCR). The higher level of the Switch-en (i) make the IP core in the operational state, and the lower level of the Switch-en (i) make the IP core in the bypass state.

The application of three kinds of switch circuits strengthens the controllability of the test process, and the increase of the test circuit overhead is inevitable. The number of the switch is in direct proportion to the I/O ports of the Wrapper, and the I/O ports conclude the Wrapper serial inputs (Wsi), Wrapper serial outputs (Wso), Wrapper interface ports (WIP), Wrapper parallel inputs (Wpi) and Wrapper parallel outputs (Wpo). For the complicate internal structure of IP cores, the proportion of the limited switch circuits to the whole IP core circuits is lower, so the additional circuits' overhead is small.

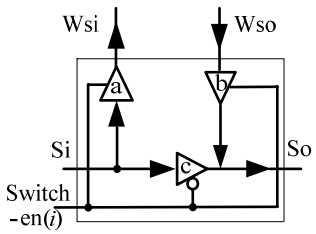

Figure 1. Serial-access Control Switch

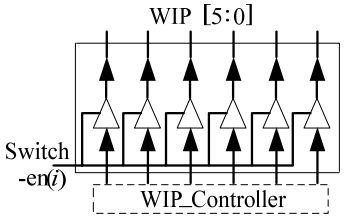

Figure 2. WIP Control Switch

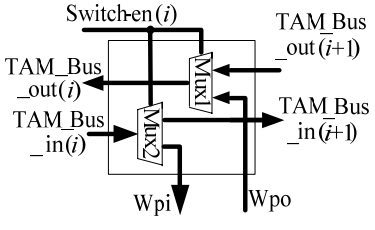

Figure 3. TAM-Bus Reuse Switch

TABLE I.
SCR WORK MODE TRUTH TABLE

Mode	Select-CR	Shift-SCR	Update-SCR	di	do	Clock-SCR	Switch-en	SCRSTN
Shift	1	1	0	sd	sd	clk	×	0
Update	0 (or 1)	1 (or 0)	1	×	Sd	×	sd	0
Reset	×	×	×	×	0	×	0	1

III. SWITCH CONTROL REGISTER OF IP CORES

In the test process of SoC based on IP cores, the paper designed the SCR to control all the switches of IP cores for better controllable test. The SCR module is shown in Fig 4. The main functions of the module are the Shift and Update of the switch control data. The module has three kinds work modes, Shift, Update and Reset, as shown in Table I, which is the truth table of the SCR work mode. In Table I, the sd is the control data of the switch, and the clk is the clock signal. The test process for IP cores is sequential, so the control for all the switches sequential. In the control process of the switches, the SCR should be reset before the input of the new switch control data, and the operation can ensure the validity for the control of all the switches.

The paper configured test switch for all IP cores in SoC. The cascade of all the SCR modules is shown in Fig. 5, it is the chip level switch control register sets (SCRs). The control signals of the SCRs come from the chip level control module eTAP. When the signals Select-SCR and Shift-SCR are in higher level, the SCRs is in the enable situation. And at the same time, the switch situation data was scanned into the SCRs at the rising edge of the Clock-SCR signal. The data input port di and output port do of SCRs connected to the test data input (TDI) and test data output (TDO) of the chip level control module eTAP respectively. The Update operation of the switch situation data was controlled by the higher level of the Update-SCR signal, and the switch situation data applied on the switches of IP cores from the output port Switch-en (i). The number of the IP cores in SoC decided the length of the register SCRs, designers can flexibly control the length of the register SCRs based on the number of IP cores. The signal SCRSTN reset the register SCRs before new switch situation data was scanned into the SCRs.

IV. CHIP LEVEL TEST CONTROL MODULE

A general chip level test controller is required in the test of SoC based on IP cores. There are two facts should be considered for the design of the chip level test controller, one is design of the standard test circuits interface, and another is decreasing the occupation of the chip external pins for test controller. The paper designed the chip level test controller by applying the test access port (TAP) of the IEEE 1149.1 Standard [7-8], which is compatible with the IEEE 1500 Standard. The TAP as the mature technique has been widely used in board level test and complex IC test. In addition, the standard TAP controller has five interface ports, and it will occupy only a few chip pins source.

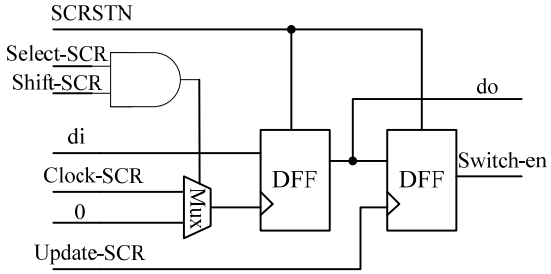

Figure 4. SCR Shift and Update register module

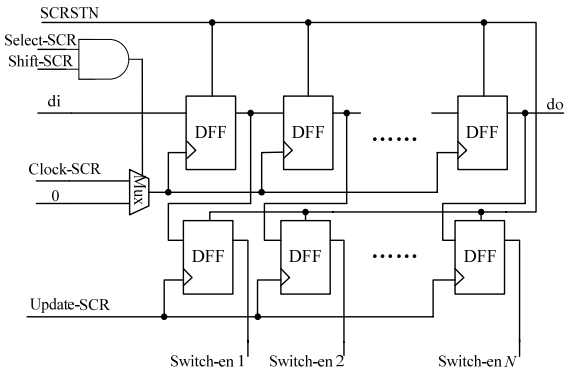

Figure 5. Chip level SCRs for IP Cores

The five test control signals of the TAP controller include test clock signal (TCK), test mode select signal (TMS), test data input signal (TDI), test data output signal (TDO), test reset signal (TRST). All of the test control signals accept the logic level from the external of the chip and generate the output signals. The paper expanded the states of the finite state machine based on maintaining the original states. The Fig 6 shows the chip level test control module, it includes the expanded TAP controller (eTAP), WIP_controller and SCRs. The eTAP controller provided logic control signals for the SCRs and the Wrapper interface ports (WIP).

The eTAP controller signals for SCRs include clock signal SCRCK, reset signal SCRSTN, select control signal SelectSCR, shift control signal ShiftSCR and update control signal UpdateSCR. The eTAP controller signals for WIP include the WIR selection signal SelectWIR, the shift signal ShiftWR, the update signal

UpdateWR, the capture signal WR, the clock signal WRCK and the reset signal WRSTN.

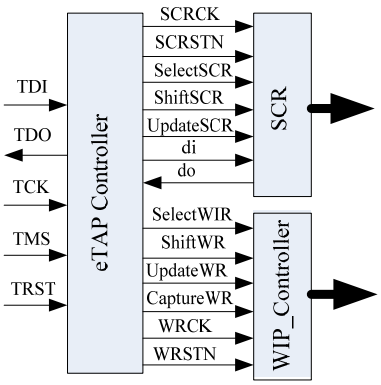

Figure 6. Chip level test control module

The TAP controller is a finite state machine (FSM), which include sixteen states. In order to achieve controllability of the SCR, the paper expanded the FSM, as shown in Fig.7. The eTAP FSM has nineteen states, which are departed into three groups based on state function. The states of Group 1 control the Wrapper data register (WDR) of IP cores; the states of Group2 control the Wrapper instruction register (WIR) of the IP cores; the states of Group3 which is the expanded states control the SCRs. The states of Group1 and Group2 have same function with the original TAP controller FSM, and have the same state transition condition. The SCRs include shift registers and update registers, so the eTAP FSM need to control the update and shift operation of the switch situation data.

V. Design of the Chip Level Test Circuit Structure

The SoC test control mechanism which is the most important part of the chip test is required not only to implement control on the input of the test vectors and the output of the test response, but also to control the test sequence of the Wrapper and the Wrapper external circuits of the IP cores. The simple and controllable test circuit structure is the advantage of the chip level test circuits. The IEEE 1500 Standard standardize the Wrapper circuits of the IP cores, and the TAP of the IEEE 1149.1 Standard as the widely used test technology is compatible with the Wrapper of the IEEE 1500 Standard, so the chip level test control circuits structure improve the test controllability for the SoC.

The paper configured three kinds of switches, the SCS, the WIP-CS and the TBS. The SCS and TBS mainly focus on the control the test vectors and the test response, and the WIP-CS is used to choose the under test IP cores for the chip level test controller. All the switches are configured by the SoC chip level test control module, and the configuration ensured the independent for the test of IP cores and ensured that there is no interference for test states, test date and test sequence of IP cores during the test process.

The SoC chip level test control structure based on IEEE 1500 Standard is shown in Fig. 8, every IP core in Fig. 8 has been configured three kinds of switches, and all the switches has the same enable signal Switch_en, which is provided by the SCR and transported to the switch enable ports by the signal bus Switch_en [1: N]. In the parallel access mechanism, the test Source and test Sink can be provided on the chip or the external chip ATE. In the serial access mechanism, the SCS controlled the input date which include the Wrapper implementation code and the serial test vectors for the Wrapper Boundary Register.

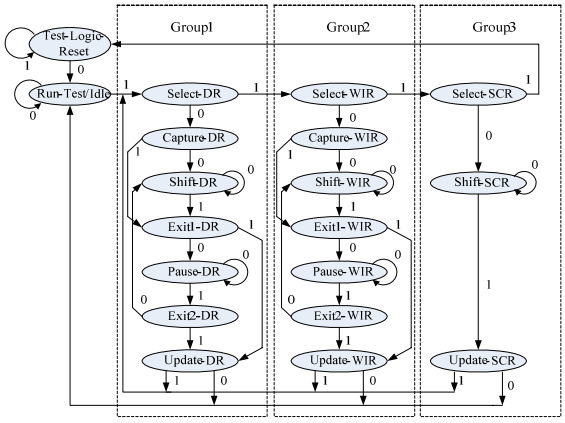

Figure 7. eTAP controller state transition diagram

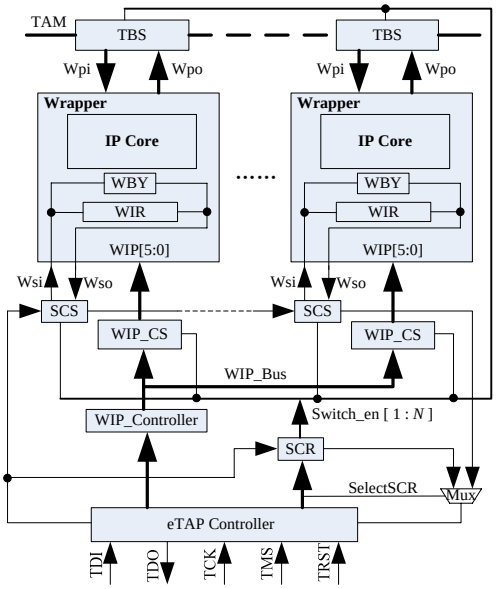

Figure 8. The chip level test control structure

The SoC chip level test control module designed in the paper has few circuits overhead, it only occupied five external pins of the chip. The Test Date Input port TDI of the eTAP directly connected with the date input port di of SCR and date input port Si of SCS, and the Test Date Output port TDO connected with a selector Mux. The control signal port of the Mux is the SelectSCR, when the SelectSCR is in high level, the TDO connected with the date output port do of the SCR, and when the SelectSCR is in low level, the TDO connected with the date output port So of the SCS. The Wrapper serial

control ports WIP [5: 0] of IP core accept the logic signal SelectWIR, ShiftWR, UpdateWR, CaptureWR, WRCK and WRSTN of the WIP_Controller through the signal bus WIP_Bus.

Above all, the chip level eTAP controller finished the input and output of the test date, and achieved the implementation of the test logic signals through the test switch bus Switch_en [1: N], the Wrapper serial port signal bus WIP_Bus, and the parallel access mechanism bus TAM_Bus.

VI. The Application of the Test Architecture

In order to validate the whole test circuit designed in the paper, we applied Verilog HDL to describe the test modules in the paper and adopted the software of the Mentor Graphics Modelsim to complicate the emulation.

First, the signal TRSN made the SCRSTN and WRSTN enable to reset the internal registers of the Wrapper. Then, the chip level control module eTAP made the signal sel_scr in high level to choose the SCR, at the same time, the SCR serially connected between the input port TDI and output port TDO. The paper taken a chip with three IP cores as example, so then the eTAP made the signal shi_scr in high level, the switch situation date 101 was scanned in with the clock signal, as shown in Fig. 9, and the signal date switch_en [2: 0]=101 was output at the falling edge of the clock signal to select the under test cores Core1 and Core3.

The eTAP FSM has nineteen states, so the paper adopted five bit binary code to define all the states. The signal sequence simulation of the SCR and WIP_Controller from the eTAP FSM is shown in Fig. 10. The control sequence included two processes: first process is achieving the sequence control for SCR and configuring all the switches, and the second process is finishing the sequence control for WIR and applying the instruction on the Wrapper. We can see from the Fig. 10 that the update signals Update-SCR of SCR and the UpdateWIR of WIR were enable at the falling edge of the signal TCK. The Fig. 10 is an example simulation for the SCR and the WIR. In the test example, there are three IP cores on the chip, so it required configuring switches of three groups, and the length of the SCR is three bit. First, the eTAP FSM scanned the configuring date 101 into the SCR, the application of the configuring date which is controlled by the Update_scr signal occurred at the falling edge of the TCK. After the configuring of the SCR, the eTAP FSM module input the instruction for the Wrapper of the selected IP cores, so as to control the work mode of the Wrapper registers. The wir_code 1001 in the Fig. 10 presented that the selected IP cores are required to implement parallel test.

VII. Block Model for SoC BIST

The TAM is important part of SoC testing structure, it provides an access to transfer testing data, and it transfers test stimulus from source to inputs of core and transfers test response from outputs of core to response analyzer.

The TAM adopts Testing Bus structure on SoC usually. All the scan data inputs and outputs of IP core are assembled to make up of Testing Bus. Its' beginning is input packaging pins of chip, and its' end is output packaging pins of chip. All these packaging pins reuse the chip function packaging pins. Under testing mode, all these Testing Bus transfer testing data for testing IP cores on chip. Besides, the width of Testing Bus always is determinate, it is decided by the sharing amount of input and output pins on chip and the allowable costs of routing for Testing Bus. Adopting special Testing Bus, makes the function design and testing design separate, accordingly, it makes IP cores testing reuse easily.

For single IP core testing in this paper, the internal circuit of IP core adopts scan chain testing; the external circuit of IP core adopt Self-Testing Using an MISR and Parallel Shift Register Sequence Generator (STUMPS), which is common BIST structure, as shown in Fig.11.

In Fig.11, the Pseudo-Random Pattern Generator (PRPG) generates testing vector, the Phase Shifter can expand the PRPG order when input ports are much more, so it decreases the hardware costs of PRPG. The operation of scan shift is controlled by the Shift Counter, and the vector number of scan testing is controlled by Pattern Counter. The Multiple input Signature Register (MISR) and Space Compactor compress and export testing response. The testing data transfer to MISR through internal scan chain.

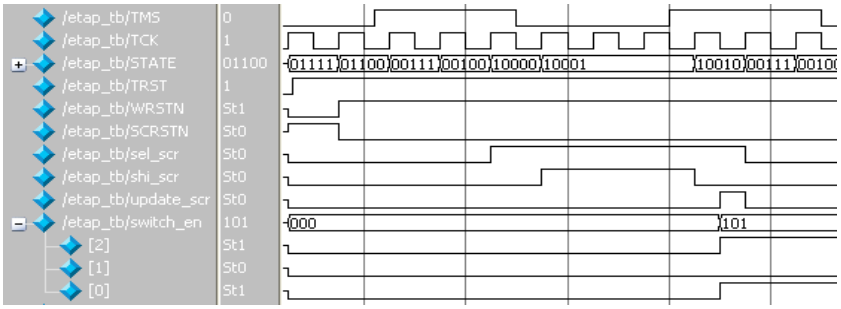

Figure 9. Configuring the switches state

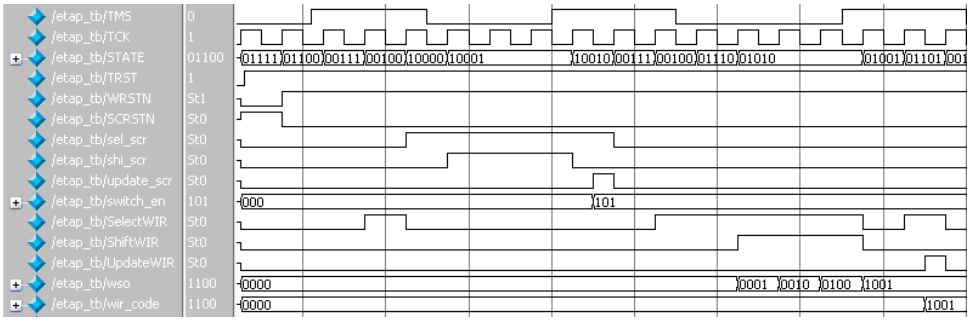

Figure 10. The sequence simulation of test date for the SCR and WIR

For the SoC testing structure within BIST, in order to reduce testing time, all the BIST in the SoC should implement parallel testing, but all the parallel testing simultaneously lead to more peak power. So in order to shorten testing time and reduce testing power, the paper proposes a BIST Block testing model. We assume that the Wrapper has been optimized, determine an assignment for given width of TAMs and partition of all IP cores to every assigned TAM. Every assigned TAM and all the IP cores on the same TAM make up of a Block circuit. In the same Block, IP cores implement serial testing; in different Block, IP cores implement parallel testing.

The Fig.12 presents a Block circuit, it is the NO.i embranchment of TAM partition, and all the IP cores in this figure implement serial testing. The Block circuit adopts STUMPS BIST structure; the PRPG generates testing vectors, and the Signature Generator analyses testing response. The Testing Controller controls PRPG and Signature Generator to implement BIST, and controls the bypass mode in IP cores serial testing.

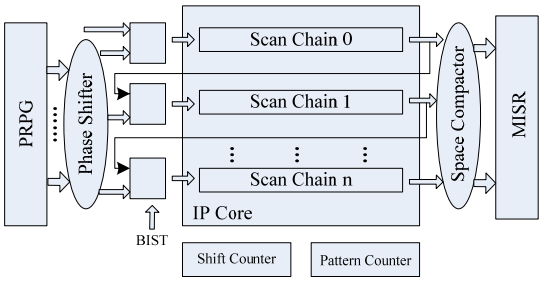

Figure 11. The STUMPS BIST architecture

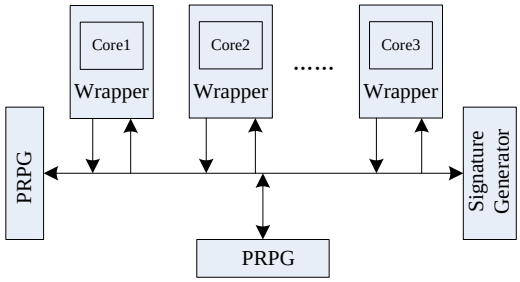

Figure 12. BIST serial testing structure for Block circuit

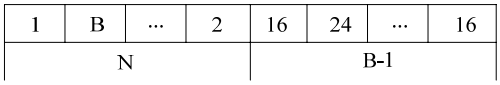

Figure 13. The chromosome coding for problem $P_{PAW-Block}$

VIII. NGA OPTIMIZE PARTITION OF TAM AND IP

Based on the BIST Block idea mentioned in the paper, we present $P_{PAW-Block}$ problem: for a given SoC, its' IP cores number is N, its' TAM number is B, and its' total TAM width is W. Determine a partition of the total TAM width and an assignment of cores to the TAMs, such that SOC testing time is minimized. In the same Block, IP cores implement serial testing, and in different Block, IP cores implement parallel testing, so SoC testing time is decided by the longest Block testing time.

We assume the core Wrapper has been optimized, the problem of optimization partition of TAMs and IP cores is described as follows, first determine the chromosome coding and adaptability function, then discuss the problem of premature convergence of the NGA when working out problem $P_{PAW-Block}$.

The chromosome has two segments, in first segment, the number of N of gene represent all the IP in SoC, gene value is the numbering of assigned TAMs; in the second segment, the number of B-1 of assigned TAMs are seemed as gene, its' gene value is the width of all assigned TAMs. The total width of TAMs is W, so only B-1 TAMs variables are independent. So the chromosome has N+B-1 gene, as shown in Fig.13.

Based on problem $P_{PAW-Block}$, the objective function is

$$MinT = \max_{1 \le j \le B} \left[\sum_{i=1}^{N} T_i(w_j) \times x_{ij} \right] \quad (1)$$

The constraint condition is

$$\sum_{j=1}^{B} w_j = W, w_j \le w_{\max}, 1 \le j \le B \quad (2)$$

If the numbering i IP is assigned to the numbering j TAM, x_{ij} =1; otherwise, x_{ij} =0. The $T_i(w_j)$ represents the testing time of the numbering i IP assigned to the numbering j TAM. The w_j represented every TAM width cannot be bigger than $w_{\max}$ which is the TAM maximum width when IP testing time is minimized. The $w_{\max}$ is decided by the following theorem [1, 3]: An IP core has n function inputs, m function outputs, and sc internal scan chains. The width of its' scan chains is l (i) separately, i=1, 2, …, sc. So when SoC testing time is minimized the TAM maximum width is

$$w_{\max} = \left\lceil [\max(n,m) + \sum_{i=1}^{sc} l(i)] / \max_{i=1,2,\cdots,sc}[l(i)] \right\rceil \quad (3)$$

The $\lceil x \rceil$ represents integer that is not smaller than x. Because it is the minimization problem, so the objective function maps to adaptability function

$$F_{PAW-Block} = T_{\max} - \max_{1 \le j \le B} \left\{ \sum_{i=1}^{N} T_i(w_j) \times x_{ij} \right\} \quad (4)$$

The $T_{\max}$ is the testing time when all IP cores connected to the same rather narrow TAM. This paper optimizes the problem $P_{PAW-Block}$ using a lookup table [3]. The lookup table has been built when all the IP cores has been optimized, it includes all the optimized $T_i(w_j)$.

The NGA is one of Multi-objective Genetic Algorithm. The niche is a kind of organization function in special environment. The same species biota always live together in the evolution process, they live in some determinate region. In each niche, there are some superior cells. The diversity of solutions can be preserved based on NGA. The NGA has great global searching ability; it can avoid the premature phenomena.

We consider the problem $P_{PAW-Block}$, the gene value of TAM chromosome segments affects the individual adaptability, every TAM partition scheme will result in different optimization results, and so a niche exists surrounding every TAM partition scheme. The NGA is preferable to work out problem $P_{PAW-Block}$, it can obtain more local optimal solutions, avoid the premature phenomena, and find global optimal solutions.

The description of NGA for solving $P_{PAW-Block}$:

```
main NGA
{
  Random build M initial colonies to initialize P (0);
  Work out individual adaptability in initial colonies;
  Do descending sort for all individual adaptability, former C (C<M) individuals as crowding members;
  Generation t=0;
  While (terminal conditions T is not satisfy) do
  {
    for i =1 to M do
       P (t) selection operation;
    for i =1 to M /2 do
       P (t) crossover operation;
     for i =1 to M do
       P (t) mutation operation;
     for i =1 to M do
       P (t) adaptability calculation;
     Calculate Hamming distance between C crowding members and new M individuals:
```

$$\left\| X_i - X_j \right\| = \sqrt{\sum_{k=1}^{N+B-1} (x_{ik} - x_{jk})^2} \quad (5)$$

In the (5), the condition is (i=1, 2, …, C ; j=1, 2, …, M);

$$\left\| X_i - X_j \right\| < L \quad (6)$$

When (6) is real, the implement penalty function

$$F_{\min}\left\{X_i, X_j\right\} = \text{Penalty} \quad (7)$$

Equation (7) is to lower adaptability individuals;

```
     Do descending sort for M+C individuals including crowding members, remember former C individuals, and make former M individuals to be new colony;
     for i =1 to M do
     P (t+1) =P (t): t = t+1:
   }
}
```

IX. Experimental Results

For comparing the optimization results of NGA to other algorithms, we adopt ITC'02 Test Benchmarks circuits to simulate the NGA. We chose the widely used SoC d695 circuit to implement simulation. Table II is the optimization results of problem $P_{PAW-Block}$ when B is three.

TABLE II.
NGA Optimization Results (B=3)

Total TAM Width	TAM Width Partition	Core assignment	Testing time
16	2, 6, 8	3, 3, 1, 1, 3, 2, 2, 1, 1, 3	42268
24	17, 5, 2	3, 2, 3, 3, 1, 1, 1, 3, 1, 2	28292
28	16, 8, 4	3, 1, 3, 3, 2, 1, 1, 3, 3, 1	24812
32	18, 9, 5	1, 3, 3, 3, 2, 1, 1, 3, 3, 1	21518
40	17, 18, 5	3, 3, 3, 3, 1, 2, 1, 3, 1, 2	17677
48	20, 23, 5	2, 3, 3, 3, 2, 1, 2, 3, 2, 1	16975
56	38, 18, 5	3, 2, 3, 3, 1, 2, 1, 3, 2, 1	13207
64	19, 35, 10	1, 1, 3, 3, 2, 1, 2, 3, 1, 2	12941

The table III lists every testing time of NGA, GA, ILP, and heuristic algorithm for SoC d695 circuit when B is 3.we can conclude that the testing time of NGA is not longer than the GA, ILP, and heuristic algorithm by comparing the data in table III. Accordingly, the optimization results are superior to other algorithm.

TABLE III.
Optimization Results Of Four Algorithms (B=3)

Total TAM Width	Testing time			
	NGA-TAW	ILP	Heu	GA
16	42268	42568	42952	42268
24	28292	28292	30032	28889
28	24812	*	*	*
32	21518	21566	24851	21518
40	17677	17901	18448	17677
48	16975	16975	17581	16975
56	13207	13207	15510	13795
64	12941	12941	15442	12941

X. Conclusion

The paper designed the test control structure for SoC based on IP cores, which included three kinds of test control switches for IP cores, switch control register, and the chip-level test control module. Finally, the paper verified the test control structure through simulation and the results reflect the effectiveness and practicality of the control structure. The test control structure designed in

the paper is universal for the Wrapper of IP cores based on IEEE 1500 Standard. Specially, the test control switch configured to the Wrapper can accurately control the I/O test date. And the switches protected the test of cores from being sequence interference. The application of the switches and the SCR achieved an efficient test for IP cores with the Wrapper structure based on IEEE 1500 Standard.

In conclusion, in section IX, the experimental result shows that the NGA is superior in optimization partition of IP cores and assignment of TAM than other algorithms. At the same time, the Block model proposed in the paper provides testing data sharing mechanism for multiple IP cores.

ACKNOWLEDGMENTS

This work was supported by the National Natural Science Foundation of China (No. 60861003).

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