Modeling and Novel Modulation of Enhanced Z-source Inverter

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***Abstract*—In this paper, an Enhanced Z-source inverter is proposed. Compared to the traditional Z-source inverter, it can obtain high voltage conversion factor with a short shoot-through duration, and can decrease Z-source capacitor voltage stress significantly. In order to identify its inherent character, the transient modeling of continuous conduction mode (CCM) in dc side is presented. Through the detailed analysis, a right-half-plane zero is found in its control-to–output function. Moreover, an improved control method for the Z-source inverter is proposed in this paper. In comparison with traditional maximum constant boost control method, this improved control method has noticeable advantages. Not only switching frequency can be reduced significantly but also the volume of the Z source can be lessened as a result of six shoot through states per carrier period while obtaining the same voltage boost gain. Simulation and experimental results have demonstrated the validity of small-signal models and the merits of the proposed control method.**

***Index Terms*—small-signal model, signal-flow-graph, non-minimum-phase system, pulse width modulation (PWM), Voltage gain, Z-source inverter.**

I. INTRODUCTION

Traditionally, there is a dc-dc converter in front of the VSI to make it obtain buck and boost ability. However, the dc-dc converter makes this inverter costly and inefficient, and the two stage topologies also cause difficulties in control strategy. Recently, a Z-source inverter [1] which posses both voltage-buck and boost capabilities in one single stage has been used in distributed generation (DG) systems. The ZSI can boost the dc voltage and produce a desired output which is higher than dc bus voltage. In addition it can greatly reduce the output distortion and improve the reliability since dead time is no longer needed and a short circuit across any phase leg is allowed. So, Z-source inverters have been developed in different directions [2-8]. Unfortunately, the traditional voltage fed ZSI has some significant drawbacks such as the discontinuous input current in the boost mode and a high sustaining voltage of the capacitors. Authors in [2] presented the improved Z-source inverters to decrease voltage suppress of the capacitors, and authors in [3-4] improve the voltage boost inversion ability of the Z-source.

The modified Pulse-width-modulation (PWM) controls for the Z-source inverter were investigated in [5-8] to produce the shoot-through in zero states. The simple control method [1] was applied to ZSI for the first time. A maximum boost control was presented to produce the maximum dc voltage at any given modulation index [5]. However, careful analysis has shown that it introduces adverse low-frequency current ripple in inductor. This drawback of the maximum boost control has been overcome by the maximum constant control [6], which could obtain the maximum voltage boost gain while maintain a constant shoot-through duty ratio. But all the control methods above are edge-insertion (EI) PWM, switching frequency is adversely doubled, and additional cyclic logic is needed for realization.

To design controllers for ZSI, some recent publications focused on dynamic modeling and analysis of ZSI [9-11]. Authors in [9] present ac small signal modeling and analysis of ZSC in continuous conduction mode, which can help investigate system characteristics. Authors in [10-11] employ the modeling and design of ZSI to demonstrate that the control to output transfer function has right-half-plane zero which is obtained using signal-flow-graph and state-space-averaged method.

In this paper, we will propose an enhanced Z-source inverter topology with high voltage boost inversion ability. To investigate inherit nature of the Enhanced-Z-Source Inverter; the accurate ac small signal model in CCM based on signal-flow-graph is derived. The RHP zero is also found in the control-to-output transfer function, which indicates a non-minimum-phase characteristic. And a novel modulation of proposed Z-source inverter will be presented to achieve maximum constant voltage boost gain without increasing the switching frequency. Moreover, the component volume will be decreased by increasing the shoot-through states per carrier period. The constrains of the shoot-through

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time in SVPWM will be derived; therefore the maximum shoot-through duty radio can be deduced. Afterwards the operation principle and the merits of the proposed control method will be investigated and verified by simulation and experiments.

II. CONSIDERATION ON ENHANCED Z-SOURCE INVERTER

A Z-Source Inverter

Fig.1 shows the traditional voltage fed ZSI, as described by PENG [1], the Z-source capacitor voltage can be expressed as:

$$V_{C1} = V_{C2} = V_C = \frac{1-D_{sh}}{1-2D_{sh}} V_{in}$$
$$V_{PN} = BV_{in} = \frac{1}{1-2D_{sh}} V_{in} \quad (1)$$

Where, V_{in} is the input dc voltage and D_{sh} is the shoot-through duty ratio. From (1), V_c is higher than V_0 (0< D_{sh}<0.5).

According to Kirchhoff's Current Law, we can also obtain

$$I_D = 2I_L - I_i \quad (2)$$

Since the Diode shuts off in the shoot-through time and conduct in the non-shoot-through time, the ZSI draws discontinuous input current.

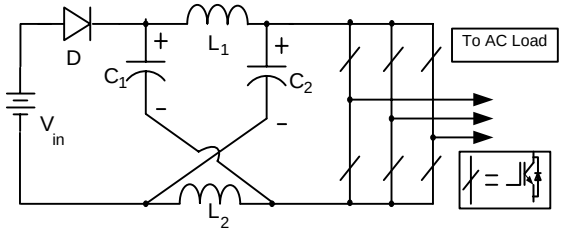


Fig.1 Z-source inverter

B. Enhanced Z-Source Inverter

The Enhanced Z-source inverter is shown in Fig.2. The difference between Z-Source Inverter and Enhanced Z-Source Inverter is inductors. The inductors in enhanced topology are replaced by the switched inductor branches. The first branch is consisted by the two inductors (L_1,L_3) and three diodes (D_1,D_2,D_3), and the second branch is consisted by the two inductors (L_2,L_4) and three diodes ((D_4,D_5,D_6). The energy is stored and transferred by both switched inductors from the capacitors to the dc bus in the switching duration.

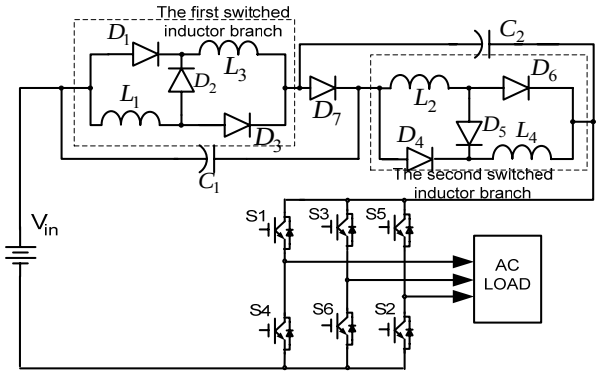


Fig.2 Enhanced Z-source inverter

C. Circuit Analysis

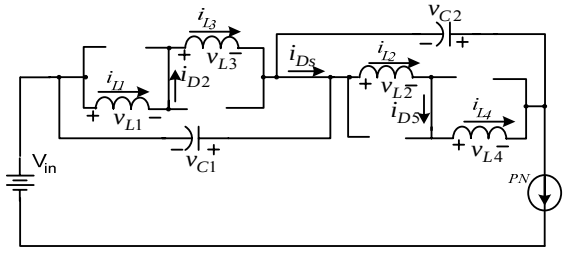
Assuming that L_1=L_2= L_3= L_4=L, C_1=C_2=C, so we can get

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_L, v_{C1} = v_{C2} = v_C \quad (3)$$

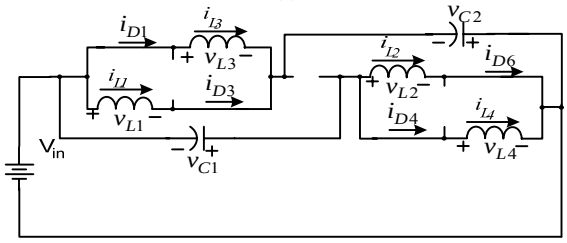
The Enhanced -Z-source inverter also has two types of states: the non-shoot-through state and the shoot-through state. Figs.3(a) and 3(b) illustrate the equivalent circuits of the two states.

When in the non-shoot-through state (including the active and null states) as fig. 3(a), the inverter side can be simplified to be an equivalent current source, one can derive

$$2v_L = -v_C, \quad v_{PN} = 2v_c + V_{in} \quad (4)$$



(a)



(b)

Fig.3 Equivalent circuit of Enhanced Z-source inverter(a) Non-shoot-through state. (b). Shoot-through state.

When in the shoot-through state as fig. 3(b), the inverter side is shorted, one can get

$$v_L = V_{in} + v_C, \quad v_{PN} = 0 \quad (5)$$

Because the average voltage across the inductors over one switching period is zero, we can deduce

$$V_c = \frac{2D_{sh}}{1-3D_{sh}} V_{in} \quad (6)$$

where D_{sh} is the shoot-through duty ratio.

The peak dc-link voltage across the inverter phase legs V_{PN} and peak output phase voltage V_p can be expressed as

$$V_{PN} = 2V_C + V_{in} = \frac{1+D_{sh}}{1-3D_{sh}} V_{in} = BV_{in} \tag{7}$$

$$V_p = M\frac{V_{PN}}{2} = MB\frac{V_{in}}{2} \tag{8}$$

where B is the boost factor and M is the modulation ratio.

III. AC SMALL SIGNAL MOMELS OF QUASI-Z-SOURCE

A. Ac Small Signal Models

As a convenient graphical method which can derive the control-to-output and disturbance-to-output transfer functions with little mathematical manipulations, signal-flow-graph is used here to provide a more comprehensive guide on Z-source impedance modeling [10].

The stray resistances $\{r_1=r_2=r_3=r_4=r\}$ of the Z-source inductors $\{L_1, L_2, L_3, L_4\}$ and equivalent series resistances (ESR's) $\{R_1=R_2=R\}$ of the capacitors $\{C_1, C_2\}$ are taken into consideration, then

$$I_L = \frac{1}{sL+r} V_L$$
$$V_C = (R + \frac{1}{sC}) I_C \tag{9}$$

Representing (3) to (10) graphically after introducing small-signal variations to all state variables, the signal-flow representation is drawn in Fig.4.

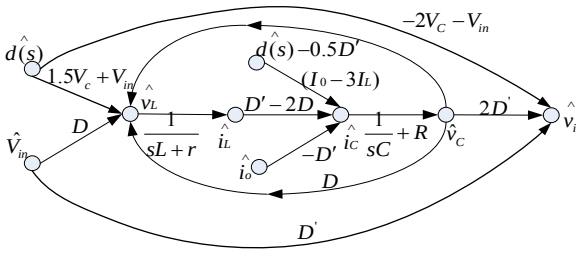


Fig. 4 Graphical signal-flow representation of the quasi-Z-source impedance network

Ignoring the branches of the independent variables $\hat{v}_{in}$, and moving the branch of $\hat{d}$ at the node $\hat{i}_c$, from Fig. 4, applying Mason's gain rule [10], the transfer function between of $\hat{v}_c$ and $\hat{d}$ can be calculated as (10), and the transfer function between of $\hat{v}_c$ and $\hat{v}_{in}$ can be calculated as (11).

According to (9), the simplified system block diagram can be built as Fig. 5, which is very useful in designing the controllers.

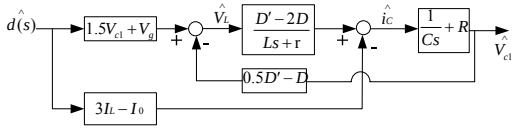


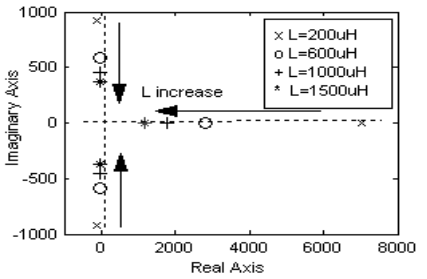
Fig.5 Block diagram representation of the quasi-Z-source impedance network

As expected, Small signal model investigations are paramount to the optimization of parameters of the Z-source networks.

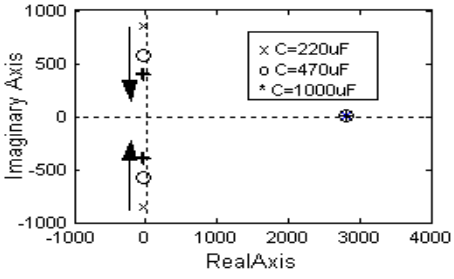
B. Theoretical Analysis based on Models

There is one RHP zero in (10), and any system having an odd number of open-loop RHP zeros is identified by its initial inverse response (undershoot) to a step input. It limits the bandwidth of the closed loop because the crossover frequency needs to be well below the frequency due to the RHP zero, which makes the system dynamics slow [12].

The RHP zero and pole location in the s-domain move following with the Enhanced Z-source parameters (r, R, L and C) and control input D_{sh} variations. These movements would result in unsatisfactorily oscillatory and non-minimum-phase response especially for DG sources, where D_{sh} is controlled to change from 0 to 0.3. For example, when $V_{dc}=150V$, $C=470u$, $R_0=115\ \Omega$, $L=350uH$, $r=0.05$, $R=0.02$, $D_{sh}=0.2$, $f_s=7.2kHz$, the various root and pole locations are plotted by changing a particular parameter with the others kept constant. With the Enhanced Z-source inductance L changes from 200u H to 1500uH, Fig. 6(a) indicates that both zeros and poles are coming toward the origin along the real axis with the increasing of the inductors.



(a)



(b)

Fig. 6: Pole-zero locus of the control-to-capacitor-voltage function in (10) with different parameters of the Enhance Z-source inverter-Z-source (a) L and (b) C.

$$G_{vd} = \frac{\hat{v}_C}{\hat{d}_0} = \frac{[(1.5V_C + V_{in})(D' - 2D) - (3I_L - I_0)(sL + r)](1 + RCs)}{LCs^2 + \left[r + 0.5R(D' - 2D)^2\right]Cs + 0.5(D' - 2D)^2} \tag{10}$$

$$G_{vg} = \frac{\hat{v}_C}{\hat{v}_{in}} = \frac{D(1 + RCs)}{LCs^2 + \left[r + 0.5R(D' - 2D)^2\right]Cs + 0.5(D' - 2D)^2} \tag{11}$$

Noticeably, the undershoot becomes severe as the RHP zero is close to the origin [10]. The settling time turns longer and oscillatory is aggravated with the increasing of the inductors L. By varying the Enhance Z-source capacitance C from 220*uF* to 1000*uF*, Fig. 6(b) shows the shifting of poles vertically towards origin, while RHP zero stays relatively undisturbed. Although the RHP zero position stays unchanged, the shifting of poles is considered to increase rise-time and decrease oscillation frequency.

These trajectories obviously show that large *L* and *C* conduce to low steady-state voltage and current ripples, but they give rise to inferior transient (longer rise-time and settling time) response, and a compromising approach must be taken depending on the particular applications.

The shoot-through duty ratio is an important control parameter for the qZSC, which ultimately determines the dc-link boost capability. As has been discussed, expression (10) describes how control input variations influence the output voltage. Fig. 7 shows the pole-zero map of G_{vd} with various shoot-through ratios (0.1, 0.15, and 0.3). We can find that pole placement move towards the real axis indicating an inferior transient response, while the zero placement moves towards the origin manifesting an increase in non-minimum-phase under-shoot.

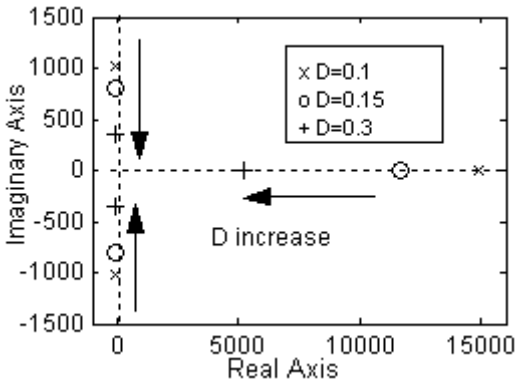


Fig.7: Pole-zero locus of the control-to-capacitor-voltage function in (16) with different shoot-through duties ratios.

IV THE MODIFIED MXIMUM CONSTANT BOOST CONTROL

A The Maximum Constant Boost Control

The maximum constant boost control [6] is shown in Fig.7, which can obtain the maximum voltage gain at any given modulation index and overcome the low-frequency current ripple of the maximum boost control [5]. There are five curves in this control method: three reference signals V_a, V_b, V_c , and two shoot-through envelope signals V_p and V_n .

As shown in Fig.7, V_a reaches its peak value $(\sqrt{3}/2)M$ while V_b is at its minimum vale $-(\sqrt{3}/2)M$ at $\pi/3$. So the upper and lower envelope curves are easily obtained.

$$V_p = \frac{\sqrt{3}}{2}M, V_n = -\frac{\sqrt{3}}{2}M \tag{12}$$

where *M* is the modulation index. The shoot-through zero states happen when the carrier triangle wave is higher than the upper shoot-through envelope V_p or lower than the bottom shoot-through envelope V_n .

Obviously, under a given modulation index M, the distance between these two curves is kept as a constant $\sqrt{3}M$. This indicates that the shoot-through duty ratio is constant and can be expressed as:

$$D_0 = \frac{T_0}{T} = \frac{2 - \sqrt{3}M}{2} = 1 - \frac{\sqrt{3}M}{2} \tag{14}$$

Where D_0 is the shoot-through duty ratio, T_0 is the shoot-through time, T is the switching cycle. This is different from the maximum boost control where D_0 varies periodically resulting in low-frequency current ripple.

The boost factor *B* and the voltage gain *G* can be calculated as follows:

$$B = \frac{1}{1 - 2D_0} = \frac{1}{\sqrt{3}M - 1} \tag{15}$$

$$G = MB = \frac{M}{\sqrt{3}M - 1} \tag{16}$$

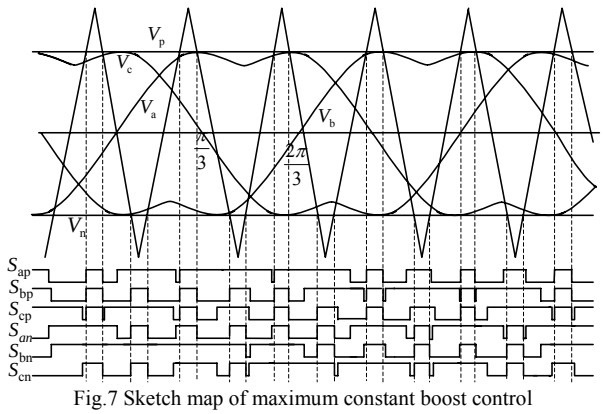


Fig.7 Sketch map of maximum constant boost control

The improved maximum constant boost method will be proposed basing on SVPWM and employing advantages

from both the traditional maximum constant boost method and the modified reference PWM.

B Zero States Time of SVPWM

Switching states of a conventional SVPWM is shown in Fig.8 and the algorithm for the conventional SVPWM of VSI is briefed as follows (section I).

Time for active voltage vector is

$$T_1 = \sqrt{3}\frac{V_{ref}}{V_{dc}}T_s \sin(\frac{\pi}{3}-\theta)$$
$$T_2 = \sqrt{3}\frac{V_{ref}}{V_{dc}}T_s \sin\theta \qquad (0<\theta<\pi/3) \tag{17}$$

The reference voltage vector V_{ref} can be expressed as

$$V_{ref} = (V_1T_1 + V_2T_2)/T_s \tag{18}$$

The null-states time T_N can be calculated as

$$T_N = T_s - T_1 - T_2 = T_s - \sqrt{3}\frac{V_{ref}}{V_{dc}}T_s \sin(\frac{\pi}{3}+\theta) \tag{19}$$

So the minimum null-states time is

$$T_{N\min} = T_s - \sqrt{3}\frac{V_{ref}}{V_{dc}}T_s \quad (\theta=\pi/6) \tag{20}$$

C The Improved Maximum Constant Boost Control

Shoot-through states are inserted in null intervals, so under the prerequisite of maintaining active intervals constant, the maximum shoot-through intervals is $T_{N\min}$, then maximum shoot-through duty ratio can be express as

$$D_{\max} = \frac{T_{N\min}}{T_s} = 1 - \frac{\sqrt{3}}{2}m \tag{21}$$

Where $m = 2V_{ref}/V_{dc}$

If the shoot-through duty ratio we chose is just equal to $D_{\max}$, we will get the same effect as the maximum constant control.

The shoot-through time T_0 is

$$T_0 = (1-\frac{\sqrt{3}}{2}m)T$$
$$D_0 = D_{\max} = 1 - \frac{\sqrt{3}}{2}m \tag{22}$$

The boost factor B and the voltage gain G can be calculated as follows

$$B = \frac{1+D_0}{1-3D_0} = \frac{4-\sqrt{3}M}{3\sqrt{3}M-4} \tag{23}$$

$$G = \frac{U_m}{V_0/2} = MB = \frac{4-\sqrt{3}M}{3\sqrt{3}M-4}M \tag{24}$$

Where U_m is the output peak phase voltage, Equation (24) shows that the voltage gain is determined by the modulation index. Obviously, the proposed improved modulation strategy can achieve maximum constant effects for equation (23) and (24) is constant with equation (15) and (16). With (22)-(24), we can get

$$D_{sh} = \frac{3\sqrt{3}G - \sqrt{27G^2 - 8\sqrt{3}G + 16}}{4} \tag{25}$$

$$M = \frac{4 - 3\sqrt{3}G + \sqrt{27G^2 - 8\sqrt{3}G + 16}}{2\sqrt{3}} \tag{26}$$

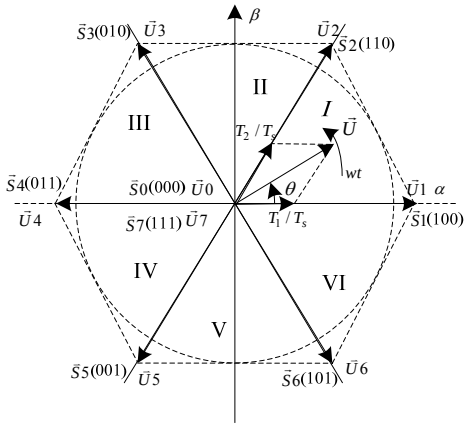


Fig.8 Voltage vector through conventional SVPWM of VSI

With equation (25)-(26), the shoot-through ratio and modulation index can be calculated by input voltage V_0 and output peak phase voltage U_m.

Fig.9 shows the proposed modified SVPWM for ZSI in section I.

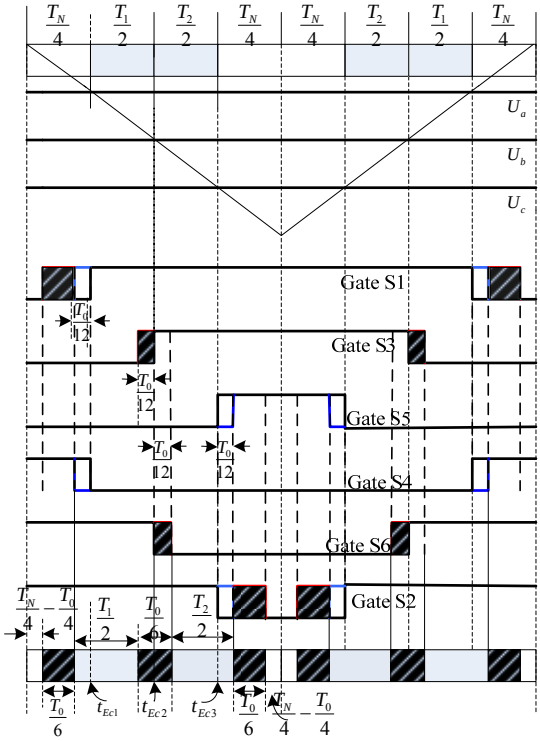


Fig.9 Improved maximum constant control in section I

The first inserting shoot-through state occurs when the upper switch S1 is turned on at ($t_{Ec1}-T_0/4$), while the shoot-through is ended by the lower switch S4 turned off at ($t_{Ec1}-T_0/12$).Here, the $T_0/12$ motion is to make sure that the third insertion has equal utilization time as the first one, and then a $T_0/6$ shoot-through time is inserted. The second one starts at the time of the upper switch S3 is turned on at ($t_{Ec2}-T_0/12$), and ends by the lower switch turned off at ($t_{Ec2}+T_0/12$), then a $T_0/6$ shoot-through time is created. And the third one happens when the upper switch S5 turns on at ($t_{Ec3}+T_0/12$) and ends after the lower switch turning off at ($t_{Ec3}+T_0/4$).In this part, the $T_0/12$ motion is to keep the active state as before and the residual part is the shoot-through time. The switching time of the upper switches and lower switches in a three-phase inverter is summarized in Table I below.

TABLE 1

SWITCH TIME DURATION AT EACH SECTOR

Sector	Upper(S1,S3,S5)	Lower(S4,S6,S2)
1	$S_1=T_1+T_2+T_N/4+T_0/4$ $S_3=T_2+T_N/4+T_0/12$ $S_5=T_N/4-T_0/12$	$S_4=T_N/4-T_0/12$ $S_6=T_1+T_N/4+T_0/12$ $S_2=T_1+T_2+T_N/4+T_0/4$
2	$S_1=T_2+T_N/4+T_0/12$ $S_3=T_1+T_2+T_N/4+T_0/4$ $S_5=T_N/4-T_0/12$	$S_4=T_1+T_N/4+T_0/12$ $S_6=T_N/4-T_0/12$ $S_2=T_1+T_2+T_N/4+T_0/4$
3	$S_1=T_N/4-T_0/12$ $S_3=T_1+T_2+T_N/4+T_0/4$ $S_5=T_2+T_N/4+T_0/12$	$S_4=T_1+T_2+T_N/4+T_0/4$ $S_6=T_N/4-T_0/12$ $S_2=T_1+T_N/4+T_0/12$
4	$S_1=T_N/4-T_0/12$ $S_3=T_2+T_N/4+T_0/12$ $S_5=T_1+T_2+T_N/4+T_0/4$	$S_4=T_1+T_2+T_N/4+T_0/4$ $S_6=T_1+T_N/4+T_0/12$ $S_2=T_N/4-T_0/12$
5	$S_1=T_2+T_N/4+T_0/12$ $S_3=T_N/4-T_0/12$ $S_5=T_1+T_2+T_N/4+T_0/4$	$S_4=T_1+T_N/4+T_0/12$ $S_6=T_1+T_2+T_N/4+T_0/4$ $S_2=T_N/4-T_0/12$
6	$S_1=T_1+T_2+T_N/4+T_0/4$ $S_3=T_N/4-T_0/12$ $S_5=T_2+T_N/4+T_0/12$	$S_4=T_N/4-T_0/12$ $S_6=T_1+T_2+T_N/4+T_0/4$ $S_2=T_1+T_N/4+T_0/12$

D The Switching Frequency

The switching frequency of the modified constant boost control is only half in comparison with the traditional constant boost control because every switch in Fig.9 switches once per half carrier period, while the switch in Fig.7 switches two times. The switching frequency of this method is same as the modulation of traditional VSI,

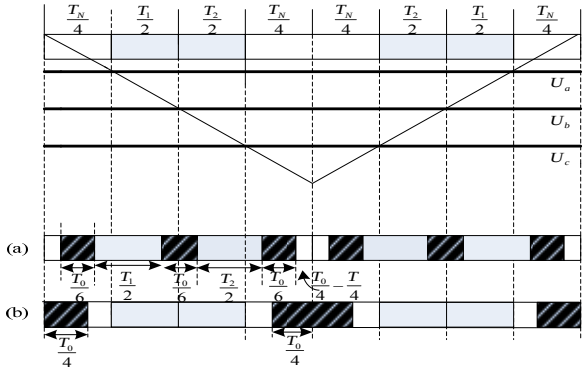


Fig.10(a) The switching pattern for Improved maximum constant control
(b) Sketch map of traditional maximum constant boost control

Therefore, the Z-source inverter is applicable to circumstances with higher carrier frequency without constrains set by switching frequency limitation.

E The Inductor Current Ripple

The inductor current ripple can be expressed

$$\Delta i_L=\frac{D_0TV_{C1}}{L}=\frac{D_0(1-D_0)V_{in}}{(1-2D_0)fL} \tag{27}$$

Where, *f* is the charging frequency. In Fig.10, there are six shoot-through states in (a) while there are two shoot-through states in (b). Therefore the charging frequency of inductor in Fig.10 (a) is three times higher than that of Fig.10 (b). So from (27), we can conclude that the inductor current ripple (a) is much smaller than (b) in the same conditions.

V SIMULATIONS RESULTS

The ac small signal model is simulated in a MATLAB environment along with SIMULINK and power-system-blockset (PSB) toolboxes. Figs. 11 show the simulation results of subjecting to a step change of shoot through ratio ranging from 0.1 to 0.11 by the detailed switching circuit mode (Fig.2) and small–signal model Fig.4. Here, 0.01 is the disturbance of the D_{sh}, which is used to obtain the transient response of the model. From Fig. 11, we can obtain that the transient response of small-signal model is consistent with that of the detail circuit. Therefore the inherent character of the Enhance Z-source inverter impedance network can be described successfully by the small-signal model. However, the values of inductance and capacitance we choose are so minor that the under-shoot is not obvious here.

In order to illustrating the non-minimum-phase undershoot product by the right-half-zero, Fig.12 shows the simulate z-source capacitor voltage response of step D_0 transition. The simulate result clearly illustrates an initial voltage dip before rising, hence confirming the dc-side non-minimum-phase nature, as predicted theoretically.

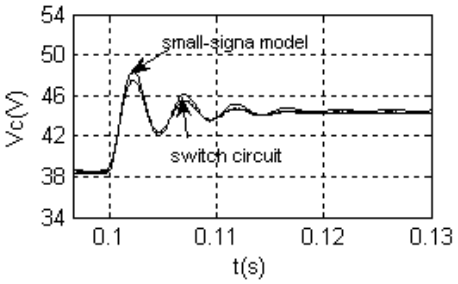


Fig.11 Simulation results of Enhance Z-source inverter output to a step change of D_0 at t=0.1s

To verify the control strategies with reduced voltage stress cross devices, simulations were performed in Matlab/Simulink. The parameters are given:

1）Z-source network: L_1=L_2=1.0mH, C_1=C_2=470μF

2) Output filter: L_2=3.5mH, C_f=10μF

3）switch frequency : 7.2 kHz.

4) load: three-phase resistance load R=43Ω.

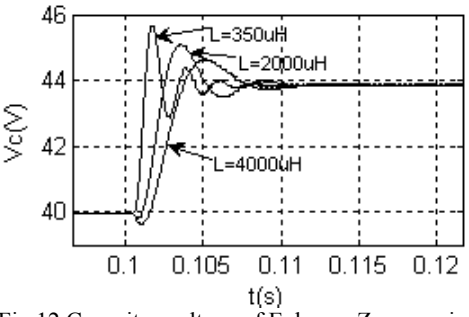


Fig.12 Capacitor voltage of Enhance Z-source inverter subject to a step change of shoot-through duty at t=0.1s with different inductances

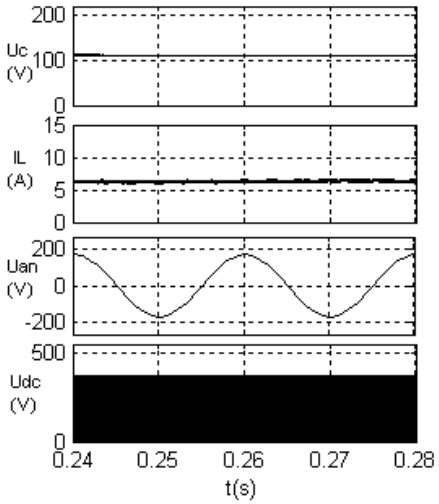


Fig.13 Simulation results with M =0.94 and input voltage 145Vdc

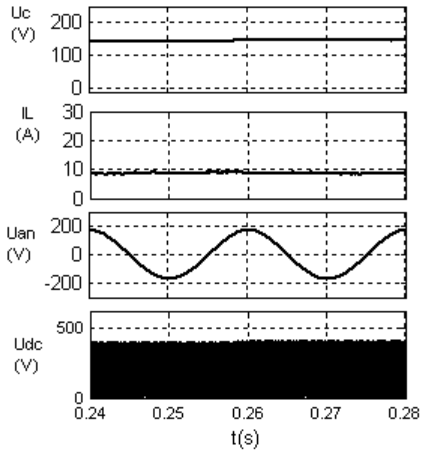


Fig.14 Simulation results with M =0.91 and input voltage 110Vdc

The purpose of the system is to compare the performance of the Z-source inverter under different input voltage and similar output three-phase voltage of around 208V rms. The simulation results at input voltage level 110V, and 145V are shown in Fig13-14, respectively. The corresponding modulation indexes are $M = 0.91, M = 0.94$ respectively.

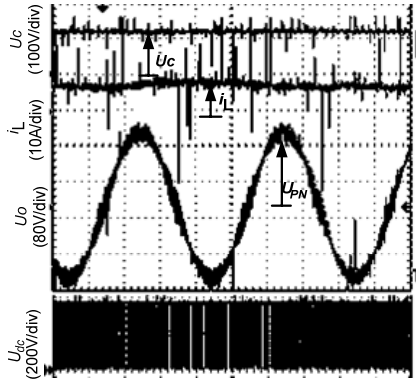
In the simulation results, V_c is the capacitor voltage, V_{dc} is the dc bus voltage, which is also the voltage stress V_s , and V_{an} is the output voltage after the filter. Based on the analysis above, the theoretical voltage stress and output line to phase peak voltage are listed in Table II. From Fig.13-14, the capacitor voltage is only about 110V and 150V respectively. And the voltage stress in Fig.14 is higher than the one in Fig.13. So the results are quite consistent with the theoretical analysis, which verifies the above analysis and the control concept.

TABLE II.
CAPACITOR VOLTAGE, THEORETICAL VOLTAGE STRESS AND OUTPUT VOLTAGE UNDER DIFFERENT CONDITIONS

Operation condition	Capacitor voltage	Voltage stress	Output voltage
M=0.94,V0=145V	106V	350V	170V
M=0.91, V0=110V	142V	390V	170V

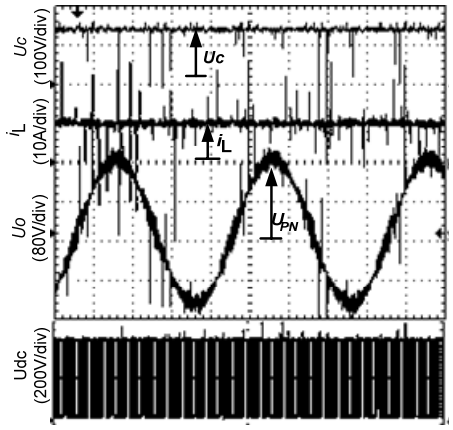
VI EXPERIMENTAL VERIFICATION

The parameters used in the experiment and simulations are identical. The prototype is also used to verify the design issues discussed above. The experimental results with the same conditions are shown in Figs.15-16, respectively. The voltage of capacitor is below 200V and the voltage stress is same to that of the maximum constant boost control. And the results agree well with simulation results.



t (5ms/div)

Fig.15 Experimental results with M =0.94 and input voltage 145Vdc



t (5ms/div)

Fig.16 Experimental results with M =0.91 and input voltage110Vdc

VII. CONCLUSIONS

This paper has presented a novel Z-source inverter topology. Comparing with the previous Z-source inverters, the enhanced Z-source has the advantage of high voltage boost inversion ability and low Z-source capacitor voltage stress. Signal-flow-graph is used to develop a small-signal model of Enhance Z-source inverter for further dynamic state investigation. This model illustrates that the output voltage has a non-minimum-phase response as a RHP zero exited in its control-to-output transfer function. A modified maximum constant boost method has also been presented. Compared with the previous maximum constant boost method, the switching frequency is reduced resulting in lower turn off loss in the same voltage boost gain condition. And it can greatly reduce the *L* and *C* volume in the Z-network. In the end, simulation and experimental results have verified the merits of the proposed method.

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