High-Speed Low-Power MCML Nanometer Circuits with Near-Threshold Computing

Jianping Hu, Haiyan Ni, and Yinshui Xia
Faculty of Information Science and Technology, Ningbo University, Ningbo City, China
Email: nbhjp@yahoo.com.cn

Abstract—In this paper, the standard cells of the high-speed low-power MCML circuits with near-threshold computing are developed. The basic MCML standard cells include buffer/inverter, AND/NAND, XOR/XNOR, multiplexer, and full adder. The layout, abstract design and standard-cell characters of near-threshold MCML basic cells are described at a NCSU FreePDK 45nm technology. The 2-bit multiplier is verified by using the MCML cells. For normal supply voltage, the MCML basic gates can save more energy and have better performance than the traditional CMOS counterparts at 1GHz or higher operation frequencies. Near-threshold computing for MCML circuits is investigated by scaling down the supply voltage. The results show that the power consumption of MCML circuits that operate on near-threshold regions can be reduced without performance degrading.

Index Terms—nanometer circuit, near-threshold computing, MOS current-mode logic, low power, high-speed operating

I. INTRODUCTION

MOS current mode logic (MCML) techniques could be used to realize high-speed circuits [1]. Therefore, MCML is usually used for high-speed applications such as high-speed processors and Gbps multiplexers for optical transceivers [1, 2]. The circuits designed with the MCML techniques can operate over a wide range of frequencies [3]. Moreover, MCML has low noise level due to constant current flowing through supply rails and low crosstalk because of small logic swing. Another interesting advantage of this technique is that their speed and power consumption can be simply adjusted by altering the bias current of the gates without the need for resizing the devices. Therefore, MCML is very suitable for mixed mode integrated circuits in order to reduce the digital interference between the analog and digital blocks.

MCML has large static power consumption due to its constant operation current. Recently, the low power MCML designs have obtained quite some attentions [4-7]. P. Heydari and G. Caruso presented the methodologies for the low-power design of MCML-based buffer chain and ring oscillators, respectively [4, 5]. Mohab H. Anis et al. proposed the multi-threshold MCML (MTMCML) technology that allows the reduction of the minimum supply voltage of the two-level MCML circuits, thus to lower the power dissipations of the MCML circuits [6]. However, the analysis for MTMCML presented in [6] was based on inaccurate long-channel modeling equations, which is inappropriate for today’s nanometer CMOS technologies. In [7], H. Hassan et al. presented a comprehensive MTMCML analytical formulation based on the BSIM3v3 model.

In this work, the standard cells of the high-speed low-power MCML circuits with near-threshold computing are developed. The basic MCML standard cells include buffer/inverter, AND/NAND, XOR/XNOR, multiplexer, and full adder. The layout, abstract design and standard-cell characters of near-threshold MCML basic cells are described at a NCSU FreePDK 45nm technology. The 2-bit multiplier is verified by using the proposed MCML cells. Near-threshold computing for MCML circuits is investigated by scaling down the supply voltage. The results show that the power consumption of MCML circuits that operate on near-threshold regions can be reduced without performance degrading.

II. OPERATION OF MCML CIRCUITS AT NORMAL SUPPLY VOLTAGE

The basic MCML buffer/inverter and its bias circuit are shown in Fig. 1. The MCML inverter is composed of three main parts: the load transistors P1 and P2, the full differential pull down switch network consisting of N1 and N2, and the current source transistor Ns. The load transistors are designed to operate at a linear region with the help of the control voltage $V_{rfp}$ produced by the bias circuit, which also controls the output logic swings [8]. The pull-down network (PDN) NMOS N1 and N2 are used to perform logic operation. The NMOS Ns is used to provide the constant current source, which is mirrored from the current source in the bias circuit. In the MCML, the two signals $V_{rfp}$ and $V_{rfn}$ are generated from the bias circuit to ensure the proper operating for output voltage swings and to provide the constant bias current.

![Figure 1. MCML Buffer/Inverter and its bias circuit.](image-url)
MCML is a type of differential logic with differential input logic tree. Therefore, the design of the MCML PDN is similar to other differential logic styles such as DCVSL and DSL [9]. The complex logic functions can be realized by replacing N1 and N2 of the buffer/inverter shown in Fig. 1 with NMOS logic trees.

The MCML AND2/NAND2, XOR2/XNOR2 and 2-1 MUX are shown in Fig. 2. Fig. 2 (a) is also called as MCML universal logic gate, since it can realize the basic two-input logic functions (AND2/NAND2, and OR2/NOR2). The additional transistor N5 improves the symmetry of the universal gate, thus to improve the performance of the MCML gate in high-speed applications [10].

The more complex logic functions can be also realized by replacing N1 and N2 with NMOS logic trees, which is similar to DCVSL circuits. The three-input AND3/NAND3 and XOR3/XNOR3 based on MCML techniques are shown in Fig. 3.

The operation of MCML is performed in the current domain. The pull down network switches the constant current between two branches, and then the load converts the current to output voltage swings. The high and low digital logic levels are $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - I_B R_D$, respectively, where $R_D$ is the PMOS load resistance. The logic swing $\Delta V = V_{OH} - V_{OL} = I_B R_D$.

III. LAYOUTS OF MCML CIRCUITS AND AREA COMPARISONS

In order to show energy efficiency and performance of the MCML circuits, the MCML basic gates have been realized with the NCSU FreePDK 45nm technology. Full-custom layouts are drawn. Fig. 4 shows the layout of the MCML two-input basic gates including Buffer/Inverter, AND2/NAND2, XOR2/XNOR2 and 2-1 MUX.
The layouts of the MCML three-input AND3/NAND3 and XOR3/XNOR3 are also realized, which are shown in Fig. 5. Fig. 6 shows the layout of the 1-bit full adder based on MCML.
The layout areas among NCSU FreePDK45nm OSU_SOC library, Nangate 45nm Open Cell library, and MCML Cell library have been compared, as shown in Table I.

<table>
<thead>
<tr>
<th>Cell</th>
<th>Area (μm²×μm)</th>
<th>NCSU FreePDK45nm osu_soc library</th>
<th>Nangate 45nm Open Cell Library</th>
<th>MCML Library</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>0.57×2.47</td>
<td>0.38×1.4</td>
<td>0.95×3.42</td>
<td></td>
</tr>
<tr>
<td>NAND2</td>
<td>0.76×2.47</td>
<td>0.57×1.4</td>
<td>1.52×3.42</td>
<td></td>
</tr>
<tr>
<td>AND2</td>
<td>1.14×2.47</td>
<td>0.76×1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NAND3</td>
<td>0.95×2.47</td>
<td>0.76×1.4</td>
<td>1.71×3.42</td>
<td></td>
</tr>
<tr>
<td>AND3</td>
<td></td>
<td>0.95×1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XOR2</td>
<td>1.71×2.47</td>
<td>1.14×1.4</td>
<td>1.33×3.42</td>
<td></td>
</tr>
<tr>
<td>XOR3</td>
<td></td>
<td></td>
<td>2.09×3.42</td>
<td></td>
</tr>
<tr>
<td>2:1 MUX</td>
<td>1.52×2.47</td>
<td>1.33×1.4</td>
<td>1.33×3.42</td>
<td></td>
</tr>
<tr>
<td>Full adder</td>
<td>3.61×2.47</td>
<td>3.04×1.4</td>
<td>3.99×3.42</td>
<td></td>
</tr>
</tbody>
</table>

IV. POST-LAYOUT SIMULATIONS OF MCML CIRCUITS AT NORMAL SUPPLY VOLTAGE

The optimization performance metrics of the MCML gates mainly include propagation delay, power dissipation and power-delay product [11-13]. Due to the operating constant current whenever it is either in activate mode or in standby mode, the power consumption of a MCML gate is independent of the switching frequency, and it can been written as

\[ P_{MCML} = V_{DD} \times I_B, \quad (1) \]

where \( V_{DD} \) is the supply voltage, and \( I_B \) is the bias current of the MCML gate.

The delay time of a MCML gate can be calculated assuming that, at each transition, the whole \( I_B \), ideally, flows through one branch of the differential pair and charges the total load capacitance \( C \), is given by

\[ t_d = 0.69 \cdot RC = 0.69 \cdot \frac{C \cdot \Delta V}{I_B}, \quad (2) \]

where \( I_B \) is the operating constant current, \( R \) is the equivalent resistance of one branch of the load PMOS transistor, \( C \) is identical load capacitance on an output node, and \( \Delta V \) is the output voltage swing that is generated from the bias circuit.

The power-delay product is independent of the switching frequency and can be calculated as

\[ PDP = P_{MCML} \times t_d = 0.69V_{DD} \times \Delta V \times C. \quad (3) \]

For given source voltage \( V_{DD} \) and bias current \( I_B \), the power dissipation of MCML gates is a constant value. It is independent of both the operation frequencies and fanouts. Therefore, the power of MCML gates is also independent of the logic function. The power dissipation of conventional CMOS circuits can be expressed as

\[ P_{CMOS} = fV_{DD}^2C_L, \quad (4) \]

where \( f \) is operation frequency of conventional CMOS circuits, and \( C_L \) is load capacitance of conventional CMOS circuits. The power dissipation of CMOS circuits depends on the operation frequency linearly. Therefore, there exists a cross-frequency, above which a MCML circuit is more power efficiency than the conventional one.

It is important to estimating the cross-frequency for using effectively MCML circuits from the power efficiency point of view. There is a simple method to estimate the cross-frequency according to the power dissipations of the MCML and conventional CMOS gates. When PCMOS=PMCML, the cross-frequency \( f_c \) can be derived as

\[ f_c = \frac{I_B}{V_{DD}C_L}. \quad (5) \]

It is assumed that the MCML and conventional CMOS circuits operate in the same supply voltage. According to (5), the cross-frequency \( f_c \) can be estimated. The power dissipation and power-delay product can be optimized from (1) – (3).

An optimization has been carried out for the MCML basic cells at the NCSU FreePDK 45nm technology. Post-layout simulations have been carried out using HSPICE, and full parasitic extraction is done. Fig. 7 shows comparison results of the energy dissipation of the basic gates per operating cycle among the NCSU FreePDK45nm OSU_SOC library, Nangate Open cell library, and MCML cell library. The operation frequency is 2GHz, and the supply voltage is 1.0V.

From Fig. 7, it can be seen that the power dissipation of MCML basic gates is the smallest among the three cell libraries. Moreover, the power dissipations of all MCML basic gates such as inverter, AND2/NAND2, MUX2, and XOR2/XNOR2 are almost the same, and independent of their logic structure.

The power dissipation of the XOR2/XNOR2 gates based on MCML and conventional CMOS circuits at different operation frequencies is shown in Fig. 8 at the NCSU FreePDK 45nm technology and 1.0V supply voltage. As the operation frequency rises from 10KHz to 2GHz, the power dissipations of the traditional CMOS basic cells increase rapidly, while the MCML cell keeps a constant value.

From Fig. 8, the cross-frequency \( f_c \) is about 1GHz. When the MCML cells operate at higher frequencies than 1GHz, their power dissipation is lower than the traditional CMOS cells. This character of MCML circuits makes it fit for high-speed applications.
V. NEAR-THRESHOLD COMPUTING FOR MCML CIRCUITS

Power dissipation of the MCML circuits is equal to $V_{DD} \times I_B$, where $V_{DD}$ is the supply voltage and $I_B$ is the current flowing through the constant current source. Therefore, the power dissipation of the MCML circuits can be saved by reducing either $V_{DD}$ or $I_B$. Reducing $I_B$ would result in the increase of delay time and the decrease of the logic swings. Therefore, reducing the supply voltage is an effective method to lower the power consumption of the MCML circuits.

HSPICE simulations have been carried out for the MCML circuits by varying the source voltage from 1.0V to 0.6V. Fig. 9 shows the energy dissipations of XOR2 based on MCML and conventional CMOS circuits at different supply voltages. From the curves, we can see that the energy per operation cycle dissipated in the MCML XOR2 cell is lowest among the three circuits. Compared with the XOR2 used in Nangate and NCSU FreePDK45, the XOR2 based on MCML attains about 46.5% and 87.1% energy savings, respectively.

VI. 2-BIT MCML MULTIPLIER

Cell-based design flow has been widely used for digital chip designs with commercial EDA tools. In order to realize a low-power MCML chips, standard cell libraries should be constructed.

The design of the standard cells could be carried for MCML cells. The GDS database can be generated by using the stream out function of IC5141. Then, the auto place and route (P&R) library is created using this GDS database. The synthesis library is generated by using the liberty NCX and HSPICE. After the layout design, the abstract view should be created in library Exchange Format (LEF) for standard cells. The generated abstracts are based on physical layout and logical data, process technology information. It is used in place of full layouts to improve the performance of place-and-route tools, such as Cadence Encounter.

The LEF (Library Exchange Format) tech file can be read by the place-and-route tools. Therefore, LEF tech files should be generated for standard cells. To perform characterization, Liberty NCX should be used to run circuit simulations for the library cells to determine the cell behavior. The library can then be used for timing, power, and noise analysis with various tools such as DesignCompile and PrimeTime. For a characterization task, the template file must specify the SPICE model file name, the SPICE netlist directory, and the SPICE simulator executable. The input and output library names should be also specified.

After the characterization, we can get a library in the liberty format (.lib) that can be used for timing and power analysis with various tools such as Design Compile. We can use the Library Compile tool from Synopsys capture this liberty (.lib) file and translates them into Synopsys internal database (.db) format for synthesis.
In order to estimate effectiveness of the proposed MCML cells, the 2-bit multiplier is verified by using the MCML cells. The structure of the 2-bit multiplier is show in Fig. 10. Fig. 11 and Fig. 12 show the schematic of the 2-bit multiplier. The layout of the 2-bit multiplier using MCML cells is shown in Fig. 13.

HSPICE pre-layout and post-layout simulations are carried out for the MCML 2-bit multiplier. Full parasitic extraction is done for post-layout simulations. The pre-layout and post-layout simulated waveforms are shown in Fig. 14. From Fig. 14, the 2-bit multiplier based on the MCML cells has the correct logic function.

Figure 10. The structure of the 2-bit multiplier.

Figure 11. The schematic of the MCML 2-bit multiplier.

Figure 12. The schematic of the MCML 2-bit multiplier with the bias circuit.

Figure 13. The layout of the MCML 2-bit multiplier using the proposed MCML cells.

Figure 14. The simulation waveforms of the MCML 2-bit multiplier.
VII. CONCLUSIONS

MCML is usually used for high-speed applications. The design methods of the high-speed low-power MOS MCML have been addressed in this paper. The layout implementations of MCML basic gates are also presented at a NCSU FreePDK 45nm technology. Full-custom layouts are drawn, and full parasitic extraction is done. The post-layout simulations are carried out. The results show that the MCML basic gates can save more energy and have better performance than traditional CMOS implementations used in Nangate and NCSU FreePDK45 libraries at 1GHz or higher operation frequencies.

In order to show energy efficiency and performance of the MCML circuits in low-voltage applications, near-threshold computing for MCML circuits is investigated by scaling down the supply voltage from 1.0V to 0.6V. The post-layout simulations show that the power consumption of MCML circuits that operate on near-threshold regions can be reduced without performance degrading.

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Jianping Hu was born in 1961. He received the B.S. degree in Electrical and Electronic Engineering from Dalian Maritime University, Dalian, China, in 1982. He received the M.S. degree in IC Design from University of Electronic Science and Technology of China, Chengdu, China, in 1988. He has been a teacher at Ningbo University since 1988. He is currently a professor in Faculty of Information Science & Technology at Ningbo University, Ningbo City, China. His current research interests focus on low-power digital nanometer circuits and analog integrated circuits.

Prof. Hu got Ningbo Progress Prize in Science and Technology in 2009.

Haiyan Ni was born in 1977. He received the B.S. degree in Electronic Science and Technology Engineering from Ningbo University, Ningbo, China, in 2001. He is currently a M.Sc. student in Circuit & System at Ningbo University, Ningbo, China. His current research interests focus on low-power digital integrated circuits and ASIC design.

Yinshui Xia was born in 1963. He received the B.S. degree in physics from Hangzhou University, Hangzhou, China, in 1984. He received the M.S. degree in semiconductor physics from Hangzhou University, Hangzhou, China, in 1991. He received his doctoral degree from Napier University, Edinburgh, United Kingdom, in 2003.

He is currently a professor in Faculty of Information Science & Technology at Ningbo University, Ningbo City, China. His current research interests focus on EDA design tools and logic synthesis.

Prof. Xia got Zhejiang Progress Prize in Science and Technology in 2011.