Design and Implementation of Ultrasonic Velocity Measuring Module Based on Phase-Locked Loop

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***Abstract*—Due to the important relationship between ultrasonic velocity and some properties of sample, the measurement of velocity of ultrasound is widely needed in various fields. In this paper, based on phase-locked loop technique, a new hybrid circuit is designed for ultrasonic velocity measurement and named as UV-PLL. In order to improve the stability of phase and achieve the ability of fast locking, an auxiliary capturing circuit, which consists of phase shift circuit and capturing circuit, is designed and implemented in this module. Additionally, two methods for estimating the propagation delay is compared and described in detail. The UV-PLL module is validated through the ultrasonic velocity measurement in distilled water at different temperatures. Experimental results show that the maximum relative deviation of velocity measurement is less than 0.15% and the loop can be quickly locked, indicating that this module can meet the requirements of online measurement and can be widely applied.**

***Index Terms*—ultrasound, velocity, phase-locked loop (PLL), auxiliary capturing circuit, amplitude**

I. INTRODUCTION

Due to its advantages of non-destruction, rapidity, accuracy and cheapness, ultrasonic testing has become a hotspot in the industrial inspection field. During the process of testing, a lot of interesting properties of sample are related to the ultrasonic velocity. Therefore, the ultrasonic velocity in specific sample is one of the most important parameters and how to accurately measure this parameter becomes the key problem in the whole inspection system [1, 2]. Usually, the methods for acoustic velocity measurement can be classified into two categories. One is to acquire the velocity through measuring wavelength and frequency, such as the interferometry. The other is to measure the propagation time of acoustic wave through a certain distance to obtain it by division, such as the pulse-echo method and the phase-shift measurement method [3, 4]. Although the former has higher precision, it needs longer measurement time and higher equipment cost. Thus, it is not suit for the requirement of online measurement. Comparatively speaking, the later has shorter measurement time and simple device, but it often has low precision and is easily disturbed by the stray waves.

In this paper, a new circuit module for ultrasonic velocity measurement in liquid sample, which is based on phase-locked loop (PLL) technique, is designed and named as UV-PLL module. The UV-PLL module acquires the velocity parameter through the phase measurement used by PLL. With the features of cheapness and simple operation, PLL is widely applied in radio, computer and other electronic applications. However, it often suffers from the problem of poor phase stability and long measurement time [5]. Thus, an auxiliary capturing circuit is added in UV-PLL module for performance improvement. In order to validate this module, the velocity of ultrasound in distilled water was measured in different temperatures. Experiment results show that the UV-PLL module can achieve the advantages of rapidity, high stability and high precision, which can meet the requirements of online detection system.

II. THEORY

Ultrasonic velocity v in certain medium is determined by two factors: propagation distance l and propagation time τ, which can be described as

$$v = l/\tau \tag{1}$$

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where l can be measured with extremely high precision by the laser distance finder. So, how to get the propagation τ with high precision is the key problem to improve the performance of velocity measurement.

When the ultrasound wave propagates along the x axis, the wave equation can be obtained as [6]

$$A(x) = A_0 e^{-\alpha x} \cos \omega \left(t + \frac{x}{v} \right) \tag{2}$$

where A_0 is the amplitude in original point, $A(x)$ is the amplitude in position x, α is the attenuation coefficient, ω is the angular frequency and t is the time point. It is clear that the phase difference between any two points is determined by the distance between themselves. Assuming that the distance of two points is l and the propagation velocity is v, the phase difference can be computed as

$$\theta = \frac{\omega l}{v} = \frac{2\pi f l}{v} = 2\pi f \tau = \omega \tau \tag{3}$$

where τ also can be called as the phase-delayed time according to phase of signal.

PLL is a phase-controlled feedback system, which tries to generate an output signal whose phase is related to the phase of the input "reference" signal. It is an electronic circuit consisting of a variable frequency oscillator and a phase detector. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phase matched. When the loop is locked, there is no frequency difference between the input signal and output signal, but only a permanent phase difference exists [7]. The PLL circuit can automatically change the frequency, and track the phase difference between input signal and output signal. Since the frequency is the derivative of phase, keeping the input and output phase in lock step implies keeping the input and output frequency in lock step. If the original signal and the τ-delayed signal are used as the input and output signal, the PLL circuit must be locked with the phase difference equaling to $2n\pi$. In other words, the following equation can be established

$$\tau = \frac{\theta}{\omega} = \frac{2n\pi}{2\pi f} = \frac{n}{f} \tag{4}$$

where n is a positive integer and f is the locked frequency of the PLL circuit. It is clear that this equation implies that the ultrasonic wave propagates n cycles during the time segment τ.

The locked frequency f_L can be measured accurately by the digital frequency meter (the error is less than 0.01Hz). Supposing that the integer n can be calculated accurately, the propagation time τ can be easily determined with the same precision.

In the UV-PLL module, the approximate propagation time τ_0 of the ultrasound between the two points is gained through a counter running within the cycle T_M. When the time interval τ_0 is less than T_L which is the cycle of the locked signal, there should be at least one transition of the counter in a cycle T_L (f_L^{-1}). Consequently, the difference between τ and τ_0 is less than T_M, which can be described as

$$0 \le \tau - \tau_0 < T_M \tag{5}$$

$$\tau_0 = pT_M \tag{6}$$

$$\tau = nT_L \tag{7}$$

where p is a positive integer. Then, the range of parameter n can be obtained as

$$\tau_0 f_L \le n < \tau_0 f_L + \frac{T_M}{T_L} \tag{8}$$

Because that T_M is less than T_L ($T_M / T_L < 1$), the value of n can be determined as following

$$n = \begin{cases} \left[\tau_0 f_L \right], & T_L = mT_M \\ \left[\tau_0 f_L \right] + 1, & T_L > T_M, \text{and } T_L \ne mT_M \end{cases} \tag{9}$$

where $[\cdot]$ denotes the operation of rounding and m is a positive integer.

III. Design Of The UV-PLL Module

The hardware structure of the measuring system is shown in Fig. 1, where the PLL circuit and the propagation time measurement circuit are the two core parts of the module. The UV-PLL module consists of two ultrasonic transducers whose center frequency and -6dB bandwidth are 5 MHz and 2MHz, respectively. One is used as the transmitter and the other is used as receiver. These two transducers are aligned and fixed at both opposite sides of the sample cell by epoxy resin. The distance between the two transducers is obtained as L_S=10.086cm by the laser distance finder (XY-FS, Quick Send Measurement Co., LTD, China). Additionally, the temperature of sample is controlled by water bath with precision 0.1℃ and the micro-controller unit (MCU) controls the process of velocity measurement. Here, the integrated chip ADuC848 (Analog Devices, USA) is chosen as the controller of the module.

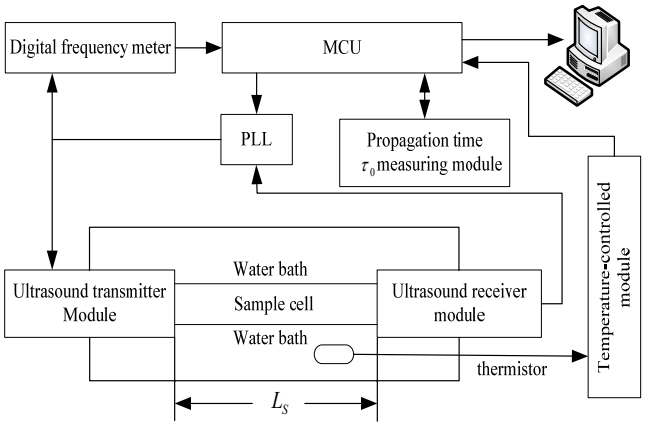

Fig. 1 Block diagram of UV-PLL module

Fig. 2 depicted the structure of sample cell with inner diameter 6mm. Four temperature transducers are equipped for measurement of sample temperature.

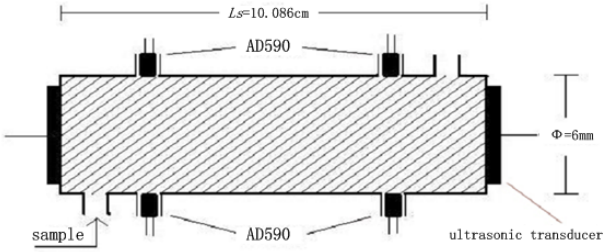

Fig. 2 The structure of sample cell.

A. PLL System Design

The structure of PLL circuit is shown in Fig. 3, which consists of an integrated PLL chip (MC14046B, ON Semiconductor, USA) and its peripheral circuit. In order to improve the stability and precision, surface acoustic wave voltage-controlled oscillator (VCO) is employed in the module, whose free oscillation frequency is 5MHz. generally speaking, if two or more orders active filter is used and step signal does not exist, there is no phase difference between $e_1(t)$ and $e_2(t)$ in steady state. In this module, there will be a certain phase difference between $e_1(t)$ and $e_2(t)$ because of the signal propagation across the sample cell. However, if the phase difference is not equal to $2n\pi$, the PLL circuit would adjust the frequency through VCO until the locked stead-state phase difference is equal to $2n\pi$.

The basic PLL circuit is slow system, and serious phase jitters exist after it is locked, for which it is not suit for high precision measurement. In this work, a new hybrid phase-locked loop system is designed by adding two auxiliary circuits for fast locking and phase stability improvement. The two auxiliary circuits are phase shift circuit and auxiliary capturing circuit.

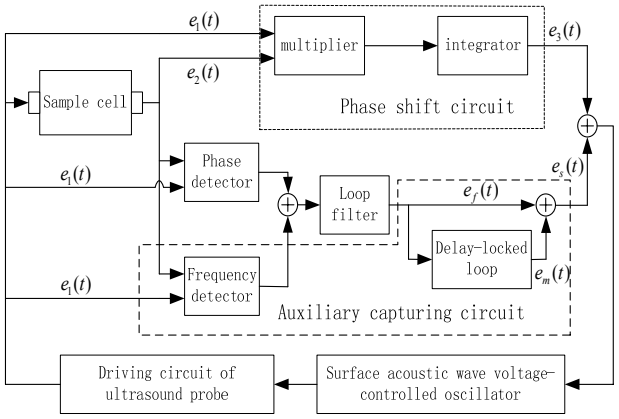

Fig. 3 Structure of the PLL system

(1) Phase shift circuit

When the propagation time τ changes, the locked frequency ω_L also will change resulting in the change of steady-state phase difference accordingly. Therefore, an additional error $\Delta\theta$ will be introduced and the phase difference can be denoted as [8]

$$\theta = \omega_1\tau + \Delta\theta \tag{10}$$

Although increasing the gain of the PLL circuit can improve the stability of θ, it also can lead to the destruction of the entire circuit. When the gain of loop is too high, self-excitation must occur during the phase capturing. Here, to eliminate the impact of additional errors $\Delta\theta$, a phase shift circuit is equipped to reduce the phase jitter. As shown in the dashed-box of Fig. 3, a phase shift circuit mainly includes a precision analog multiplier (MPY634, Texas Instrument, USA) and an analog integrator. Supposing that the two input signals of the multiplier are

$$e_1 = A_1\cos(\omega_I t + \phi_1) \tag{11}$$

$$e_2 = A_2\cos(\omega_I t + \phi_2) \tag{12}$$

where ω_I is the angular frequency of input signal, and ϕ_1 and ϕ_2 are the initial phase. Then the output signal can be computed as

$$\begin{aligned} e_3(t) &= \int_0^t e_1(t')e_2(t')\mathrm{d}t' \\ &= A_1A_2\int_0^t \cos(\omega_1 t' + \phi_1)\cos(\omega_1 t' + \phi_2)\mathrm{d}t' \\ &= \frac{1}{2}A_1A_2\int_0^t \left[\cos(2\omega_1 t' + \phi_1 + \phi_2) + \cos(\theta)\right]\mathrm{d}t' \end{aligned} \tag{13}$$

where

$$\theta = \phi_1 - \phi_2 \tag{14}$$

When $\theta \neq 2n\pi + \pi/2$ or $\theta \neq 2n\pi + 3\pi/2$, the direct current (DC) component of $e_3(t)$ will force the VCO to adjust its frequency and phase until the phase capturing is

achieved. However, $\theta = 2n\pi + 3\pi/2$ is not the stable point of the loop [9], meaning that the $\Delta\theta$ is fixed to $\pi/2$ in steady state. So τ can be obtained from Eq. (4) as

$$\tau = \frac{n + 0.25}{f_L} \tag{15}$$

where

$$n = \begin{cases} [\tau_0 f_L - 0.25], & T = mT_M \\ [\tau_0 f_L - 0.25] + 1, & T > T_M, and T \neq mT_M \end{cases} \tag{16}$$

(2) Auxiliary capturing circuit

In the PLL circuit, auxiliary capturing circuit can accelerate the phase capturing and loop-locked, which is composed of frequency detector (PD) and delay-locked loop (DLL) as shown in Fig. 3. The frequency detector and phase detector are in parallel connection and their outputs add together as the control voltage of VCO. At the beginning, the frequency difference of the PLL is very large, so the circuit turns to steady state mainly depending on the error voltage of frequency detector. Otherwise, after the circuit enters into the rapid capture band, the frequency difference is small and the voltage of phase difference (the output of PD) will mainly lead the PLL circuit into locked state (steady state) [10].

In the process of capturing, filter of the loop (a low-pass filter) will remove the multiple frequency components from the output signal of phase detector to provide bias DC voltage for VCO. Suppose that the cutoff frequency of the filter is f_p. When the condition $2f_I < f_p$ is true, the multiple frequency components can not be filtered out, which will lead to a big jitter of the voltage (e_s) and result in the increase of time consumption for loop lock. To make the loop fast locked, a delay-locked loop is equipped as shown in Fig. 4. The phase detector in DLL circuit is used to compare the phase difference between the input signal (e_f , the output of filter) and the output signal (e_d). Accompanied with the output of MCU e_I, the signal e_f is directly applied as the control signal of voltage-controlled delay line until the loop produces a steady delayed output signal [11].

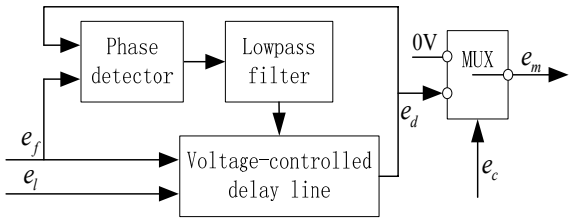

Fig. 4 Block diagram of delay-locked loop

In the ideal case, after the output of phase detector passed through the loop filter, the signal of VCO can be described as

$$e_f = \begin{cases} A\cos(2\omega_I t + \phi) + C, & if\ 2f_I < f_P \\ C, & if\ 2f_I \geq f_P \end{cases} \tag{17}$$

where constant C is the DC component. In Fig. 3, after the processing of DLL, the signal is $e_d(t) = e_f(t + \tau_D)$, where τ_D is the delay time. In DLL module, the output e_m is generated by a multiplexer (MUX), which is controlled by the signal e_c generated by MCU. When the condition $2f_I < f_p$ meets, $e_m(t) = e_d(t)$. Otherwise, $e_m(t)$ is equal to 0. Thus, the signal $e_s(t)$ in Fig. 3 can be obtained as

$$e_s(t) = e_f(t) + e_m(t) = \begin{cases} 2A\cos\omega_I\tau_D\cos(2\omega_I t + \phi + \omega_I\tau_D) + 2C, & 2f_I < f_P \\ C, & 2f_I \geq f_P \end{cases} \tag{18}$$

When the condition $2f_I < f_p$ meets, the jitter of the signal e_s can be improved through the adjustment of τ_D.

B. Propagation Time τ_D Measurement

The sub-circuit for propagation delay τ_D measurement consists of MCU, analog comparator and counter as shown in Fig. 5. Here, coupled with 10MHz crystal oscillator, the integrated circuit SN74LV8154 (Texas Instruments, USA) is chosen as the counter.

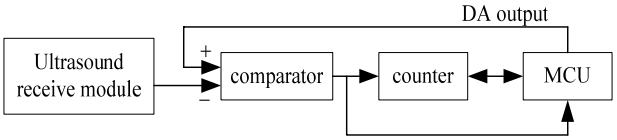

Fig. 5 Block diagram for approximate propagation time measuring.

In the process of measurement, a threshold voltage, which is set up by the digital to analog converter (DAC) of MCU according to the amplitude of the received ultrasonic signal, is added to the non-inverting input. At the beginning, there is no received signal and the output of comparator is a high level signal. Then the MCU starts the PLL to drive the transmitter, meanwhile the counter runs. Because the threshold voltage is lower than the amplitude of received signal, a negative edge will appear at the output edge of comparator when the ultrasound is received. This negative edge will close the counter and inform the MCU through interrupts. At last, the MCU reads the value of counter to calculate the approximate propagation time τ_0. So, how to measure the amplitude of the received ultrasonic signal and how to set the threshold voltage become the key problem.

(1) Method for amplitude measurement

To measure the amplitude of a signal, an analog to digital converter (ADC) can be implemented to sample the corresponding signal. However, if the signal is not slow and steady, its amplitude is very difficult to obtain

because of the sample rate of ADC. Thus, a step-wise-comparison method is applied based on the DAC. This method can be simply summarized as:

step1. MCU controls the DAC to output the maximum voltage which must be higher than the amplitude of the received ultrasonic signal.

step2. MCU checks whether the output of DAC is lower than the amplitude of the received ultrasonic signal. There are two cases.

case1. If the output of DAC is higher than the amplitude of the received ultrasonic signal, the output of DAC decreases by a minimum step. Then, the *step2* repeats once.

case2. If the output of DAC is lower than the amplitude of the received ultrasonic signal, the algorithm ends and the output of DAC can be approximately viewed as the amplitude of the received ultrasonic signal.

It should be noted that this method can also be applied in the opposite direction, meaning that the output of DAC increases by a minimum step and the MCU checks whether the output of DAC is higher than the amplitude of the received ultrasonic signal. Because the output of DAC decreases or increases by the minimum step, the estimated amplitude can be obtained with the same resolution of DAC and must be very close to the true amplitude of the received ultrasonic signal.

(2) Circuit for amplitude measurement

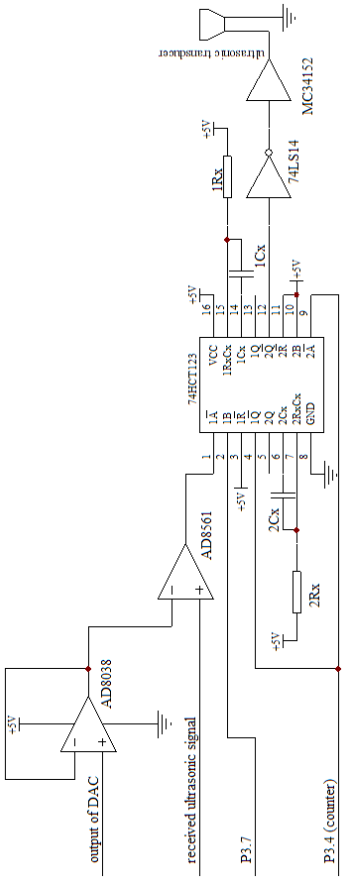

Fig. 6 The circuit for approximate propagation time measuring

According to the method of amplitude measurement, the measurement circuit should consist of DAC, comparator, and MCU at least. In UV-PLL, the circuit for amplitude measurement is depicted in Fig. 6. In this circuit, the chip AD8561 (Analog Devices, USA) is the comparator with the maximum 7 ns delay, the chip AD8038 (Analog Devices, USA) is an operational amplifier, the chip 74LS14 (Texas Instrument, USA) is a hex schmitt-trigger inverters, the chip MC34152 (ONSEMI, USA) is the driver of ultrasonic transducer and the chip 74HCT123 (Texas Instrument, USA) is a high-speed CMOS logic dual retriggerable monostable multivibrator with the truth table as shown in Table. 1. Additionally, the output of DAC module of MCU is connected to the non-reverse input pin of AD8038, the received ultrasonic signal is inputted to the non-reverse input pin of AD8561, P3.7 is a generic I/O port of MCU and P3.4 is the external clock source pin of Timer0/Counter0 of MCU.

TABLE. 1
THE TRUTH TABLE OF 74HCT123.

$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎏
↓	H	H	⎍	⎏
X	X	L	L	H
L	H	↑	⎍	⎏

* H=high voltage level, L=low voltage level, ↑=positive edge, ↓=negative edge, ⎍=positive square wave, ⎏=negative square wave, X=don't care.

The workflow of this sub-circuit can be described as follows:

step1. Initialize P3.7 as low voltage level.

step2. Set TMOD=0x45 and let the DAC of MCU output the maximum voltage.

step3. Let P3.7 output the high voltage level and set the T0 (the register of counter0) as 0xFFFE.

step4. Let P3.7 output the high voltage level for 1 second, and then let P3.7 as the low voltage level.

step5. Check the value of the flag bit TF0. If TF0=0, the algorithm switches to *step6*. Otherwise, the algorithm switches to *step7*.

step6. The output of DAC decreases by a minimum step, and then the algorithm switches to *step3*.

step7. Save the values of register DACH and register DACL and the corresponding output of DAC is the estimated amplitude of received ultrasonic signal.

TMOD=0x45 means that the timer0/counter0 module is used as a counter and the external clock source is inputted from pin P3.4. The circuit runs under three states as follows:

state1. When the pin $1\overline{A}$ =L indicating that the output of DAC is lower than the amplitude of received ultrasonic signal, a positive edge on pin P3.7 ($1B$) can increase the counter0 by one meaning that T0=0xFFFF.

state2. When the pin $2B$ =H and the pin $2R$ =H, a negative edge on the pin $2\overline{A}$ will produce a negative

square wave on the pin $2\overline{Q}$. Through the inverter (74LS14) and the driver of ultrasonic transducer, this negative square wave will make the ultrasonic producing the signal.

state3. When the pin $1\overline{A}$ =L, the pin $1B$ =H, the pin $2B$ =H and the pin $2R$ =H, a positive pulse on ultrasonic transducer will result in a successive positive pulses imposing on the ultrasonic transducer. During a period, the register T0 must overflow with TF0=1.

state4. When the pin $1\overline{A}$ =H indicating that the output of DAC is higher than the amplitude of received ultrasonic signal, the flag bit TF0 will remain as 0 for ever.

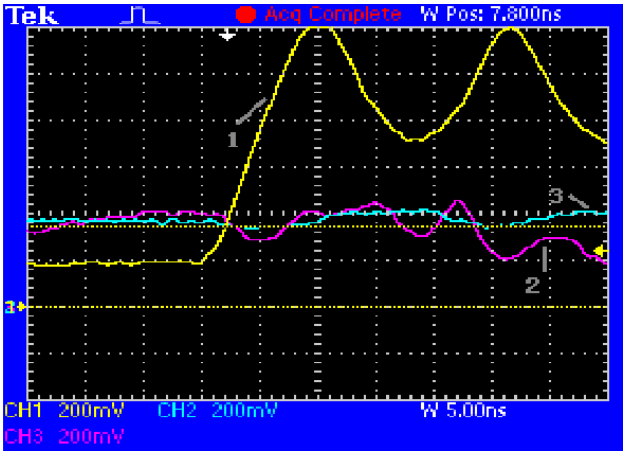

Fig. 7 A instance of *state2* for trigger of ultrasonic transducer ("1"—the output of comparator, "2"—the output of DAC, "3"—the received ultrasonic signal).

An instance of *state2* is shown in Fig. 7. It can be seen that the comparator will output the high level voltage when the output of DAC is lower than the amplitude of received ultrasonic signal. In fact, the comparator will produce several square waves because of the jitters of received ultrasonic signal when the ultrasonic transducer is triggered once. Thus, *state1*, *state2*, *state3* and *state4* can be packaged as a limited state machine, and the amplitude of received ultrasonic signal can be easily measured by the sequential implementation of *state1*, *state2* and *state3*.

After the amplitude of received ultrasonic signal is obtained, the threshold voltage is set as half of the amplitude for measurement of the propagation time τ_D .

C. The Method for Measurement Precision Improvement of τ_D

In section B, the method for estimating the propagation time τ_D is described and discussed. The time of the ultrasonic signal propagating through the sample cell is measured and treated as the propagation time τ_D . However, the propagation time through the sample cell must be very short, which is often shorter than 100us. So, small jitter on the voltage will cause the deviation of the estimated τ_D , and an error will be present in computation of the value of n in Eq. (16).

In order to improve the measurement precision of τ_D , one way is to take the average of several measurement results as the estimated value. In Fig. 6, it should be noted that this function can be achieved by a special configuration after obtaining the amplitude of received ultrasonic signal. This special configuration can be described as follows:

step1. Initialize the pin P3.7=L, TMOD=0x45 and T0=0x0000. The DAC outputs the voltage which is equal to half the amplitude of received ultrasonic signal.

step2. Determine the times of measurement m.

step3. Set pin P3.7=H and start the timer (SN74LV8154) at the same time.

step4. The MCU checks whether the register T0 is equal to m. If the value of T0 is smaller than m, *step4* is repeated. Otherwise, the timer stops and p3.7 outputs the low level voltage.

step5. The value of $\frac{T_{timer}}{m}$ is the estimated value of τ_D , where T_{timer} is the propagation time computed by the timer.

In the *step3*, the pin P3.7 initializes a positive edge on pin $1B$ to drive the ultrasonic transducer. Hereafter, a negative edge will be produced on the pin $1\overline{A}$ when the ultrasonic signal is received in the non-reverse input pin of AD8038. A negative edge on the pin $1\overline{A}$ also can drive the ultrasonic transducer, and this process will continue until the value of T0 equals to m.

IV. EXPERIMENTAL RESULTS

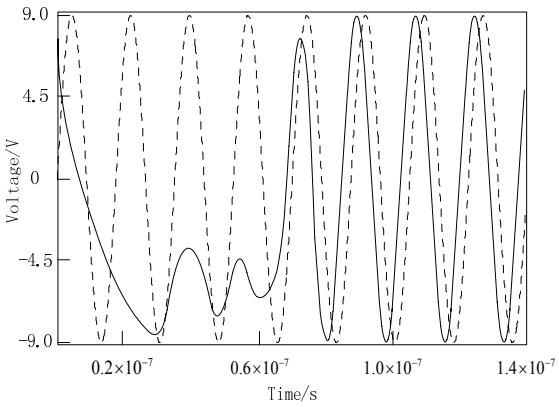

Fig. 8 Locking dynamic process of PLL with auxiliary capturing circuit

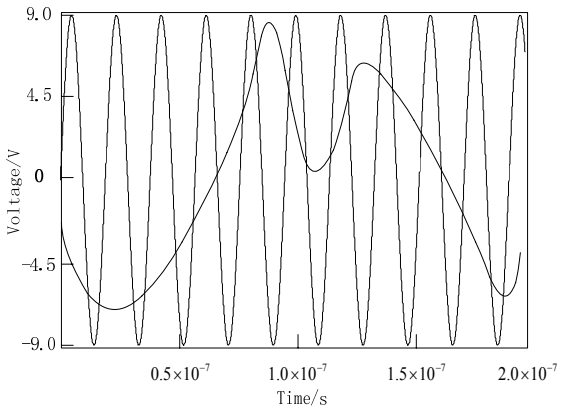

Fig. 9 Locking dynamic process of PLL without auxiliary capturing circuit

Taking the distilled water as experimental object, the process of phase lock is analyzed by using data acquisition card (PCI8622, ART Control, China). As shown in Fig. 8 and Fig. 9, the PLL with auxiliary capturing circuit can reach the steady state within approximately 5 cycles. On the contrary, after 10 cycles, the PLL can not lock the loop without the help of auxiliary capturing circuit. It is clear that the auxiliary capturing circuit can effectively decrease the locking time of the circuit.

Heating the distilled water to 20℃, after the loop is locked, the frequency is $f_L = 5.138691227$ MHz and propagation time τ_0 is equal to 67.90μs. According to Eq. (1), Eq. (15), Eq. (16) and the value of L_S, the ultrasonic velocity is achieved as 1484.004 m/s. It is almost the same as the standard value in Ref. 10. The measured ultrasonic velocity in distilled water at different temperatures is shown in Table. 2. It can be seen that with the help of auxiliary capturing circuit, the precision of the velocity measurement increases about 5 times and the average relative deviation is less than 0.15% compared with the standard values. This is mainly because the phase stability is improved by the auxiliary capturing circuit.

TABLE. 2
ULTRASONIC VELOCITY IN DISTILLED WATER AT DIFFERENT TEMPERATURES

Temperature ℃	Standard value[12] (m/s)	Measured value (m/s)	
		Without auxiliary capturing circuit	With auxiliary capturing circuit
20	1482.358	1496.451	1484.004
25	1496.704	1504.914	1498.712
30	1509.144	1499.991	1511.272
35	1519.825	1511.809	1517.911
40	1528.880	1534.024	1527.122
45	1536.425	1550.203	1538.561

Additionally, the measured ultrasonic velocity with and without average treatment in distilled water is shown in Table. 3 when m=10. It is clear that with the help of average treatment, the precision of velocity measurement has been improved. Without the average treatment during the propagation delay measurement, the average relative deviation of measured velocity is 0.24%, indicating that the error of τ_D can be reduced by using the average value.

TABLE. 3
ULTRASONIC VELOCITY IN DISTILLED WATER AT DIFFERENT TEMPERATURES

Temperature ℃	Standard value (m/s)	Measured value (m/s)	
		Using the τ_D without the average treatment	Using the average value of τ_D
20	1482.358	1487.590	1484.004
25	1496.704	1501.341	1498.712
30	1509.144	1506.939	1511.272
35	1519.825	1516.217	1517.911
40	1528.880	1531.976	1527.122
45	1536.425	1533.308	1538.561

V. CONCLUSIONS

In this paper, the UV-PLL module, which is based on PLL technique, is designed for ultrasonic velocity measurement in liquid. To decrease the time of phase lock and improve the stability of phase, an auxiliary capturing circuit is introduced and equipped into this module. In validation experiments, the UV-PLL module is used to measure the ultrasonic velocity in distilled water at different temperature. The experimental results show that the UV-PLL module has the advantages of rapidity, stability and high precision, which can be applied to the ultrasonic velocity measurement for liquid samples.

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