Research on Low Power Sigma-Delta Interface Circuit used in Capacitive Micro-accelerometers

Yue Ruan, Ying Tang and Wenji Yao
Zhejiang Shuren University, Hangzhou, China
Email: andyruan729@gmail.com; {635766060, 25428878}@qq.com

***Abstract*—Accelerometers have a wide range application in many fields, such as airbag deployment system and electronic stability control system in vehicles, and inertial navigation system in aircrafts and rockets. As Micro-Electro-Mechanical System (MEMS) technology advances, accelerometers are made smaller and smaller, often integrated in a single chip, with lower implementation costs and power consumptions. Modern MEMS accelerometers can be used in portable devices such as cell phones, RFID tags and even integrated in other sensors. This paper presents chip-level design and implementation of a second order sigma-delta interface circuit used in capacitive micro-accelerometers. The interface circuit provides 1-bit data stream and operates at a sampling frequency of 2.5MHz. The system model considers non-ideal factors in the circuit such as nonlinear distortion and noises. These non-ideal factors have been discussed through system level simulation in MATLAB. The micro-accelerometer, which is a highly integrated MEMS device, is then designed and implemented in silicon-on-insulator (SOI) substrate. Finally, the chip-level layout of interface circuit is implemented. Results have shown the chip with area of 1.32mm^2 and power consumption of about 5mW.**

***Index Terms*—micro-accelerometer, sigma-delta, capacitive, interface circuit, layout**

I. INTRODUCTION

Micro-Electro-Mechanical Systems (MEMS) are small integrated devices which are usually fabricated on a silicon substrate and able to combine electrical and mechanical elements for sensing or actuating purposes [1]. Examples of MEMS components include accelerometers, RF MEMS switches, microphones, and micro-resonators. With the fast development of modern MEMS technology, the micro-accelerometers, as the most mature MEMS-based inertial sensor application, have seen significant progress over the past decades. The advantages such as low-cost, low-power, small size, batch fabrication make micro-accelerometers have a wide range of applications, such as automotive safety and stability, biomedical applications, oil and gas exploration, and computer accessories [2]. Take the automotive as example: the micro-accelerometer is used in airbag deployment system to make sure the airbag bounces out when collision occurs (High-G acceleration). In modern vehicles, electronic stability control system (ESC) is often installed. One of the most important sensors in ESC is the accelerometer. A group of accelerometers measure vehicle accelerations in each direction and send data to the control system to increase safety. Besides, modern consumer electronic devices usually use micro-accelerometers in game control. The hard disks in PCs also have micro-accelerometers to detect free-fall and help prevent data loss. Current micro-accelerometers based on MEMS technology have the highest degree of integration, with sensing elements and electronic interface circuitry integrated on a single chip together [3]. The high integration makes micro-accelerometer tiny and consumes little power, which can satisfy requirements in many applications.

Capacitive MEMS accelerometers have been implemented using various surface and bulk micromachining technologies. Unlike bulk micromachining, which defines structures by selectively etching inside a substrate (wafer), surface micromachining creates structures on top of a substrate by using a succession of thin film deposition and selective etching [4]. In MEMS devices, the thickness of the deposited layer and hence the proof mass is small, result in limitations on the performance of the accelerometers. Typically, the resolution of the commercial MEMS accelerometers is in the milli-gravity (mG) range [5]. On the other hand, bulk micromachining features larger proof mass and larger capacitive area that leads to higher sensitivity and higher resolution approaching micro-gravity (μG).

Currently, high performance mixed-signal interface circuits have received growing attention towards high-level of integration, power reduction and noise cancellation (improved resolution). The new generation of accelerometer interface architecture should have the versatility of interfacing with sensors of various sensitivities while maintaining low power consumption, small drift, increased functionality, and large dynamic range.

Silicon-on-insulator (SOI) technology has been widely applied to automotive industry. One of the most obvious advantages of SOI is the reduction of parasitic capacitances compared with conventional silicon (bulk CMOS) due to isolation from the bulk silicon, which improves power consumption at matched performance. In addition, SOI provides resistance to latch-up due to complete isolation of the n and p well structures [6]. Therefore, power consumption is reduced, and faster operation can be achieved.

The objective of this work is to design and implement a second order - modulator to readout the MEMS SOI

doi:10.4304/jcp.7.10.2383-2389

accelerometer. Sigma-delta modulators are often used as interface circuit due to its wide dynamic range, inherent linearity and relaxed accuracy requirements on the analog circuits. The accelerometer described in this paper is designed with the SOI technology. The fully differential 2nd order switched capacitor - modulator as interface circuit is implemented using 1μm, 5V SOI-CMOS process. The modulator performs well in simulation. The peak Signal-to-noise and distortion ratio (SNDR) is about 70 dB (minimum capacitance resolution of 15 aF) in a 5 kHz signal bandwidth from -40ºC to +150ºC. The chip area is 1.32 mm^2 with power consumption of about 4.8 mW. The system level simulation is done in Matlab, and Cadence software environment is used for circuit design and layout.

II. System Modelling

In common accelerometers, a mechanical sensing element converts the unknown quantity of acceleration into a displacement that is then detected and converted to an electrical signal output. The simplified schematic of a fully-differential capacitive MEMS accelerometer is depicted in Figure 1 below [7]. The central part of the accelerometer is a micromechanical proof mass M suspended to a supporting frame by mechanical springs with effective spring constant K, which acts as the sensing element. The squeezed film damping D is imposed by the surrounding air on the structure. The accelerometer has a fully differential sense topology; it means that four sense electrodes with one common node at the proof mass are devised in the fabricated MEMS accelerometers. C_{S1}, C_{S2}, C_{S3}, and C_{S4} are sensing capacitors between the proof mass fingers and the four sense electrodes, respectively.

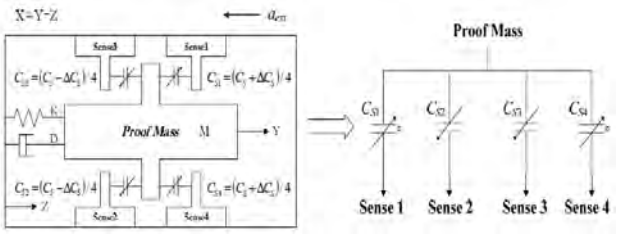

Fig. 1 Schematic of a fully-differential capacitive accelerometer

From Figure 1, C_{S1}, C_{S2}, C_{S3} and C_{S4} has the following relationships:

$$C_{S1,4} = (C_S \pm \Delta C_s)/4$$
$$C_{S2,3} = (C_S \mp \Delta C_s)/4 \quad (1)$$

Where C_S is the rest capacitance at zero acceleration and ΔC_s is the capacitance variation of the sensor at acceleration a_{ext}.

When an external acceleration a_{ext} is applied, the proof mass will move along with the sensing axis with respect to the moving frame of reference (X = Y - Z), causing a change in distance between it and the adjacent fixed electrodes. The displacement of the proof mass can be measured as a very small change in capacitance between it and the fixed electrodes. Figure 2 shows a scanning electron microscope (SEM) image of how this is implemented in silicon. In figure 2, the movable proof mass fingers and fixed sense fingers generate capacitances. When no acceleration detected, ΔC is zero. As external acceleration increases, ΔC follows. By integrating the interface circuit on the same chip with the sensor, extremely small changes in capacitance (ΔC_s, in aF level) can be detected, which means small accelerations can be detected.

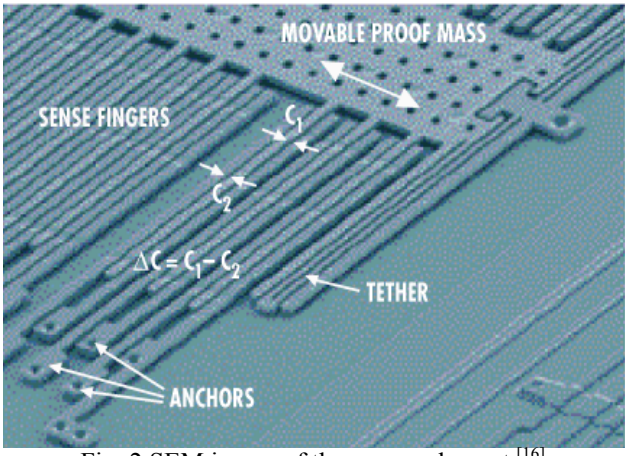

Fig. 2 SEM image of the sensor element [16]

The schematic as shown in Fig. 1 shows the mechanical parameters for the sensing element. According to Newton's law, the differential equation for the displacement x as a function of external acceleration a_{ext} is that of a second-order mass-spring-damper system [1]:

$$M\frac{d^2x}{dt^2} + D\frac{dx}{dt} + K_{eff}\,x = F_{ext} = Ma_{ext} \quad (2)$$

Where, D and K_{eff} are the damping coefficient and spring constant, respectively, and linear relations are assumed. Taking Laplace transform of equation 2 yields the second order equation:

$$(Ms^2 + Ds + K_{eff}) \cdot X(s) = M \cdot A(s) \quad (3)$$

Solving for $X(s)$ gives the transfer function:

$$\frac{X(s)}{A(s)} = \frac{1}{s^2 + \frac{D}{M}s + \frac{K_{eff}}{M}} = \frac{1}{s^2 + \frac{\omega_r}{Q}s + \omega_r^2} \quad (4)$$

With the resonant angular frequency $\omega_r = \sqrt{K_{eff}/M} = 2\pi f_r$ and quality factor $Q = \sqrt{K_{eff}M}/D$. When the system frequency is well below resonance frequency, that is $\omega \ll \omega_r$, the displacement value $x \approx a/\omega_r^2$. The system sensitivity is expressed as:

$$S = x / a \approx 1 / \omega_r^2 \quad (5)$$

This relationship on sensitivity states that there is a tradeoff between the system bandwidth and sensitivity of sensor. As the bandwidth of system increases, ω_r also increase, which results in low sensitivity of the system. On the other hand, low resonant frequency results in large displacements and high sensitivity, but restricts the bandwidth of the sensor.

In this design, an open-loop system is used, as it is simple in hardware, consumes less power than a closed-loop system and fits into automotive stability system application, because such application does not impose requirements on linearity and bandwidth. The system is depicted in Figure 3, which consists of a sensor functioning as the acceleration-to-displacement (capacitance) converter, and a position readout circuit generating the output voltage.

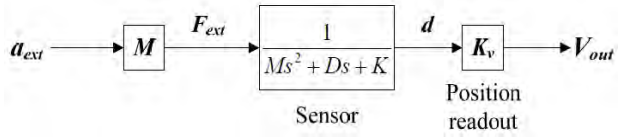

Fig. 3 Schematic of an open loop system

The architecture of a 2nd order Σ-Δ modulator as an interface circuit for accelerometers is shown in Figure 4. The 1st integrator also acts as a capacitance-to-voltage (C/V) converter for the accelerometer.

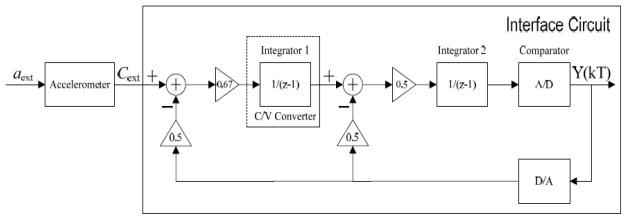

Fig. 4 A 2nd order Σ-Δ modulator as the interface circuit

III. Detailed Interface Circuit Design

This part of the paper illustrates the detailed interface circuit design of the Σ-Δ ADC using 1μm 5V SOI-CMOS technology. In the detailed interface circuit design, the schematics of integrators, with 1st and 2nd order are presented first, and other required modules including op-amps, comparator, band-gap reference and clock generator are designed and simulated. Finally, the layout is carried out.

The Σ-Δ modulator as interface circuit is shown in Figure 5 [8].

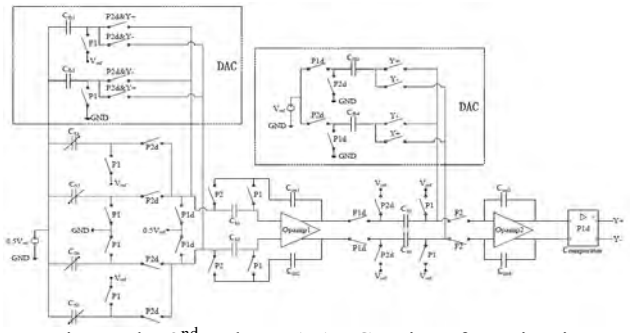

Fig. 5 The 2nd order Σ-Δ ADC as interface circuit

A. Integrators

The integrators have a significant impact on the performance of the Σ-Δ ADC. Some safety margins are taken in the implementation of Σ-Δ modulator to assure integrator performance. Schematic of the 1st and 2nd integrators are shown in Figure 6 and 7 below.

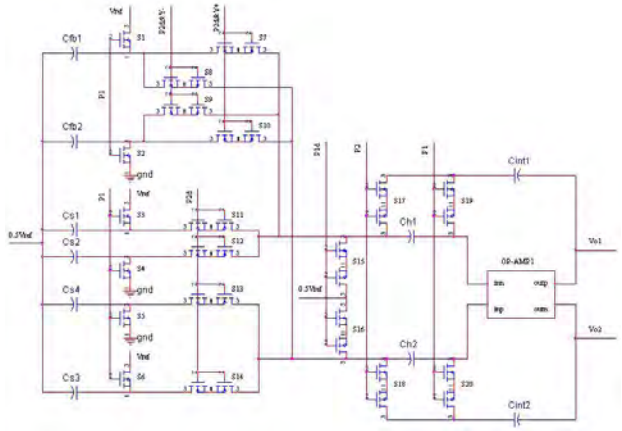

Fig. 6: Schematic of the 1st integrator

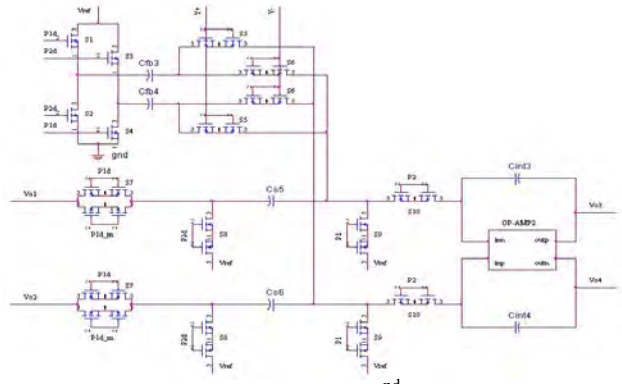

Fig. 7 Schematic of the 2nd integrator

B. Operational Amplifiers

The operational amplifier used in integrators is the most important component of the modulator. In order to suppress harmonic distortion, the op-amps should have enough DC gain. Besides, they should have sufficient slew-rate and large bandwidth to allow fast settling response within the available period. The need for high speed, large bandwidth, coupled with a relatively modest gain requirement of 70 dB to suppress harmonic

distortion, encouraged the use of the fully-differential folded-cascode op-amp as shown in Figure 8 [9].

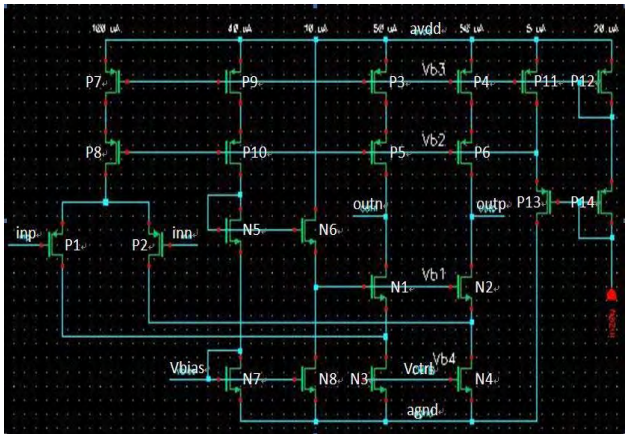

Fig. 8 Folded-cascode op-amp with biasing circuits

C. Comparators

The second major component of the modulator is the quantizer. The one-bit quantizer is realized with a dynamic comparator and a SR latch as shown in Figure 9 [10] and Figure 10 respectively. The function of the comparator in a sigma-delta modulator is to quantize a signal in the loop and provide the digital output of the modulator. The structure and operation are explained as follows.

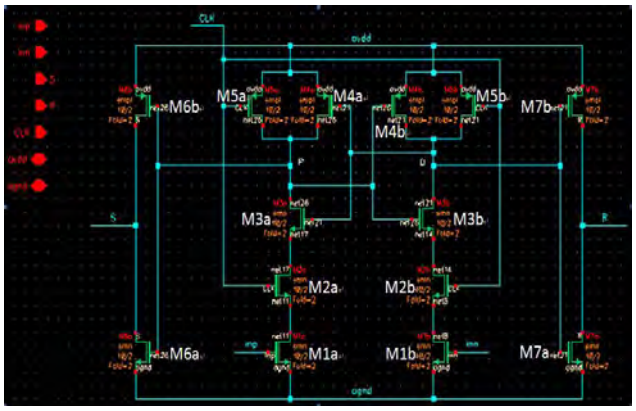

Fig. 9 Schematic of the dynamic comparator

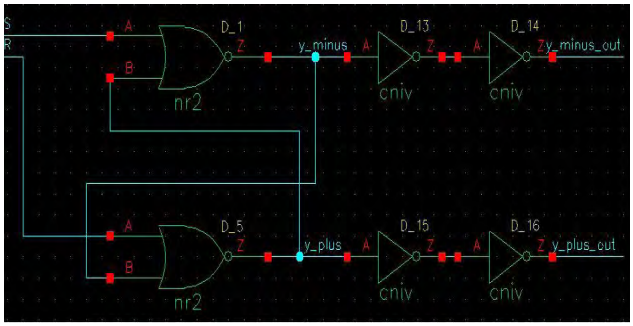

Fig. 10 Schematic of the SR latch and buffers

For a single-bit Σ-Δ modulator, the requirement for the quantizer is quite relaxed as non-idealities such as the comparator offset and hysteresis in this stage can be largely suppressed in the baseband by the second-order noise shaping. The comparator outputs are buffered by digital inverters (CNIV) and then recorded by off-chip data acquisition system for testing. All the transistors are of the size 10 μm/2μm.

IV. Simulation Results

The modulator depicted in Figure 3 is simulated using transistor-level models to evaluate the performance on signal transfer function, quantization noise shaping and distortion, etc. The transistor level is the bottom level in IC design, with the most complicated models and the most precise simulation results. The input signal in the proposed model is ΔC_{smax} = 0.039 pF at 1.6785 kHz. The output signal swings of the 1st integrator and the 2nd integrator are depicted in Figure 11. Their envelopes follow ΔC_{smax}. They are both within ±2V, which fits the op-amp output range (±3V) without significant harmonic distortions.

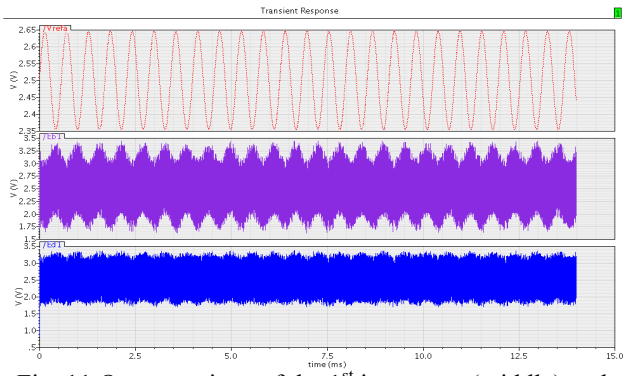

Fig. 11 Output swings of the 1st integrator (middle) and the 2nd integrator (bottom).

Figure 12 shows the two-level digital single-bit stream at the output of the modulator in time domain. The duty cycle of the output pulses follows the input signal ΔCs.

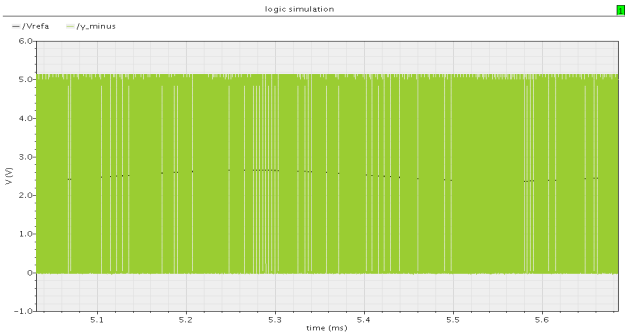

Fig. 12: Output single-bit stream of the modulator and input sinusoidal signal

In order to increase the spectral resolution of a Fast Fourier Transform (FFT), coherent sampling technology is used which is one of the most useful techniques for evaluating the dynamic performance of high-speed ADCs. Coherent sampling describes the sampling of a periodic signal, where an integer number of cycles fit into a

predefined sampling window [11]. Figure 13 and Figure 14 illustrate the output spectrum of the modulator in frequency domain without (Figure 13) or with (Figure 14) DC offset in the 1st op-amp respectively.

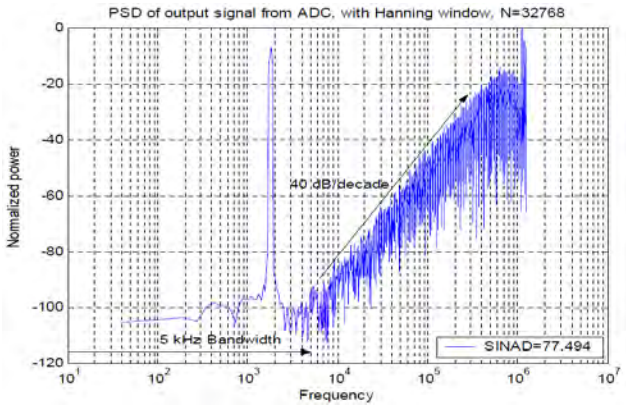

Fig. 13 Output spectrum of the modulator (without DC offset), SNDR = 77.49 dB

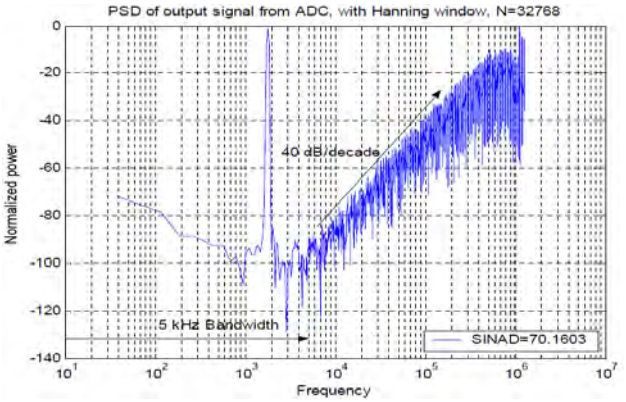

Fig. 14 Output spectrum of the modulator (with DC offset), SNDR = 70.16 dB

From the simulation results in figures above, we can get some comments and conclusions:

1) Since the device models used in transient analysis are noiseless, the output power spectrums in Figure 13 and Figure 14 do not include the contributions of switch noise, op-amp thermal noise and flicker noise, but only contain quantization noise, harmonic distortions and numerical errors due to accuracy of finite in-band FFT bins, simulator algorithm and device models, etc.

2) Both figures show the 2nd order quantization noise shaping of 40 dB / decade, and most of the quantization noise moves to higher frequencies outside the signal bandwidth.

3) In both figures, significant harmonic distortion is not observed within the signal bandwidth of 5 kHz. Therefore, it can be inferred that the implementation of the op-amps, the capacitors, the switches and the DACs have sufficient linearity.

4) In Figure 13, the signal to noise-and-distortion ratio (SNDR) is 77.49 dB when DC offset is not introduced, and it is 70.16 dB in Fig 11 when DC offset is added. Compared to the result from system-level simulation, which is 82.1 dB for the ideal modulator, one reason is the finite DC gain of op-amps degrades the attenuation of quantization noise in the signal bandwidth. The other reason is the limited accuracy of the simulator.

5) In Figure 14, the FFT bin at the lowest frequency is corresponding to frequency smearing of DC offset by Hanning window, and its power is -73dBr. The auto-zeroing technology effectively reduces the op-amp DC offset together with the flicker noise.

V. Hardware Implementation and Performance Test

The layout of the interface circuit is derived via Cadence tools, which is depicted in Figure 15 below. The total chip area is 1.2mm×1.1mm. The blank region is filled by decoupling capacitors for supply voltage and reference voltages, which is not shown for clarity. Separate bond-pads for analog and digital supply voltage are added. On-chip sampling and feedback capacitors $C_{S1\text{-}4}$ and $C_{fb1\text{-}2}$ (0.17 pF each) in the 1st integrator, together with their enable/disable pins, are implemented to make it possible to test the modulator without or with an accelerometer.

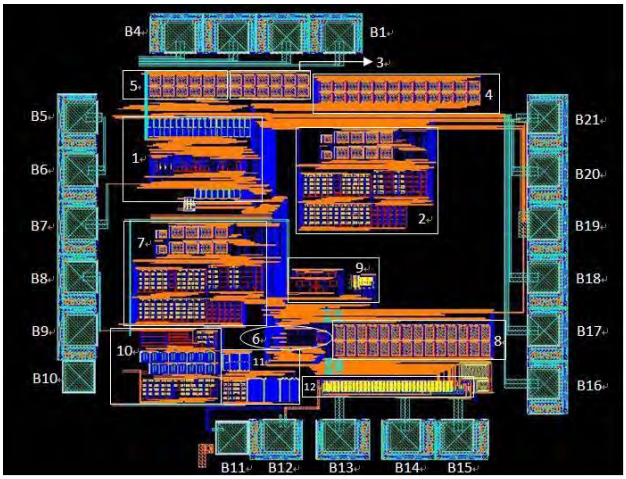

Fig. 15 Layout of the interface circuit

Table 1 below lists the system specification of the proposed MEMS accelerometer. The accelerometer has a full scale measurement acceleration range of 5G. When in 5G acceleration, the capacitance variation of the sensor reaches its full scale value of 0.039pF (39fF), which results the 7.8fF/G capacitive sensitivity. Besides, the rest capacitance C_S is 0.67pF.

Table 1: Specifications of the proposed MEMS accelerometer

Proof mass dimensions ($L \times W \times T$)	0.5 mm × 0.6 mm × 1.5 μm
Proof mass M	9.011×10^{-10} kg
Rest capacitance C_s	0.67 pF
Full scale ΔC_{smax}	0.039 pF
Full scale a_{max}	5 G
Capacitive sensitivity S	7.8 fF/G
Mechanical noise floor	77.53 μG/√Hz
Capacitive gaps d_{narrow}/d_{wide}	0.5 μm/1 μm
Quality factor Q	0.92
Resonance frequency f_r	5 kHz
Mechanical bandwidth f_{-3dB}	4.6 kHz

Table 2 below summarizes the performance of the accelerometer implemented, which is based on 1μm SOI-CMOS technology.

Table 2: Summary of the accelerometer performance

Rest capacitance C_s	0.67 pF
Full scale ΔC_{smax}	0.039 pF
Signal bandwidth	DC to 5 kHz
Oversampling ratio *OSR*	250
Sampling frequency f_s	2.5 MHz
Peak SNDR	70 dB
Resolution ΔC_{smin}	15 aF
Supply voltage	5 V
Power consumption	5 mW
Chip area	1.32 mm^2
Temperature range	−40ºC to +150ºC
Technology process	1 μm SOI-CMOS

VI. Conclusion and Future Works

MEMS devices especially sensors and micro motors are widely used in applications ranging from automotive safety and stability systems to biomedical applications, oil and gas exploration, computer accessories, etc. The objective of this work is to design and implement an interface circuit for SOI accelerometers in automotive stability systems. This work has focused on the analysis of accelerometer system and the design of a low-power high-resolution interface circuit in top-down design methodology.

The principle of the accelerometer model indicates that sensor capacitance changes in response to external acceleration. Accelerometer systems are classified into open-loop and closed-loop systems, depending on whether a force feedback loop is applied to the sensor. In this design, open-loop structure is used as it is simple and effective for the application. The specifications of SOI accelerometers and its readout circuitry have been proposed. A fully differential sigma-delta modulator is adopted in this project due to its wide dynamic range, inherent linearity and relaxed accuracy requirements on the analog circuit.

The 1st integrator is a crucial component in the design of a 2nd order sigma-delta modulator. It acts as a capacitance-to-voltage converter and determines the noise and distortion performance of the modulator. Based on noise analysis, auto-zeroing technique is applied to reduce flicker noise and DC offset, achieving high resolution.

The specifications on circuit blocks are easily established by modeling and simulating non-idealities of the Σ-Δ modulator, such as sampling jitter, *kT/C* noise and operational amplifier parameters (noise, finite DC gain, finite bandwidth and slew rate, and saturation voltages) on the system-level in MATLAB.

An experimental Σ-Δ modulator that fulfills these specifications is implemented using 1μm 5V SOI-CMOS technology. This includes implementation of the integrators, op-amps, comparator, band-gap reference, clock generator and layout. In the simulation, the modulator performs well in a 5 kHz bandwidth from -40 ºC to +150 ºC, and has a peak SNDR of 70 dB which corresponds to 11-bit resolution and minimum capacitance resolution of 15 aF. The chip area is 1.32 mm^2 with power consumption of approximately 5 mW.

Regarding to future works, this design can be extended to further lower voltage operation (i.e., 3.3 V) despite the large threshold voltage of transistors (approximately 1 V). The reference voltage can be tied to supply voltage for better resolution. Some trade-offs can be made between the power dissipation and resolution, to allow the use of other ADCs such as successive approximation registers (SAR) as interface circuit for accelerometers.

This work has been verified by CADENCE, which is a mixed-mode simulation tool. The transistor-level simulation is very time consuming. In recent years, the mixed-signal circuit design is more and more popular. In order to speed up the period of design flow path, using other modeling level simulation tools such as Verilog-A is an important method. Besides, demonstrating the functional operation and performance metrics of the designed interface circuit by taping out and measuring is another important procedure in the future.

The future research interest would be to employ a closed-loop system. Force-feedback may improve many characteristics of a sensor including bandwidth, dynamic range and linearity. The most popular approach is to pulse-modulate the force-feedback signal [12]. High-order closed-loop system (i.e., 2nd order sensor element and 2nd order electronic filter [13]) may result in low quantization noise.

References

[1] B. V. Amini, “A Mixed-Signal Low-Noise Sigma-Delta Interface IC for Integrated Sub-Micro-Gravity Capacitive SOI Accelerometers”, *Doctoral Thesis*, Georgia Institute of Technology, May 2006.

[2] G. Zhang, “Design and Simulation of A CMOS-MEMS Accelerometer”, *Master Thesis*, Carnegie Mellon University, May 1998.

[3] W. Yun, “A surface micromachined accelerometer with integrated CMOS detection circuitry”, *Doctoral Thesis*, U.C. Berkeley, 1992.

[4] http://en.wikipedia.org/wiki/Bulk_micromachining.

[5] B. V. Amini and F. Ayazi, “A 2.5-V 14-bit ΣΔ CMOS SOI Capacitive Accelerometer”, *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2467–2476, Dec. 2004.

[6] http://en.wikipedia.org/wiki/Silicon_on_insulator.

[7] B. V. Amini and F. Ayazi, “Micro-gravity Capacitive Silicon-on-Insulator Accelerometers”, *J. Micromech. Microeng.*, vol. 15, pp. 2113-2120, Sep. 2005.

[8] Y. Yu, A Sigma-delta ADC as Interface Circuit for SOI Accelerometers, *Master Thesis*, TU Delft, 2005.

[9] B. Razavi, “Design of Analog CMOS Integrated Circuits”, *McGraw-Hill*, 2001.

[10] T. B. Cho and P. R. Gray, “A 10 b, 20 M sample/s, 35 mW pipeline A/D converter”, *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995

[11] http://www.maxim-ic.com/appnotes.cfm/an_pk/1040/, “Coherent Sampling vs. Window Sampling”, Application Note 1040, *Maxim-IC*, Mar. 2002.

[12] A. M. Lemkin, B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics", *IEEE J. Solid-State Circuits*, vol. 34, no. 4, Apr. 1999.
[13] V. P. Petrov and B. E. Boser, "A fourth-order sigma-delta interface for micromachined inertial sensors", ISSCC 2004, pp. 320-329, 15-19 Feb. 2004.
[14] Kulah. H, Chae. J, Yazdi. N. and Najafi. K, "Noise analysis and characterization of a sigma-delta capacitive microaccelerometer", *Solid-State Circuits, IEEE Journal of* , vol.41, no.2, pp. 352-361. Feb.2006.
[15] Jeongjin Roh, etc. "A 0.9-V 60-μW 1-Bit Fourth-Order Delta-Sigma Modulator With 83-dB Dynamic Range", *Solid-State Circuits, IEEE Journal of,* vol.43, no.2, pp. 361-370. Feb. 2008
[16] http://www.micromagazine.com

Yue Ruan received the B.S degree in electronic engineering from Zhejiang University, Hangzhou, China, in 2006, and the M.Sc degree in electrical engineering from Royal Institute of Technology (KTH), Stockholm, Sweden, in 2008.

He is currently a Faculty Member with the college of Information Science and Technology, Zhejiang Shuren University, Hangzhou, Zhejiang, China. From 2008 to 2009, he worked as a research engineer in Motorola Inc. He has published more than 10 technical papers and a text book entitled *Microcontroller Theory and Applications – Based on sample driven and Proteus simulation* (China, Science Press, 2011), of which he is the co-author. His current research involves wireless sensor networks, MEMS sensors, EDA based VLSI design and RF integrated circuits.