Digital High Order Multiplier-free Delta Sigma Modulator for Multistandard Fractional-N Frequency Synthesizer

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Abstract—**This paper proposes a new stable design strategy for 1-bit high order digital ΔΣ modulator for multistandard fractional-N frequency synthesizer. The proposed digital ΔΣ modulator presents simplicity, low power consumption and controls a dual-modulus divider instead of multi-modulus one as in existing ΔΣ fractional-N frequency synthesizer. Simulation results illustrate the ΔΣ modulator good performances in terms of spectrum purity and accuracy. Using this stable 1-bit digital ΔΣ modulator output to a fractional-N frequency synthesizer Simulink model verifies the multistandard frequency synthesizer specifications.**

Index Terms: **Multistandard frequency synthesis, Fractional-N PLL, Digital ΔΣ modulator.**

I. INTRODUCTION

Recently, the growing significance of wireless media for voice and data communications added to the communication standard diversity are driving the need for wireless multistandard terminals which should be low cost, little size and low power [1].

Due to the distinction between different standards specifications, without a rigorous innovation effort, the memory size, processing complexity and power consumption of such terminals will be so enormous that they will never result in a feasible commercial product. Indeed, a replication of chips to handle individually each standard would result in a great area, higher noise and increased power loss compared to a system-on-chip approach. Therefore, it is important to improve a design at several parts. One of the exigent RF parts to design is the transceiver [1, 2].

The future trends are working on the Software Defined Radio concept, where hardware is reconfigured by software in order to handle different standards [3]. To constitute a multistandard transceiver for a radio communication device, one indispensable component is crucial for both receiver and transmitter paths: the frequency synthesizer. It generates the local oscillator signal for frequency conversion stage. In addition, the frequency synthesizer should enable correct compatibility between the different considered standards.

The ΔΣ fractional-N frequency synthesizer is considered as the most suitable frequency synthesizer for multistandard applications. For complexity and low power reasons, a 1-bit high order ΔΣ modulator should be used [4]. The major disadvantage of the ΔΣ modulator in literature is instability phenomena [5].

In this work, authors propose an innovative stable structure of 1-bit high order digital ΔΣ modulator for multistandard frequency synthesis. In section II, we investigate the general problem of frequency synthesis and detail three topologies of PLL-based frequency synthesizers: integer-N frequency synthesizer, fractional-N frequency synthesizer and ΔΣ fractional-N frequency synthesizer. In section III, we establish multistandard PLL-based frequency synthesizer design specifications. Section IV deals with the proposed stable digital ΔΣ modulator, evaluates its performances in case of ΔΣ fractional-N frequency synthesizer application and presents results of controlling a fractional-N frequency synthesizer Simulink model by the obtained ΔΣ modulator output. Finally, conclusions are drawn in section V.

II. FREQUENCY SYNTHESIS TOPOLOGIES

A. Phase-Locked Loop

PLL is fundamentally a closed loop control system [6, 7]. It consists of a Phase Comparator (PC), a Loop Filter (LPF) and a Voltage Controlled Oscillator (VCO). The PC compares its two input signals phases and generates a measure of their phase error. The phase error must be filtered by a Low Pass Filter (LPF). The LPF takes out the DC part of the phase error. The VCO acts as an oscillator whose frequency changes by the filtered PC output [6, 7]. The loop is locked if phase error is constant over time. Thus, reference and VCO frequencies are equal. Fig. 1 shows a basic PLL block diagram. PLL is a multi-purpose electronic device. One of its many applications is frequency synthesis [8-10].

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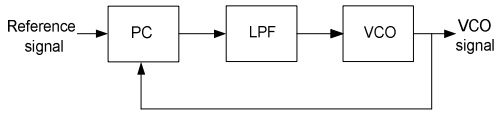

Figure 1. PLL block diagram.

B. *Integer-N frequency synthesizer*

Integer-N frequency synthesizer can be obtained by placing a programmable integer frequency divider in the PLL feedback path. Fig. 2 presents an integer-N frequency synthesizer. The integer frequency divider divides feedback signal frequency f_{VCO} by N in order to make the output frequency integer multiple of the reference frequency f_{REF} as given by (1).

$$f_{VCO} = N.f_{REF} \tag{1}$$

The VCO frequency may be changed by varying division ratio N. This means that the channel spacing is equal to the reference frequency. The reference frequency must be carefully chosen. For a high-required resolution, as for GSM and UMTS standards [11, 12], the reference frequency should be very low and the division ratio N increases with the synthesized output frequency. On the other hand, a high value of N implies the growth of phase noise level [13]. Consequently, the PLL bandwidth must be small relatively to the reference frequency to diminish the phase noise. Reducing the loop bandwidth will raise the time required to achieve the chosen VCO frequency [7, 14].

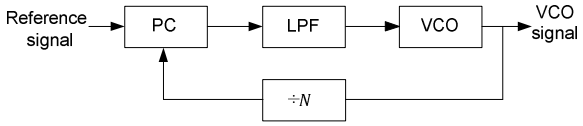

Figure 2. Integer-N frequency synthesizer.

C. *Fractional-N frequency synthesizer*

A non-integer multiple of the reference frequency can overcome the problem of integer-N frequency synthesizer by keeping unchanged the required resolution for higher reference frequency. This allows a larger PLL bandwidth and as a result the required locking time is greatly reduced. We can make fractional-N frequency synthesizer by replacing the simple integer divider by N with a dual-modulus divider N/N+1. Fractional-N frequency synthesizer is given by Fig. 3.

The difference between the integer-N frequency synthesizer (Fig. 2) and the fractional-N frequency synthesizer (Fig. 3) is that the frequency divider has a choice between two integers N and $N+1$. The dual-modulus divider divides its input by N when the accumulator is not overflowed. When an overflow signal appears at the accumulator output, the dual-modulus divider divides the feedback signal frequency by $N+1$. On average, the divider divides its input by a fractional ratio N_{fract} between N and $N+1$. We assume that the accumulator size is F. For every F clock cycles, the accumulator overflows K times, thus the divider divides K times by $N+1$ and divides by N for the remaining time as indicated in (2).

$$N_{fract} = \frac{K(N+1)+(F-K)N}{F} = N + \frac{K}{F} \tag{2}$$

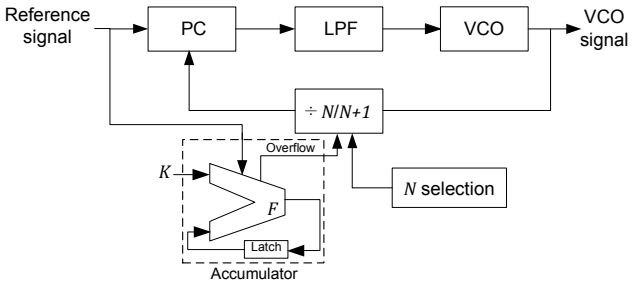

Figure 3. Fractional-N frequency synthesizer.

The alternating N/N+1 division causes the variation of the output frequency between $N.f_{REF}$ and $(N+1).f_{REF}$. This alternating cyclical process generates spurious tones at the fractional offset frequency [14].

D. *ΔΣ Fractional-N frequency synthesizer*

Another variety of fractional-N synthesizer uses the ΔΣ modulation to randomize the choice of N/N+1 division ratio [10, 15]. The accumulator can be considered as a first order ΔΣ modulator. When higher order ΔΣ modulator is used, noise can be shaped and pushed away from PLL bandwidth and hence concealed at the output of the frequency synthesizer. Fine frequency resolution can be restricted just by sizing the digital integrators [2]. In fact, multiple-bit ΔΣ modulator needs multi-modulus divider.

Later in this paper, we adopt ΔΣ fractional-N frequency synthesizer in multistandard frequency synthesis for its advantages. Fig. 4 illustrates single-bit ΔΣ fractional-N frequency synthesizer.

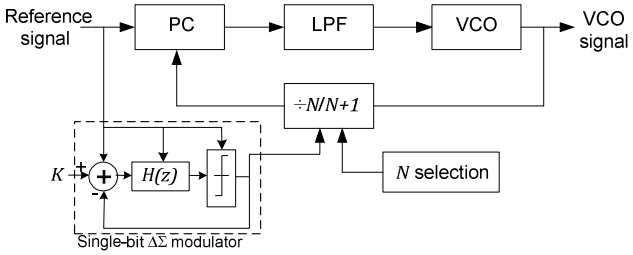

Figure 4. ΔΣ Fractional-N frequency synthesizer.

The loop filter cut-off frequency is expressed in (3) when ΔΣ modulator order and loop filter order are equals [16].

$$f_{cmax} = \left[S_{\Sigma\Delta}(f) \frac{12}{(2\pi)^{2n}} f_{REF}^{2n-1} f^2 \right]^{1/2n} \tag{3}$$

where $S_{\Delta\Sigma}(f)$ is the required phase noise level specification at a frequency offset f, f_{REF} is the reference frequency and n is the $\Delta\Sigma$ modulator order.

III. MULTISTANDARD FREQUENCY SYNTHESIS SPECIFICATIONS

To target realistic specifications, multistandard frequency synthesizer design uses various communication standards. The standards incorporate different specifications as frequency range, channel bandwidth, modulation technique, transmission rate and phase noise. Table I summarizes the listed specifications of the different communication standards [17].

TABLE I. STANDARDS SPECIFICATIONS AND FEATURES

	Frequency Range (MHz)	Channel (MHz)	Modulation technique	Rate (Mbit/s)	Phase Noise (dBc/Hz @MHz)
GSM	890-960	0.2	GMSK	0.271	-141@3
DCS	1710-1880	0.2	GMSK	0.271	-133@3
PCS	1850-1990	0.2	GMSK	0.271	-133@3
UMTS	1900-2025	5	QPSK	3.84	-145@20
802.11a	5150-5825	16.6	QAM	54	-102@1
802.11b	2400-2484	14	QPSK	11	-102@1
802.11g	2400-2484	14	QAM	54	-102@1

These various properties imply the difficulty for a transceiver to support the different standards when sharing some of the components. Generally, it is essential to offer a clean, stable, cheap, low power, variable and fast local oscillator signal.

A. Spectral purity and frequency stability

It may appear in the frequency spectrum synthesizer some spurious tones [15]. Assuming that spectrum of the local oscillator signal contains a spurious tone, two spectral components appear in the output spectrum after the frequency conversion stage. Indeed, the useful signal is mixed with the local oscillator signal and the spurious tone. A similar situation affects the quality of transmitted data.

In the frequency domain, local oscillator signal spectrum is never a line focused at a specified frequency. The distributed power around the central frequency affects frequency conversion quality. Phase noise is typically expressed in dBc/Hz at a particular offset from the carrier frequency. From table I, we notice that the GSM required phase noise is the most restrictive. Satisfying the GSM specifications in terms of phase noise, $-141\,dBc/Hz$ at $3\,MHz$ offset, implies a valuable spectral purity for all of the standards presented in Table I. In addition, the local oscillator signal must be stable, namely the carrier frequency should maintain a constant value during time.

Local oscillator signal has to be clean and stable since spurious tone absence and low phase noise level are required by the consistency of data transmission [16]. Generally, the PLL presents high frequency stability thanks to its tracking capabilities. Fractional-N frequency synthesizer allows to PC to operate with much higher reference frequency which decreases the phase noise level in the loop. Consequently, high spectral purity is offered [10].

B. Cost-effectivity

Cost-effectivity comes in two main angles. First, the reduced market price is very important feature for a viable and competitive product. Second, the low power consumption is a vital quality for mobile equipment. The idea is to delay the battery depletion for the longest duration. Standby mode saves battery power. Nevertheless, this technique becomes needless if power consumption in active mode is very high. Thus, the aim is to minimize the power consumption in activity case. Therefore, it is necessary that all components, including the frequency synthesizer, consume relatively low amounts of power. There has been a trend toward higher levels of integration, mainly aiming at lower cost and lower power consumption. Thus, the aim is to design a frequency synthesizer suited for integration to respond to the small form factor [18].

Local oscillator requests to have a low price, to occupy a small size and to consume a low power in order to perform a commercial device [16]. Compared to multi-modulus divider, dual-modulus divider recommends ΔΣ fractional-N frequency synthesizer in terms of low power consumption.

C. Tuning range

In multistandard frequency synthesizer case, broadband and wide tuning range is a fundamental property. Indeed, supported communication standards frequency ranges are diverse. The multistandard frequency synthesizer has to cover all frequency ranges. Moreover, the multistandard frequency synthesizer should achieve very high resolution in order to generate accurate carriers.

Local oscillator signal has to be variable to address all frequency channels [16]. Thanks to locking process and ΔΣ modulator high resolution, the multistandard frequency synthesizer can provide the required accuracy. The required frequency resolution is the GSM channel bandwidth or the UMTS channel spacing equal to $200\,kHz$. For this resolution, WiFi channel spacings are satisfied because they are multiple integers of $200\,kHz$. Besides, it must contain a broadband VCO which may cover all supported communication standards bands as the multi-band VCO described in [17]. This VCO offers frequency ranges from $3.1\,GHz$ and $4.1\,GHz$. These ranges are digitally controlled in order to deliver all Table I-cited standards carrier frequencies.

D. Fast locking

Cellular systems have a determined slot to receive and transmit. The oscillator has to switch quickly before the expiration of its allocated time slot. This constraint becomes more severe in multistandard case. Indeed, each standard is characterized by a particular transmission rate. Various transmission rates imply the fast locking requirement. For any supported standard, it is imperative that the frequency synthesizer provides quickly the desired carrier. So, the local oscillator is concerned with high standards rates. The standards settling time varies generally between $150\,\mu s$ and $200\,\mu s$ [19]. This requires a synthesizer fast locking time lower than or

equal to the lowest settling slot related to IEEE802.11b. Local oscillator signal needs to fast switch to provide sufficiently rapid channel selection [16]. Fast switching is related to wide loop bandwidth of frequency synthesizer. Fractional-N frequency synthesizer presents larger loop bandwidth, and thus, smaller switching time, compared to integer-N frequency synthesizer [10].

Finally, the multistandard frequency synthesizer specifications are determined. The phase noise needs to be lower than $-141\ dBc/Hz$ at $3\ MHz$ offset corresponding to GSM features [17]. From (3), we compute the loop filter cut-off frequency f_{cmax} for a given reference signal at $13\ MHz$ delivered from a crystal oscillator. The reference signal should have a high spectral purity and a precise value. Also, the required frequency resolution is $200\ kHz$ and the maximum locking time is $150\ \mu s$. As the locking time is equal to $1/\ f_{cmax}$ which is lower than the $150\ \mu s$ [13], we need a cut-off frequency higher than $6.67\ kHz$. This value is too low compared to the reference frequency $13\ MHz$. Thus, we increase the cut-off frequency regarding the phase noise level. Indeed, a cut-off frequency of $262\ kHz$ is obtained from (3) for a 4th order loop filter and satisfying the $-141\ dBc/Hz$ phase noise level at $3\ MHz$ offset. This result is obtained when the ΔΣ modulator and the loop filter orders are equal.

Besides, as given, in Fig. 4, the ΔΣ modulator sampling frequency is the same as the reference frequency. In this work, authors propose to use a single-bit ΔΣ modulator. In this case, the maximum signal-to-noise ratio (SNR) is given by (4).

$$SNR_{max} = \frac{\sqrt{3}\sqrt{2n+1}(OSR)^{n+0.5}}{\sqrt{2}\pi^n} \quad (4)$$

where n is the ΔΣ modulator order and the OSR is the oversampling ratio between the ΔΣ modulator sampling frequency and two times the cut-off frequency. In our case, the obtained SNR_{max} is $97.34\ dB$ which requires a 16-bit resolution ΔΣ modulator. Based on the $13\ MHz$ reference frequency, the resulting minimum frequency step is therefore around $198\ Hz$.

All loop filter and ΔΣ modulator specifications are cited in Table II and come with reduced power and cost. Existing multistandard frequency synthesizers are not cost-effective. Indeed, in [2, 13], the frequency synthesizers are based on a high order ΔΣ modulator and a multi-modulus divider in the PLL feedback loop [13, 18, 20].

TABLE II. MULTISTANDARD FREQUENCY SYNTHESIZER SPECIFICATIONS

	Parameters	Values
ΔΣ fractional-N frequency synthesizer	Refrence frequency	13 MHz
	Loop filter order	4
	Cut-off frequency	262 kHz
	Divider nature	N/N+1
ΔΣ modulator	Sampling frequency	13 MHz
	Modulator order	4
	Resolution	16 bits
	Quantizer bit number	1 bit

We propose in this work to design a single-bit digital high order ΔΣ modulator to control a dual-modulus divider instead of cost and power effective multi-modulus one. Table III presents some parameters for comparison between dual-modulus and multi-modulus divider.

TABLE III.
COMPARISON BETWEEN DUAL-MODULUS AND MULTI-MODULUS DIVIDERS

	Dual-modulus divider	Multi-modulus divider
Origin	-	Extension of dual-modulus divider
Complexity	Low	High
Nature	Asynchronous	Synchronous
Power consumption	Low	High
Speed	High	Very high
Switching noise	Low	High

IV. DIGITAL ΔΣ MODULATOR DESIGN METHODOLOGY

A. Approach description

The 1-bit high order ΔΣ modulator is the most attractive thanks to its high SNR, simple circuit and good idle-tone performances [21]. ΔΣ modulator is also compatible with dual-modulus divider which offers simplicity and low power consumption to fractional-N frequency synthesizer. ΔΣ modulator and its linear model are giving respectively by Fig. 5 (a) and (b).

The major obstacle to overcome is the problem of stability. Stability is a vital matter in the design of ΔΣ modulators. In fact, the SNR of an unstable ΔΣ modulator is deteriorated by reason of alternating long output strings of 0 and 1 [22]. A helpful technique for 1-bit high-order ΔΣ modulator stability has been established: designing a new ΔΣ modulator filter [21]. Indeed, the filter $H(z)$ can always be derived from NTF by simple loop algebra of (5). Equation (6) provides the state equation of ΔΣ modulator linear model.

$$NTF(z) = \frac{1}{1+H(z)} \text{ and } STF(z) = 1 - NTF(z) \quad (5)$$

$$Y(z) = STF(z).X(z) + NTF(z).E(z) \quad (6)$$

The ΔΣ modulator shown in Fig. 5 (c) offers an independent NTF. We adopt a structure with a unity STF ($STF\ (z) = 1$) because it does not require pre-equalization.

1) Butterworth high-pass response

The problem encountered in n^{th} order pure differentiation NTF was the large high-frequency noise shaping gain for high value of n which causes the idling waveform at the comparator input to be very large, resulting in low comparator gain and hence instability [21]. We can modify the pure differentiating response by introducing poles into NTF as given by (7).

$$NTF(z) = \frac{(1-z^{-1})^n}{D(z)} \quad (7)$$

where $D(z)$ is an n^{th} order polynomial.

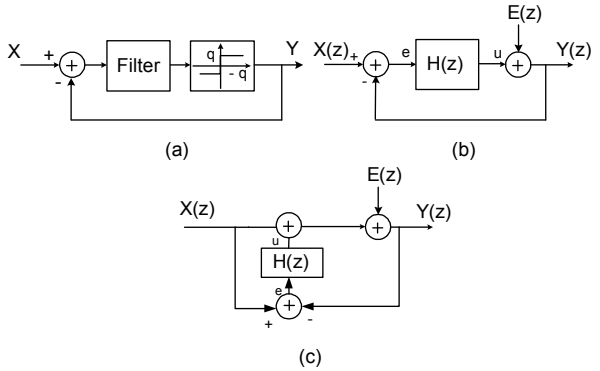

Figure 5. ΔΣ modulator (a) with its linear model (b) unity STF configuration (c).

The purpose of adding $D(z)$ is to flatten the high-frequency portion of $NTF(z)$, as shown in Fig. 6 (a). NTF is now simply a n^{th} order high-pass function. With the correct choice of $D(z)$, a Butterworth alignment of the poles can be obtained, resulting in a maximally flat high-frequency region of $NTF(z)$ [21].

2) Inverse Chebychev with complex zeros on the unit circle

The Butterworth high-pass response can be modified to move the real stop-band zeros on the unit circle to produce inverse Chebychev nulls in the noise-shaping transfer function at frequencies other than DC. An example of such a response for a fourth-order system is shown in Fig. 6 (b).

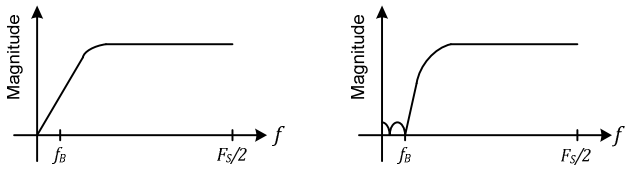

Figure 6. Butterworth (a) and Chebychev (b) noise shaping responses.

Compared with the Butterworth alignment, under the baseband frequency f_B, the area of the noise-shaping response is reduced. The equation for a general n^{th} order noise shaper of this type is given by (8).

$$NTF(z) = \frac{\prod First\_order\_terms. \prod Second\_order\_terms}{D(z)} \tag{8}$$

B. ΔΣ modulator design example

There are numerous topologies that can be used to implement $H(z)$, and can be split into numerator and denominator sections, and these can be implemented separately in different locations within the loop. We start the design by using a Butterworth filter because of its flat characteristics and its relative insensitivity to coefficient errors. The process involves computing the *s*-domain poles, then translating them into the *z*-domain with a bilinear transform. Then the desired values of the *z*-domain poles are known. Fig. 7 shows a 4^{th} order $H(z)$ LDI (Lossless Digital Integrator) structure. $H_D(z)$ is defined by (9).

$$H_D(z) = \frac{G(z-1)^n}{(z-p_1)(z-p_2)\ldots(z-p_n)} \tag{9}$$

where $p_1, p_2, \ldots, p_n$ are the *z*-domain poles. $H_D(z)$ can be related to $NTF(z)$ by a simple relationship $HD(z) = z.NTF(z)$. For the case of $n = 4$, $G = 1$, the *s*-domain poles are at $p_{1,2} = -1.8047 \pm j\,0.7486$ and $p_{3,4} = -0.7486 \pm j\,1.8047$.

In a second step we will move all the zeros of NTF from DC ($z = 1$) by using the equiripple characteristic of the Chebychev polynomials that are polynomials defined by (10).

$$\begin{aligned} T_0(x) &= 1 \\ T_1(x) &= x \\ T_k(x) &= 2T_{k-1}(x) - T_{k-2}(x) \end{aligned} \tag{10}$$

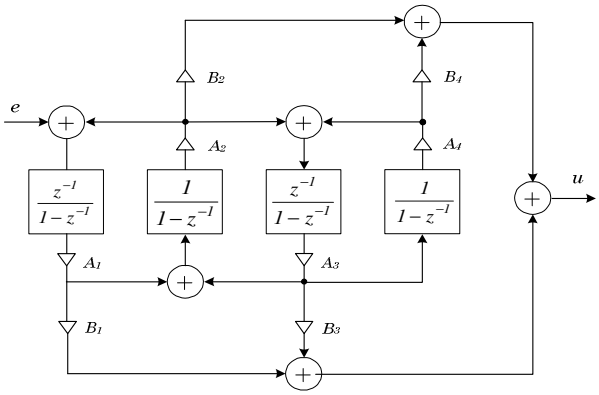

Figure 7. LDI structure of fourth-order ΔΣ modulator filter.

For the case of large oversampling rates, i.e., $f_B << F_s$, where f_B is the baseband frequency and F_s is the sampling frequency, the desired *z*-domain are located at z_i as in (11).

$$z_i = e^{j2\pi X_i (f_B/F_S)} \tag{11}$$

where X_i are the roots of T_n. For the case of $n = 4$, the X_i are equal to $0.9239, -0.9239, 0.3827$ and -0.3827. For $F_s = 13\,MHz$ and $f_B = 104\,kHz$, *z*-domain zeros are at $z_{1,2} = 0.99831 \pm j0.05801$ and $z_{3,4} = 0.99971 \pm j0.024045$.

Then, we will present the LDI structure for $H(z)$ implementation. LDI ladder filters are characterized by their good sensitivity. The calculation of the coefficients A_i and B_i is performed. Then, we try to quantize these coefficients to the nearest power-of-two values. With the quantified coefficients A_i and B_i for 4^{th} order given by Table IV, the poles of $H(z)$, which are also the zeros of the NTF, remain on the unit circle. The proposed single-bit high order digital ΔΣ modulator is then multiplier-free.

TABLE IV. QUANTIFIED COEFFICIENTS A_i AND B_i

A_i	B_i
$A_1 = 2^{-7}$	$B_1 = 2^{6}$
$A_2 = -2^{-4}$	$B_2 = -2^{9}$
$A_3 = -2^{-4}$	$B_3 = 2^{10}$
$A_4 = 2^{-6}$	$B_4 = 2^{14}$

C. Proposed ΔΣ fractional-N synthesis simulation results

We present a set of computer simulations for the main features of ΔΣ modulator, particularly its spectrum purity. A high-level simulation using the dynamic element matching tool Simulink is performed. We created Simulink model for a fourth-order ΔΣ modulator which the LDI structure filter is displayed in Fig. 7. A typical spectrum output is displayed in Fig. 8 and 9 to show our simulation results, for 13 MHz as sampling frequency F_s. The maximum input stable amplitude and the frequency of the ΔΣ modulator sine wave input are respectively 0.7 V and 73 kHz.

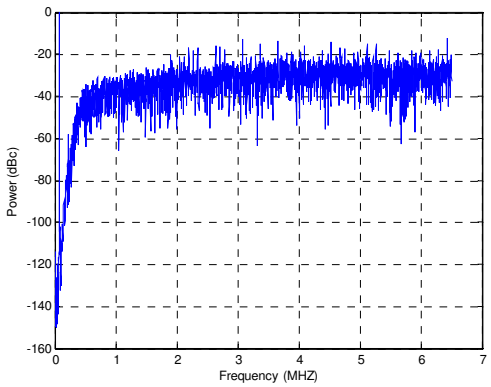

Figure 8. Low-pass ΔΣ modulator measured spectrum.

The proposed ΔΣ modulator randomizes perfectly the division control signal and maintains the same mean value which satisfies the accuracy constraint required in multistandard case. Besides, as we can observe in Table I, GSM phase noise specification is the most severe compared to the other communication standards. According to Fig. 8 and 9, we can see the ΔΣ modulator good performances in terms of spectrum purity. Indeed, ΔΣ modulator noise level is lower than the level $-30dBc/Hz$ at 3 MHz and will be filtered by the multistandard frequency synthesizer loop filter. The simulation results are in good qualitative agreement with specifications in Table II. It represents a first attempt and we have preliminary information on the sensitivity of the results to various model parameters. We have only considered here the fourth-order ΔΣ modulator. Higher orders may lead to significant contributions and should be simulated.

An additional set of simulations of the ΔΣ modulator controlling the multistandard frequency synthesizer were achieved. The prototype enables to generate carrier frequencies between 3100 MHz and 4100 MHz. The tuning range is divided in 16 bands as described in [17]. Simulation was accomplished for a reference frequency f_{REF} supplied by a 13 MHz sine wave oscillator and a passive 4th order loop filter with 262 kHz as bandwidth. The smallest output frequency step is 198 Hz which satisfies different considered standards channel spacing.

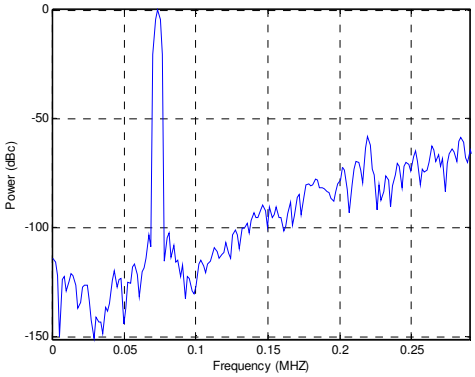

Figure 9. Low-pass ΔΣ modulator measured spectrum in signal band.

The Simulink model, given in Fig. 10, presents the synthesizer that delivers the synthesized frequency F_c as in (12).

$$F_c = synFr.(N + synM) \tag{12}$$

which is equal to 3617.9 MHz and with $synFr$ the reference frequency and $synM$ the fractional part. For multistandard aspect, we need to replace the VCO by the proposed one in the reference [17]. In this configuration, the PLL is locked from 3600 to 3617.9 MHz within 1 kHz tolerance in 34 μs locking time. N is fixed at 278 and the fractional part is equal to 0.3. The loop filter is taken regarding 4th order Butterworth approximation. The amplifier has a gain K given in (13).

$$K = 2(synFr(N + synM) - synFq)/synSen \tag{13}$$

with $synSen$ the VCO sensitivity and $synFq$ the VCO quiescent frequency equal to the frequency of the oscillator output when the input signal is zero. Both of the spectra at the VCO output and at the divider output are respectively presented in Fig. 11 and Fig. 12.

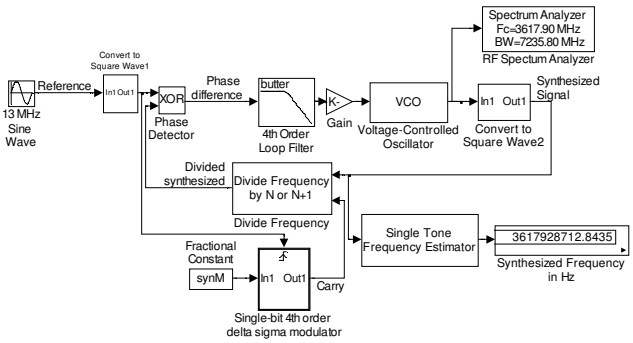

Figure 10. Simulink model of the digital 4th order delta sigma modulator for fractional-N frequency synthesizer.

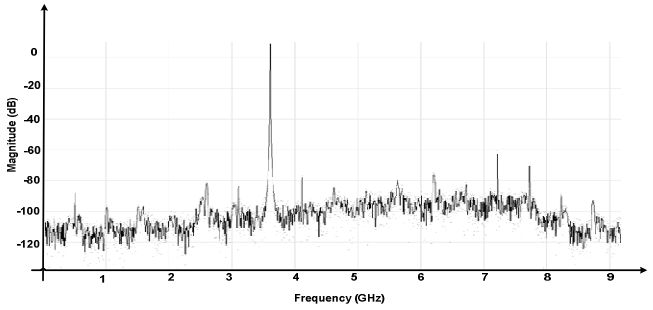

Figure 11. Spectrum at the VCO output.

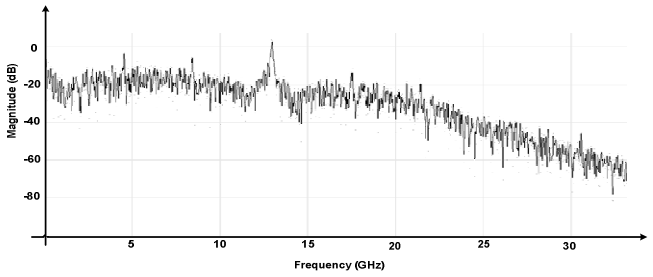

Figure 12. Spectrum at the divider output.

From Fig. 11, we verify that the noise phase level $-141\ dBc/Hz$ at $3\ MHz$ offset is satisfied. From Fig. 12, we observe that the noise phase level is very important. This quantity is filtered thanks to the 4^{th} order loop filter characterized by a $262\ kHz$ cut-off frequency. The output of the filter is then amplified and Fig. 13 illustrates a typical simulated VCO input voltage after switching order. Further simulation results are obtained for transition between two 200-kHz spaced synthesized frequencies. Required locking time is about $58\ \mu s$ when a $3610.1\ MHz$ frequency is synthesized after a $3617.9\ MHz$ frequency. Fractional number N_{fract} changes from 278.3 to 277.7. To synthesize standards required frequencies, the VCO needs to be controlled digitally to deliver frequencies in the standards range as cited in previous work [17].

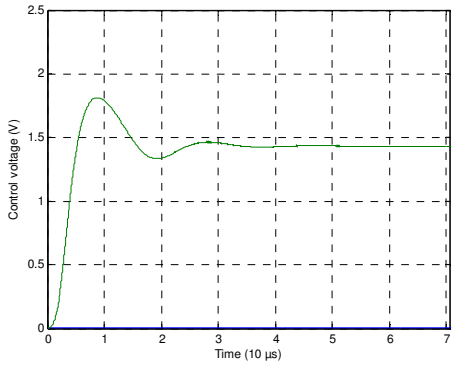

Figure 13. Simulated VCO input voltage.

V. CONCLUSION

In this paper, we have proposed an innovative stable architecture of digital ΔΣ modulator employed in multistandard frequency synthesis which offers simplicity and low power consumption. At first, we investigated the general dilemma of frequency synthesis. After that, we uncover multistandard PLL-based frequency synthesizer requirements. Finally, a design of the proposed digital ΔΣ modulator is achieved. It is shown that the proposed ΔΣ modulator presents good performances in terms of spectrum purity, accuracy and fast locking time.

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