Pseudorandom Direct Sampler for Non-Uniform Sub-sampling Architecture in a Multistandard Receiver

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Abstract — **In this paper, a Non-Uniform Sampling (NUS) technique for down-conversion stage in a multistandard radio receiver is proposed. For both narrowband and wideband standard processing, NUS promises relaxing system design constraints, decreasing the sampling frequency as well as reducing power consumption. A non-uniform clock generator, called Pseudorandom Direct Sampler (PDS), is described. PDS is used to non-uniformly control the Analog-to-Digital Converter (ADC) performing IF sub-sampling in proposed GSM/UMTS/WiFi multistandard receiver architecture. PDS architecture is based on using modified Direct Digital Synthesizer (DDS) including pseudorandom behavior. A 90-nm CMOS FPGA based prototype of PDS reveals an internal clocking up to 350 MHz and a power consumption lower than 4 mW.**

Index Terms — **Multistandard receiver, Non-Uniform Sampling, Sub-sampling, Direct Digital Synthesizer.**

I. INTRODUCTION

In communication engineering, the Software Radio (SWR) becomes an unavoidable concept to face challenging constraints of today's requirements. This concept has been first introduced by Josef Mitola in early 1990's [1]. SWR aims to perform radio receiver functions in digital domain instead of analog domain to enhance the receiver reconfigurability behavior. In SWR concept, terminals require powerful processors performing radio functions, large dynamic range for wideband data conversion and smart reduced RF front-end.

Due to technology limits and constraints, the SWR is not feasible today. In fact, the digital stage exhibits high power consumption to achieve SWR required radio functions [2]. The ADC state-of-the-art shows that SWR requirement for data conversion is not possible [3]. RF front-end reconfigurability is not allowed with actual integrated circuit technologies [2]. The adopted concept is Software Defined Radio (SDR) dealing with relaxed specifications than SWR by allowing more radio functions in analog domain [4].

In literature, architectures were proposed for SDR multistandard receiver. First category was mixer-based architecture which quickly reveals many weaknesses as image rejection, Local Oscillator (LO) leakage and flicker noise [5]. RF sub-sampling architectures were then introduced in order to avoid first category weaknesses. Nevertheless, the clock jitter and the high constraints on anti-aliasing filters (AAF) might lead to a moderate performances receiver [6].

A good approach could be a compromise between the two architecture categories. An hybrid receiver architecture including mixer-based down-conversion followed by a sampling-based down-conversion may have better results. In fact, clock jitter noise is avoided while using mixer-based down-conversion from RF to Intermediate Frequency (IF). In order to relax anti-aliasing filter constraints for the second down-conversion stage, a new technique, Non-Uniform Sampling, is introduced.

This paper encloses three parts. In section II, multistandard SDR receiver architectures are discussed and NUS-based receiver architecture is proposed. Section III is devoted to the choice of suitable NUS scheme to achieve alias-free sampling. A relaxed anti-aliasing filter design is presented to illustrate NUS advantage for GSM/UMTS/IEEE802.11a multistandard receiver. In section IV, a new non-uniform clock generator, called Pseudorandom Direct Sampler (PDS), is presented to perform suitable sampling scheme. Design implementation and validation results of PDS are presented.

II. PROPOSED NUS-BASED RECEIVER ARCHITECTURE

Conventional receivers are based on several analog mixers to down-convert RF signal. Most of these receiver architectures, especially heterodyne architectures, are neither integrated nor reconfigurable [2]. Different receiver architectures have been proposed for SDR concept. Two categories could be depicted: single mixer-based receiver architecture and sampling-based receiver architecture [7-8]. Due to high constraints on some receiver stages, no GSM/UMTS/WiFi multistandard SDR receiver has been totally realized in CMOS technology for both categories. In order to design a feasible multistandard SDR receiver, we propose an hybrid mixer- and sampling- based architecture while using NUS technique.

A. Homodyne/low-IF receiver architecture

The homodyne architecture has been introduced as a solution to superheterodyne non-reconfigurability and its

doi:10.4304/jcp.5.10.1478-1485

analog circuit crowdedness. It contains reduced analog components. This architecture allows RF signals down-conversion of RF signals in baseband using a single quadrature mixing [9]. However, homodyne receiver performances could be deteriorated by mainly two problems. The first problem is caused by isolation lack between mixer input and LO. A signal will be then self-mixed producing a null frequency signal. This problem is known as DC-offset. The second problem is related to the noise level in CMOS technology. The band from DC to 50 kHz presents an important noise especially for narrow band standards (GSM). This problem is known as flicker noise. This noise could be convoyed by BiCMOS made mixer. However, CMOS integrated circuits are highly recommended for lower cost and more integration than BiCMOS process.

One attractive solution was low-IF receiver architecture. This architecture was proposed to avoid above problems. However, image rejection problem will occur. Since quadrature mixing is still performed near RF frequencies, I/Q mismatch happens. This leads to image rejection limitations of Weaver/Hartely methods for low-IF receiver.

Combined homodyne/low-IF architecture is recently proposed [9]. The homodyne architecture is used for the wideband standards such as UMTS or WLAN 802.11.a, whereas, the low-IF architecture is preferred for narrow-band standards such as GSM or DCS1800 in order to reduce the flicker noise impact [10]. Only system level analysis is presented, the technology feasibility is under study.

B. RF sub-sampling architecture

To overcome mixers and avoid their drawbacks, RF signal down-conversion could be performed by bandpass sampling. In fact, by sampling RF signal at frequency carrier f_c by a frequency f_s lower than f_c, many replicas are produced. A filter is then applied to select the closest replica to the baseband localized at the Intermediate Frequency f_{IF}. Figure 1 explains the sub-sampling technique for frequency down-conversion [11].

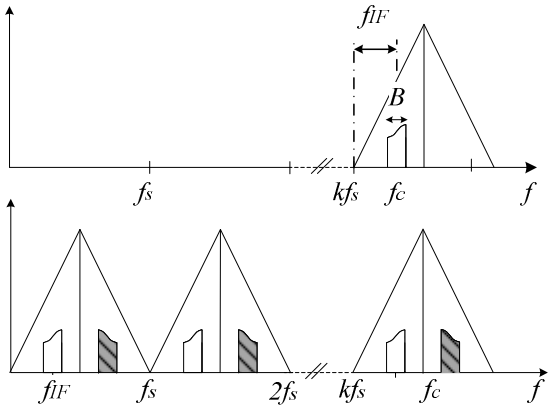

Figure 1. Sub-sampling technique for frequency down-conversion.

To realize RF sub-sampling architecture, a sample and hold circuit must be integrated. This circuit converts an analog signal from continuous time to discrete time. Such component is designed by NMOS transistor and a holding capacity C_H. The NMOS transistor is used as a sampling switch. Transistor conducting state represents the sampling mode; the blocking state represents the blocking or holding mode. In the case of RF sub-sampling architecture, mainly all components are integrated in CMOS and reconfigurable. Such architectures could be suitable for SDR concept [6, 8].

However, the sampling stage could introduce noises. Due to the jitter of the high frequency clock generators (typically All Digital Phase Locked Loop, ADPLL), the sampling instants could be erroneous. This leads to in-band noise increase and consequently Signal-to-Noise Ratio (SNR) degradation. In addition, charge injection in C_H with R_{on} resistor presence on NMOS transistor limit frequency sampling choice. The wideband thermal noise generated by switched capacitor circuit is replicated while sampled. Based on the use of first replica obtained by sub-sampling, a high constrained AAF are required to move out interfering spectrum parts (blockers). These filters are very selective, high order and not feasible.

In the next section, we propose an hybrid mixer- and sampling-based receiver architecture with relaxed constraints by using NUS technique with non-uniform spaced sampling instants.

C. NUS-based architecture

The proposed multistandard SDR receiver architecture is presented by Figure 2.

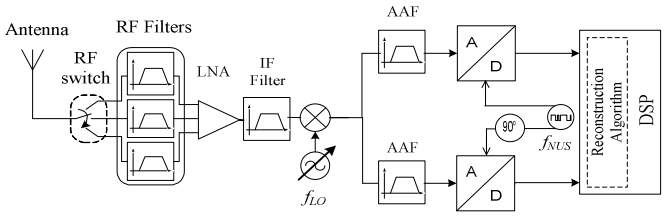

Figure 2. Architecture of the proposed receiver.

After its reception via the antenna, the signal is first filtered by adequate RF filters in order to select the signal band and to attenuate blockers outside the received band for each standard [12]. Next, the signal is amplified by wideband multistandard Low Noise Amplifier (LNA) [13] then filtered in order to avoid image problem while down-converting the signal by multistandard CMOS mixer . The considered mixer needs a variable local oscillator frequency f_{LO} [14]. Its purpose is to down-convert any channel of GSM/UMTS/802.11a standard to the same intermediate frequency f_{IF}. The signal will be then down-converted to baseband and digitized by an IF sub-sampling ADC. The ADC is controlled by a non-uniform clock that delivers non-uniformly time-spaced samples. In order to eliminate spectrum overlapping, it is mandatory to apply AAF before the ADC in order to cut off all undesirable spectrum aliases. With the objective of keeping on remaining baseband processing, a numerical reconstruction algorithm is required to convert non-uniformly time-spaced samples to uniformly time-spaced ones [15].

By down-converting the RF signal to an intermediate frequency f_{IF}, the DC-offset problem is eliminated. The CMOS mixer is devoted to down-convert all channels to a

fixed value of $f_{IF} = 600\,MHz$. This is ensured by the use of a tunable Phase Locked Loop (PLL) that will generate a signal at a frequency f_{LO} given by equation (1).

$$f_{LO} = |f_c - f_{IF}| \tag{1}$$

To get the signal down-converted to the baseband, a second frequency transposition must occur. This will be achieved thanks to a 16-bit IF sub-sampling ADC. In this case, clock jitter effect is decreased since sub-sampling is performed at IF frequency instead of RF frequency. In addition, flicker noise problem will be avoided since we will have a digital baseband signal.

The most important NUS technique feature is to perform alias-free sampling [16]. In the proposed architecture in Figure 2, the ADC is non-uniformly controlled to perform sub-sampling. This will relax constraints on AAF then it will be feasible and conventional multi-cadence analog processing is avoided. In the next section, we describe the most suitable NUS scheme for proposed architecture.

III. NON-UNIFORM SCHEMES ADAPTED FOR NUS-BASED RECEIVER ARCHITECTURE

The NUS is a kind of signal processing in which irregular sampling sequences are considered. NUS converts continuous analog band-pass signal into its discrete representation. Assume a continuous signal $x(t)$, its discrete representation $x_s(t)$ is given by equation (2).

$$x_s(t) = \sum_{k=-\infty}^{+\infty} x(t_k)\delta(t - t_k) \tag{2}$$

In the uniform sampling case, t_k is equal to a multiple of $T_{US} = 1/f_{US}$, where f_{US} is a frequency satisfying Shannon theorem [17]. In NUS case, sampling instants are defined as $t_k < t_{k+1}$ with $T_{NUS} = 1/f_{NUS}$ is the mean of the sampling period.

In [18-20], some definitions and conditions for alias-free sampling have been presented. In [21], authors proved that the condition to eliminate aliases using NUS is to have a punctual stationary sequence of non-uniform instants. In terms of probability density function, a sequence is punctual stationary if the t_k probability density functions $p_k(t)$ satisfy the equation (3).

$$p(t) = \sum_{k=0}^{+\infty} p_k(t) = f_{NUS} = \frac{1}{T_{NUS}} \tag{3}$$

NUS distinguishes different types of schemes according to the sampling instant sequence definition. Three main types are considered.

A. Random sampling schemes

The most valuable and considered schemes [21, 22] are the Jittered Random Sampling, JRS, and the Additive Random Sampling, ARS. The JRS is the addition of random times τ_k to uniform sampling instants. Sampling instants verify equation (4).

$$\begin{gathered} t_k = kT_{NUS} + \tau_k, 1 \le k \le n \\ with\ E[t_k] = kT_{NUS}\ and\ Var[t_k] = \sigma^2 \end{gathered} \tag{4}$$

where the τ_k times are random independent and identically distributed (*i.i.d.*) variables with a probability density $p_1(\tau)$, a zero mean and a variance σ^2. For $k = 0$, the t_0 probability density is $p_0(t) = \delta(t)$. The probability density function of the k^{th}sampling instant is given by (5).

$$p_k(t) = p_1(t - kT_s)\ for\ 2 \le k \le n \tag{5}$$

For ARS, the sampling instants are constructed by adding the random time to the previous sampling instant. Equation (6) gives non-uniform instants towards ARS scheme.

$$\begin{gathered} t_k = t_{k-1} + \tau_k = t_0 + \sum_{i=1}^{k} \tau_i, 1 \le k \le n \\ \text{with } E[t_k] = kT_{NUS} \text{ and } Var[t_k] = k\sigma^2 \end{gathered} \tag{6}$$

where the τ_k times are random *i.i.d.* variables with a probability density $p_1(\tau)$, a T_{NUS} mean and a variance σ^2. For $k = 0$, the t_0 probability density is $p_0(t) = \delta(t)$. The probability density function, given in (7), is the convolution product of the k^{th} sampling instant.

$$p_k(t) = \underset{i=1}{\overset{k}{\circledast}}\ p_1(t) \tag{7}$$

In order to satisfy alias-free sampling (3) and to avoid sampling at t_k before t_{k-1}, random times τ_k follow a distribution over $[-0.5T_{NUS}, 0.5T_{NUS}]$ for the JRS scheme and a distribution over $[0.5T_{NUS}, 1.5T_{NUS}]$ for the ARS scheme. Then, we define the statistical parameter σ/T_{NUS} to verify this condition on the sampling instants occurrence.
The stationary condition depends on the chosen distribution $p_1(\tau)$. In fact, from (5), all $p_k(t)$ are deduced from a kT_{NUS} time shifting. Therefore, it is simple to notice that the JRS scheme with a uniform distribution over $[-0.5T_{NUS}, 0.5T_{NUS}]$ is a stationary process thanks to equation (8).

$$p_k(t) = \frac{1}{T_s}\ with\ -k\frac{T_s}{2} \le t < k\frac{T_s}{2} \tag{8}$$

The maximum statistical parameter σ/T_{NUS} for the JRS scheme in case of uniform probability density over $[-0.5T_{NUS}, 0.5T_{NUS}]$ is computed in (9).

$$\frac{\sigma}{T_{NUS}} = \frac{\left(0.5T_{NUS} - (-0.5T_{NUS})\right)/\sqrt{12}}{T_{NUS}} = 0.2887 \tag{9}$$

Besides, we present in Figure 3 punctual probability densities for the JRS scheme with a Gaussian distribution for some values of σ/T_{NUS}. The $p(t)$ satisfies (3) only for σ/T_{NUS} values higher than 0.5.

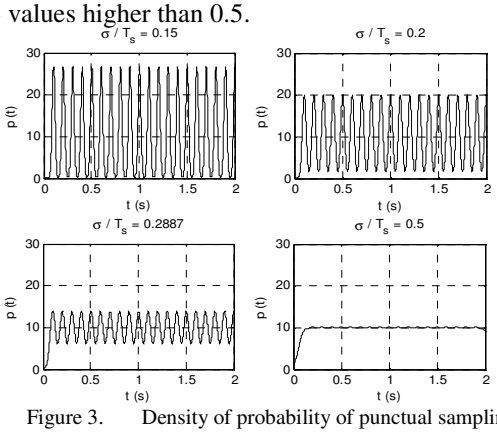

Figure 3. Density of probability of punctual sampling $p(t)$ in the case of JRS mode with a Gaussian distribution for different values of σ/T_{NUS} for $T_{NUS} = 0.1\ s$.

The ARS scheme is particularly interesting because it satisfies stationary condition and therefore alias-free sampling whatever the density distribution is [21]. For example, stationary process is obtained for Gaussian density function for some values of σ/T_{NUS} as presented in Figure 4.

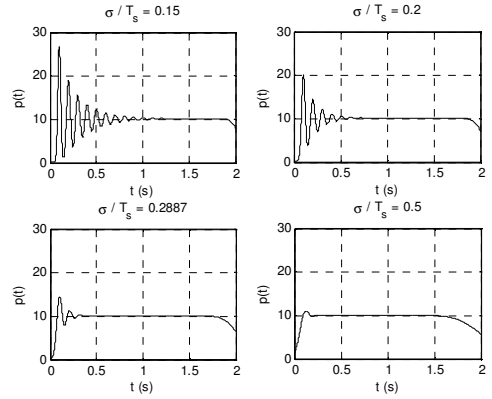

Figure 4. Density of probability of punctual sampling $p(t)$ in the case of JRS mode with a Gaussian distribution for different values of σ/T_{NUS} for $T_{NUS} = 0.1\ s$.

Although interesting, ARS and JRS NUS schemes are not adapted to the proposed receiver. In fact, it is difficult to implement such continuous-time random distribution. Therefore, another scheme is proposed. It considers quantized time sampling instants.

B. Time Quantized Pseudorandom Sampling schemes

Random sampling is not convenient to generate and precisely recover uniform sampling instants. In most random sampler implementations, the sampling instants are, either randomly or pseudorandomly, analogically generated [23]. However, these kinds of generator need a Time-to-Digital Converter (TDC) to quantize the random sampling instants before the digital reconstruction algorithm. Hence, the Time Quantized Random Sampling (TQ-RS), applied either to JRS or ARS, is more devoted to implementation. In fact, it considers quantized sampling instants with quantization step Δ defined by (10).

$$\Delta = T_{NUS}/q_T \tag{10}$$

Where q_T is the quantization factor. Each δt_k, as given in (11), will be then quantized and approximated to $\delta t_{k,q}$ the closest Δ multiples as detailed in (12).

$$\delta t_k = t_k - t_{k-1} \tag{11}$$

$$\delta t_{k,q} = n\Delta \quad if\ (n-1/2)\Delta < \delta t_k \leq (n+1/2)\Delta \tag{12}$$

Figure 5 gives an example of time quantized random sampling instants.

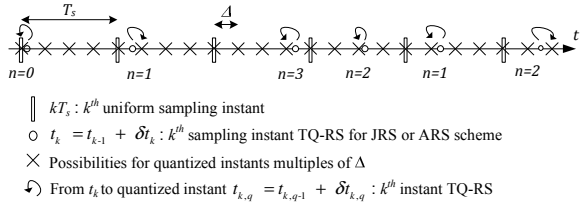

Figure 5. TQ-RS scheme description for $q_T = 4$.

One more adapted scheme to implementation is the pseudorandom version of the TQ-RS scheme. Figure 5 could illustrate the Time Quantized PseudoRandom Sampling (TQ-PRS) scheme by considering the rank n, in the k^{th} interval, as a pseudorandom number with a cycle length equal to q_T.

Similar simulation results, for ARS and TQ-PRS with q_T equal to 8, 16 and 32, were obtained for cubic spline interpolation [24]. Therefore, the use of TQ-PRS scheme use instead of TQ-RS and ARS schemes upstream from reconstruction performs same results and true pseudorandom variable is no more needed.

Assuming TQ-PRS adapted to JRS scheme with uniform distribution density, the obtained statistical parameter σ/T_{NUS} is given in (13) and is presented in Figure 6.

$$\frac{\sigma}{T_{NUS}} = \frac{1}{q_T}\sqrt{\frac{{q_T}^2 - 1}{12}} \tag{13}$$

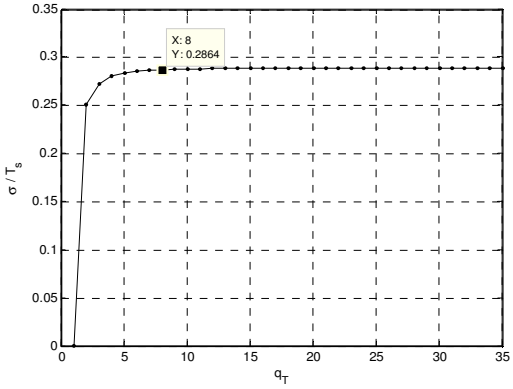

Figure 6. Statistical parameter versus q_T.

We notice choosing q_T equal to 8 performs a scheme with a 1%-near statistical parameter to theoretical value computed in (9).

C. Advantage of using Non-Uniform Sampling

In uniform sampling, in the spectrum band $[0, q_T f_{NUS}]$, aliases are located at frequencies $q_T f_{NUS} - f_{IF_{SS}}$ and $k f_{NUS} \pm f_{IF_{SS}}$ for k between 1 and $(q_T - 1)$ where $f_{IF_{SS}}$ is the intermediate frequency of the sub-sampled signal and f_{NUS} is the mean sampling frequency. When we non-uniformly sample with TQ-PRS scheme, we obtain one alias at a frequency equal to $q_T f_{NUS} - f_{IF_{SS}}$, other aliases are reduced and some wideband noise is added to the spectrum. Figure 7 shows the NUS anti-aliasing feature.

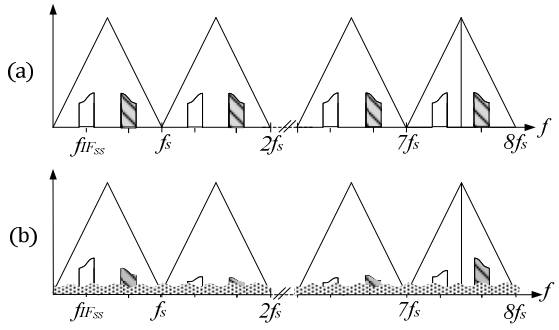

Figure 7. Resulted spectrum after uniform sampling (a) and TQ-PRS non-uniform sampling (b).

This wideband noise is suppressed with a reconstruction algorithm [15]. As presented in Figure 7, and in order to have no overlapping, the NUS mean sampling frequency has to be at least equal to Nyquist frequency. For the proposed case, where $f_{IF} = 600\,MHz$ and the maximum channel bandwidth B for the three supported standard is equal to $16.6\,MHz$, we recommend to choose a mean sampling frequency $f_{NUS} = 75\,MHz$ to guarantee a minimum Over-Sampling Ratio for all standards which will help to decrease constraints on AAF Filter.

To demonstrate the advantage of NUS, we propose to compare the AAF filter order in the case of uniform sampling and non-uniform sampling at $f_{NUS} = 75\,MHz$. The AAF filter has to cut off all interfering signals that could fall down into the signal band after sampling. In our case, the AAF filter is a band-pass that selects only the signal at f_{IF}. Figure 8 presents the AAF response as well as the cutoff and stop-band frequencies.

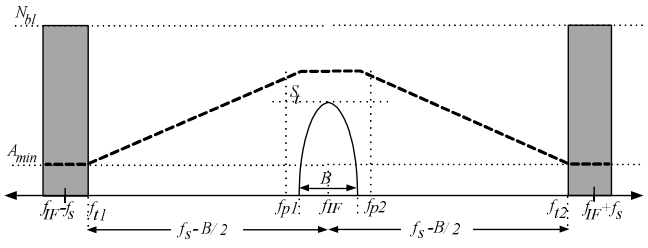

Figure 8. AAF responses and parameters.

The cutoff frequencies f_{p_1} and f_{p_2} must be less than half the useful band B with a margin of 30% [25]. The stop band frequency must to be at most at $f_s - B/2$ from f_{IF} to guarantee the rejection of the nearest replica. OSR is introduced to measure the NUS effect on the resulted spectrum given an intermediate frequency f_{IF} and a sampling frequency f_{NUS}. In fact, replicas are attenuated by Att_{NUS} given by equation (14) [21, 26].

$$Att_{NUS} = 10.log_{10}\left(\frac{2N(1-g) - 2g(1-g^N)}{N^2(1-g)^2}\right) \qquad (14)$$

with $g = exp(-2\pi^2 f_{NUS}^2 \sigma^2) = exp(-2\pi^2 \sigma^2 / T_{NUS}^2)$ and N the number of point required to represent the power density spectrum.

To compute Butterworth filter order, the minimal attenuation A_{min} has to be specified. This parameter depends, as shown by equation (15) of the blocker level to attenuate, N_{bl}, and the signal test power, S_t, the required Signal-to-Noise Ratio to demodulation SNR_{out}.

$$A_{min} = N_{bl} - S_t + SNR_{out} \qquad (15)$$

In the case of NUS, replicas are attenuated by Att_{NUS}, the minimum attenuation formula is then given by equation (16).

$$A_{min} = N_{bl} - S_t + SNR_{out} - Att_{NUS} \qquad (16)$$

Parameter computed values are summarized in Table I. We can notice that using NUS sampling allows reducing AAF filter order from 6 to 4.

TABLE I. COMPARISON BETWEEN UNIFORM SAMPLING AT f_{US} AND NON-UNIFORM SAMPLING AT MEAN SAMPLING FREQUENCY f_{NUS}

		GSM		UMTS		IEEE802.11a	
Sampling technique		US	NUS	US	NUS	US	NUS
OSR		375		19.53		3	
Cutoff frequencies (MHz)	f_{p_1}	589.21		589.21		589.21	
	f_{p_2}	610.79		610.79		610.79	
Stop-band corner frequencies (MHz)	f_{t_1}	525.1		526.92		533.3	
	f_{t_2}	674.9		673.08		666.7	
N_{bl} (dBm)		-23	-23	-44	-44	-47	-47
Att_{NUS} (dB)		-	29.47	-	16.65	-	8.569
Stop-band attenuation (dB)		85	55.53	51.8	35.16	41.6	33.03
Butterworth filter order		6	4	4	3	3	3

The non-uniform generator, has to provide a non-uniform signal with a mean sampling frequency equal to $f_{NUS} = 75\,MHz$. To benefit from the proposed NUS-based receiver architecture, the generator have to consider a TQ-PRS scheme with a quantization factor $q_T = 8$ to be reconfigurable in order to satisfy SDR conditions. We study existing non-uniform signal sampler and deduce their limits to control the IF sampling ADC in the proposed NUS-based architecture. Hence, we propose a new non-uniform generator, the Pseudorandom Direct Synthesizer, and present some implementation and validation results.

IV. PSEUDORANDOM DIRECT SAMPLER

A. Existing non-uniform signal sampler

In [27], non-uniform sampler design is based on chaotic oscillators implemented with discrete components. This design solution is not appropriate for monolithic integrated SDR receiver baseband stage. Besides, the generation of random continuous-time signal needs an extra component TDC (Time-to-Digital Converter) for digital signal reconstruction in DSP [16]. The difference between sampling instants and reconstruction instants returns inaccurate reconstruction results.

Nevertheless, non-uniform ring oscillator proposed in [28] seems to be an interesting solution for SDR receiver baseband stage. The drawback is the important length of inverters and dependence on the chosen technology since the inverter W/L CMOS parameter should be reworked to get the same inverter delay.

In [24], a more convenient pseudorandom sampler has been proposed. The Pseudorandom Signal Sampler (PSS) is an oscillator that promises a deletion of overlapping between generated phases, a low power consumption, a small die area and a time-quantization accuracy for digital reconstruction. PSS implementation proves that, for a main clock at $3.2\,GHz$, signals at mean sampling frequencies up to $200\,MHz$ are generated in 65 nm CMOS technology. These results are optimistic for future standards and services specifications.

However, in order to ensure the no overlapping characteristic, PSS apply a mechanism that allows having

only one positive non-uniform clock edge by a mean sampling period. For that, PSS impacts the clock generation process and changes indirectly the value of the instantaneous sampling period. Therefore, PSS has not a direct control on the instantaneous output periods and instantaneous output duty cycles. The mean sampling period varies either if we change the main clock or if we choose q_T equal to 8, 16 and 32. In addition, non-uniform clock generator has to be reconfigurable in order to be reused in different architectures based on NUS technique. Because of the lack of reconfigurability of the PSS, another way of clock generation is proposed in this work promising time-quantization accuracy, low power consumption and high reconfiguration.

B. Proposed PDS architecture

The proposed oscillator, the Pseudorandom Direct Sampler (PDS), digitally and pseudorandomly synthesizes frequencies. Its concept is close to the Digital Direct Synthesis (DDS) one [29]. The DDS, consists of a phase accumulator, a phase to amplitude converter (conventionally a sine ROM), a Digital-to-Analog Converter (DAC) and a filter to suppress signal harmonics as shown in Figure 9 [30-32].

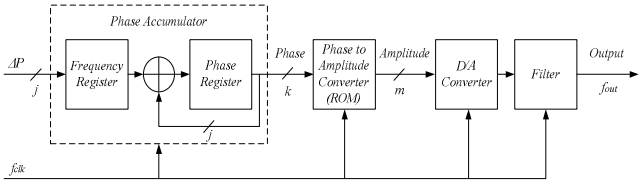

Figure 9. Synoptic of a Direct Digital Synthesizer.

The phase accumulator is a j-bit frequency register that stores a digital phase increment word ΔP, a j-bit full-adder and a phase register [30]. At each clock pulse, the digital input phase increment word is added to the phase register value. This value indexes a sine wave value in the ROM.
The PDS purpose is to generate a signal having a variable frequency following a precise distribution. To perform such target, we have chosen to consider a DDS concept with a pseudorandom access to its phase to amplitude converter. The proposed architecture is presented in Figure 10. PDS consists of a Linear Feedback Shift Register (LFSR), a phase accumulator and a phase-to-amplitude converter [29].

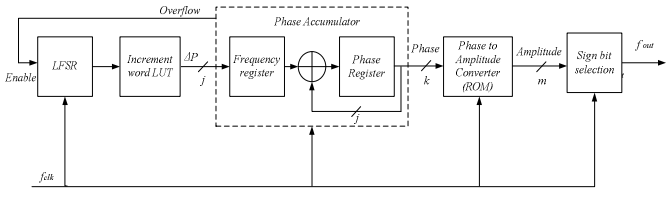

Figure 10. PDS synoptic block diagram.

An LFSR generates a pseudorandomized sequence that commands the phase increment LUT and so the ΔP value, where ΔP is the phase increment word. Hence, according to every ΔP, PDS will generate a sine wave with different frequencies. The clock generation consists on selecting the sign bit of the sine wave.

In order to get *i.i.d.* variables, LFSR have to produce all possible phases. Therefore, a primitive characteristic polynomial has to be selected. If we quantize the sampling timing axis with a quantization order $q_T = 8$, we will have to generate 7 different phases corresponding to the localization of the non-uniform samples on the timing axis. Consequently, we have to choose an LFSR having 3 flip-flops in order to have $p = 2^3 - 1 = 7$ phases. The third-order primitive characteristic polynomial chosen for the proposed LFSR is given by equation (17). According to these conditions, the selected LFSR is presented in Figure 11.

$$P(\mathrm{x}) = \mathrm{x}^3 + \mathrm{x} + 1 \tag{17}$$

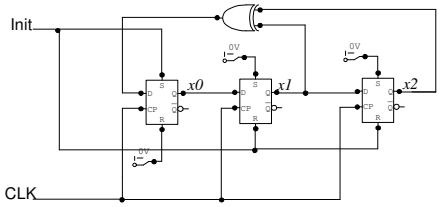

Figure 11. LFSR Architecture

When enabled and for $q_T = 8$, the LFSR generates an integer i varying from 1 to 7. In the first LUT, the integer i is converted into the phase increment word corresponding to the variable clock period $T_i = i\,\delta$ where δ is a variable clock period multiplier equal to $10\,ns$. Table II resumes possible period generated by PDS.

TABLE II. PDS GENERATED PERIODS FOR $q_T = 8$

Instantaneous Period T_i	Period T_i (ns) for $f_{NUS} = 75\,MHz$	ΔP	N_{sample}
$T_{NUS}/4$	3.33	64	2
$T_{NUS}/2$	6.66	32	4
$3\,T_{NUS}/4$	10	22	6
T_{NUS}	13.33	16	8
$5\,T_{NUS}/4$	16.66	13	10
$6\,T_{NUS}/4$	20	11	12
$7\,T_{NUS}/4$	23.33	9	14

To optimize the Phase to Amplitude converter length, many constraints must be verified. In fact, recalled samples number has to be enough in order to enable the detection of sine wave sign variation for all considered frequencies. Also, the ROM length has to allow the scan of quantized sine wave values with different phase increment word for each frequency to be generated. In order to satisfy this condition, a 128 ROM has been selected. Phase increment word and samples number for this case are summarized in Table II.

Word length in the ROM depends on the maximum of samples generated during a period. The number of bits is calculated according to equation (18).

$$i = log_2\left(\frac{N_{sample}}{4}\right) + 1 \tag{18}$$

where N_{sample} refers to the number of samples required to construct the period T_{max}. This number has to be divided by

4 due to the sine wave quarter symmetry. In the studied case, we have to generate a 3-bit length word.

C. PDS implementation and validation results

The PDS has been implemented on Altera using VHDL. In this section, we will present and discuss implemented PDS output. This signal will drive the sampling process of a 10 bit sine wave and be compared to results got using a MATLAB generated sampling instant sequence as well as uniform sampling instants. The test was made using a sine wave signal localized in a Wi-Fi channel. After the first down-conversion, this frequency signal is equal to $610\,MHz$. The mean sampling frequency for NUS is $f_{NUS} = 75\,MHz$. After the NUS stage, the signal is down-converted to $10\,MHz$. The same signal test was used for the uniform sampling at f_{NUS}. The aliasing reduction feature of NUS is shown in Figure 12. The NUS replicas number and power spectral density are reduced compared to the uniform sampling ones.

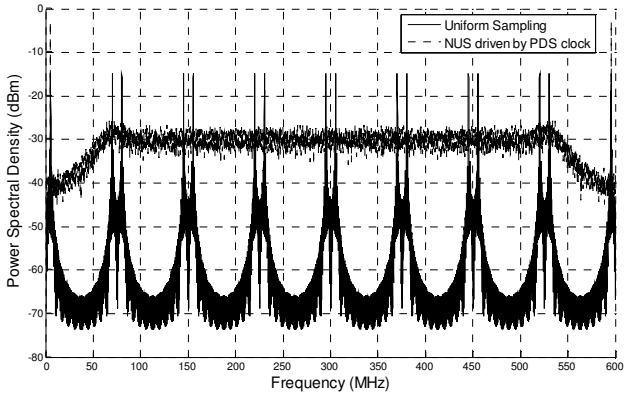

Figure 12. Power spectral density of sine wave non-uniformly sampled using PDS sequence versus sine wave uniformly sampled.

According to Table II, PDS generates the non-uniform clock using seven different instantaneous periods varying from 3.33 to $23.33\,ns$. The clock frequency needed for such result is computed regarding the number of samples N_{sample} read from the Phase-to-Amplitude Converter and regarding the required mean sampling frequency f_{NUS}. Hence, the required clock frequency is the multiplication of these two parameters $f_{clk} = N_{mean} * f_{NUS}$. where N_{mean} is the mean of the number of samples. In the studied case, N_{mean} is equal to 8 therefore required $f_{clk} = 600\,MHz$. PDS has been implementation using Stratix family; results are presented by Figure 13.

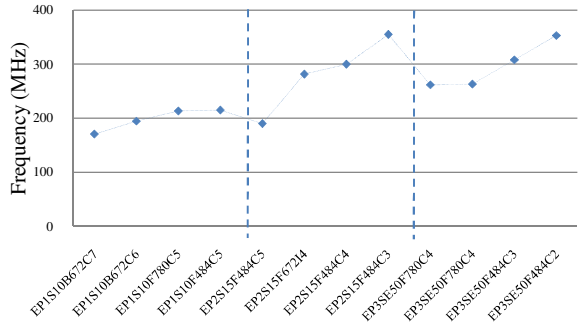

Figure 13. PDS maximum clock frequencies.

Using the best device in terms of performances, PDS principle clock reaches $354.9\,MHz$. The required performances could not be reached using $90\,nm$ FPGA implementations. Nevertheless, an ASIC implementation could probably give better performances. Other configurations of PDS could be obtained by simply change the values on the increment word LUT. PDS is a low power consumer. Its dynamic power consumption is given by Figure 14.

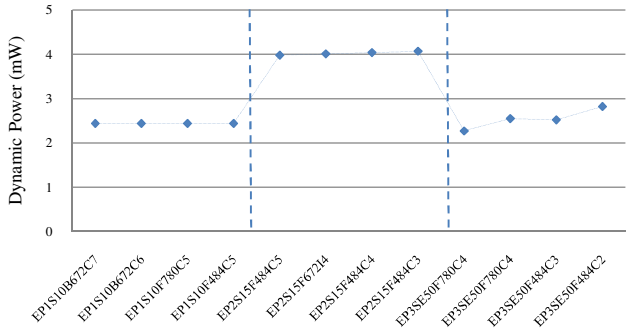

Figure 14. PDS Dynamic power consumption.

Thanks to its small power consumption, PDS circuit could be applied for multistandard receiver in order to relax constraints on filters while maintaining basically the same consumption level of the clock generation.

V. CONCLUSION

In this paper, a new solution for Non-Uniform Sampling control has been presented. A multistandard receiver architecture was first proposed. Its adaptability to SDR context was discussed and the use of NUS as an anti-aliasing technique was introduced. Then the choice of the implemented NUS scheme as well as the condition to reduce aliasing was argued. The clock generator, the PDS, adapted to the chosen architecture and the selected NUS scheme was presented. The proposed design manages the NUS sampling step in a multistandard receiver.

The PDS delivers a pseudorandom quantized sampling sequence. It encloses a flexible and programmable behavior by being able to process different signals at different mean sampling frequency. This can be done either by changing value or by changing phase accumulator words. Implemented PDS output has a good signal-to-noise ratio when applied to sine wave and a low power consumption values. Now, an ASIC implementation has to be done in order to improve PDS performances. Other possible optimizations of the proposed design are to consider as the quarter sine wave symmetry and the reduction of PDS area.

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