The Design of Serial ATA Bus Control Chip

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Abstract: **In a PC system, External storage interface is still a bottleneck in spite of its continuous improving performance, in contrast to the fast development of CPU, memory, graphic chips. The transfer rate in ATA protocol has been improved drastically from the beginning 3.3MB/s to current 133MB/s, but the plate electrode of a parallel interface is inevitably puzzled by clock skew, which limit the increasing of frequency and transfer rate can not be improved. Serial ATA protocol is compatible with Parallel ATA protocol in software layer. Its transfer rate is improved greatly due to serial interface with embedded clock. This paper will discuss the differences between Parallel ATA protocol and serial ATA protocol, and describe the hierarchical classification of serial ATA protocol model. Last a design for HPT183, a parallel/serial ATA bridge connection chip will be put forward. In high speed serial interface integrated circuit design, the design of high speed serial data recovery circuit is a troublesome task. In this paper an all-digital high speed serial data recovery circuit module for 1.5bps SATA interface implement is introduced. In contract to other design made from analog circuit, this all-digital circuit is an easily implement design and it has lower power consumption and smaller area. This circuit is being implemented in HPT183 chip which is designed and manufactured using a 0.18um CMOS process. At the end the test performance index for this chip is also provided.**

Index Terms: **Serial ATA, Bridge connection chip, SOC design**

I. INTRODUCTION

The demand on wide bandwidth and ease-to-use from new emerging applications promote the development and progress of computer industry. As far as high performance is concerned, the bandwidth of CPU doubles every 18 months. The whole performance of the system, however, is not increased simultaneously. The computer hardware which affects the whole performance not only includes the speed of CPU, but also includes bandwidth of all kinds of bus interface and data processing ability of external equipment, etc. External storage interface equipment is among those mentioned hardware. In a personal computer system, the external storage device we generally use is hard disk, whose techniques are boosted by the increasing speed of CPU, graphic chip and memory. The performance of disk sub-system is always a bottleneck of the whole system. To make the whole system run faster with high efficiency, the speed of CPU, video card and memory must be increased at the same time.

Parallel interface hold the maximum market in the past 15 years. ATA（Advanced Technology Attachment）protocol is established in 1980 with a transfer rate of 3.3MB/s[1]. The transfer rate has been increased to 133MB/s in current ATA PI-7 protocol (Ultra ATA 33/ UATA PI Mode7). It still can not match the developing speed of CPU and memory. Some bottlenecks have appeared in Parallel ATA protocol, which is still popular because of its low cost. The only way to break the transfer limit of parallel ATA is to make a fundamental breakthrough. The emerging of serial ATA protocol drastically alleviates the drive system bottleneck problem.

II. PARALLE ATA INTERFACE AND SERIAL ATA INTERFACE

A. Parallel ATA Interface

The ATA interface protocol has been put forward in the 1980s and become a hard disk connection standard between desktop PC and mobile PC due to its ease-to-use, high performance and low cost. This protocol is also used in the connection between DVD and CD drivers and the motherboard. ATA interface protocol has always increased data transfer rate to meet the demand from industry for higher and higher transfer speed of hard drive. The bandwidth of ATA interface has been promoted greatly from the original less than 3MBps to current maximum 133MBps of burst data transfer rate. To satisfy the requirement for higher performance, other aspects have also been improved in ATA protocol, such as enhanced data transfer mode Ultra DM and ATA PI, which supports DVD/CD application. Specifications for various Ultra ATA interface show in table 1.

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TABLE 1
Specifications for various Ultra ATA interface

Ultra ATA Interface	UDMA Model	Clock Frequency	Data Transfer Rate	Data Link	CRC
Ultra ATA-33	Mode 0	8.33MHz	16.67 MB/S	40pin 40line	Yes
	Mode 1	6.67MHz	26.67 MB/S	40pin 40line	Yes
	Mode 2	8.33NHz	33.33 MB/S	40pin 40line	Yes
Ultra ATA-66	Mode 3	11.11MHz	44.44 MB/S	40pin 80line	Yes
	Mode 4	16.67MHz	66.68 MB/S	40pin 80line	Yes
Ultra ATA-100	Mode 5	25MHz	100 MB/S	40pin 80line	Yes
Ultra ATA-133	Mode 6	33.3MHz	133.2 MB/S	40pin 80line	Yes

Figure 1 shows the data transfer of ultra DMA. When transferring, there is a time interval, which is half a cycle (20ns), between two continuous data transfers cycles. Another half cycle includes Required Setup Time, Required Hold time and Required Max Switching time. Require Hold time refer to the special time to hold the data after transferring. Between two data transfer there is Required Setup Time, during which the preparation for data transfer is got ready. Both Required Setup time and Required Hold Time are 4.8ns in ATAPI-6 and the remaining 10.4ns is Max Stitching Time.

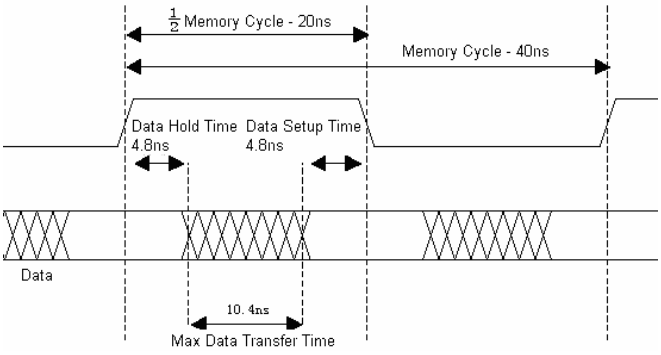

Fig.1 Ultra DMA data transfer Cycle

However, some constrains still exist to affect further increasing the performance.

1) Ultra ATA use traditional non-locking (source synchronizing) clock signal, namely having an extra signal proxy when sending signals, which can avoid broadcasting delay due to the overlong cable and tracing electric resistance. Bidirectional bus with 16bits bandwidth is adapted in ATA protocol, transmitting 2 bytes per clock. It needs the data rate of 50MHz, namely 50Mbps (bit per second), to have a capacity of 100MB/s. It is impossible to increase transfer speed through boosting frequency, since clock signals are easy of access to the edge of skew and action delay[2].

2) The need for 5 voltages will not be met effectively in the future IC with advanced manufacturing techniques. The industry world is changing toward 3.3 voltage signal to keep 5V signal of UDMA 33 from clock skew. The advantage of this change is that signals can be allocated more evenly between high and low voltage, with a 1.5v voltage on each brim, and there are still a great deal of electric charge flowing in the cable.

3) Too much base pins for an ATA interface, which has 26 base pins and need a 40 pins connector, can cause difficulties in chip design and wiring in main board. Wide parallel cable also affects the air flowing in motherboard and makes the design of eliminating of heat more tough.

B. SATA Interface

Serial ATA is a new hard disk interface technology, which was introduced by Intel Company in 2000 to replace the popular used parallel ATA interface. The first official version of Serial ATA was published in 2001 and at the beginning of 2002 the second official version was published by the association of Serial ATA.

Data transfer rate in serial ATA is higher then in parallel ATA, which can reach 150MB/s of burst date transfer rate in SATA 1.0, even higher than the maximum transfer rate of standard parallel ATA can support. In its development roadmap, next version of serial ATA, the data transfer rate supports up to 300MB/s in the, and finally the burst data transfer rate of storage system can reach 600MB/s.

Parallel ATA is totally incomparable with Serial ATA in the aspects system complexity and extension, since Serial ATA need only 4 pins in a ideal state, pin 1 for electricity, pin 2 for ground, pin 3 for data sending and pin 4 for data receiving(as shown in Figure 2). Adopting point to point protocol, there exist no master/slave problems in serial ATA and Each drive have itself bandwidth (shown in Figure 4). This bring two benefits: firstly, user need no trouble to set master/slave jumper wire; secondly, as adapting point to point protocol, single channel is not limited to connect two hard disks, which is undoubtedly a good news for those who need to connect many hard disks.

Serial ATA is software compatible with legacy parallel ATA system and without any changes in operating system and drivers, a new SATA hard ware can be used. But a compatible problem still exists, since Serial ATA adapt a completely different data transfer mode with parallel ATA. They can not directly connected, which will make the present one billion parallel devices incapable of used in serial ATA system until adding a adaptor-like controller.

C. The Layer Model of SATA 1.0: The Physical Layer, the Link Layer, the Transport Layer and Software Layer.

The physical layer is composed of transceiver of low voltage differential signal of two high speed simplex paths [3-6]. There totally are four buses, two buses for one direction. Data are sent in 8B/10B encoding and embedded

clock to reach gigabyte data rate. The bandwidth in version 1.0 is 1.5Gps; moreover, it can reach 3.0Gps in version 2.0 and 6Gps finally.

Physical layer is mainly responsible for such services:

- Sending 1.5Gbps low voltage differential signals.
- Serializing 10bit, 20bit and 40 bit bandwidth parallel data from data link layer.
- Receiving low voltage differential signal of 1.5Gbps
- Extracting data from serial bus.
- Detecting k28.5 comma characters and providing bit synchronizing parallel data out with bandwidth 10bit, 20bit and 40bit.
- Executing proper power up and speed negotiation.
- Passing device state to link layer: device exist, none-exist or exist but failing communication negotiation.
- Optional supported power management mode.

Data link layer ensure the trustily transferring of data packets by keeping integrity of data. It appends the CRC checking of data packet and automatically trying to resending signals when transfer fails. Link layer also handles the receiving and sending of data packet. It sends initial character of control signal from transport layer and receives initial characters from physical layer and converts them to control signal, which is passed to transport layer. Link layer need not to know the content of data packets.

Packet sending: receiving the demand from transport layer for sending data, link layer mainly provides the following services:

- Negotiating with the equivalent link layer to send data packets, avoiding request sending at the same time.
- Wrapping the data from transport layer with SOF, CRC, and EOF etc.
- Receiving Dword mode data from transport layer.
- Calculating CRC for data from transport layer.
- Sending packets.
- Offer packet flow control according to request of FIFO and feedback from the equivalent link layer.
- Receiving ACK of data packet from the equivalent link layer.
- Reporting to transport layer the exact transfer result and the wrong messages from link layer and physical layer.
- 8b/10b encoding.

Packet receiving: link layer mainly offers following services when getting data packets from physical payer:

Informing of the equivalent link layer the readiness to receive data.

- Receiving coded character from physical layer.
- 8b/10b decoding, Dword data aligning.
- Unwrapping packets, removing SOF, CRC and EOF.
- Calculating CRC of receiving Dwords.
- Offering packets flow control according FIFO request and the feedback from the equivalent link layer.
- Reporting to transport layer and equivalent link layer the right receiving results and wrong messages of link layer and physical layer.

According to request from command layer and acknowledgement from data link layer, transport layer start the transmitting of data packets. Transport layer implements the classical sideband signal in PATA in the way of data packets. Transport layer has no need to know how data packets are sent and received. It only needs to construct the FIS to send and deconstruct the receiving FIS. When requested by the higher layer to construct a FIS, transport layer provides the following services:

- Receiving FIS from link layer.
- Deciding FIS type.
- Distributing FIS content to where type specify.
- To transport layer of host computer, receiving a FIS may lead to a return of another FIS construction to device side.
- Report to top layer whether correctly receiving or not.

Software layer generate request for reading or writing and can access and configure some performance modes of devices. SATA is software completely compatible with PATA, allowing present PATA device drivers to use in SATA devices without any change.

Host interacts with state machine of state control of transport layer through a register interface, which is equivalent to the legacy PATA Host Adapter. Host software access register interface according to the existing standard and follows the standard command protocol.

III. System Design of HPT183, the Bridge Connection Chip for Serial ATA and Parallel ATA

Adapting totally different data transfer mode, Serial ATA and Parallel ATA are unable to connect directly each other, which will cause present 1 billion parallel devices unable to normally use in Serial ATA system. To solve this problem, we need a bridge connector to finish the conversion from serial ATA to parallel ATA. HPT183 is just such a chip to convert serial ATA to parallel ATA.

A. The Apply System of HPT 183

HPT183 can be defined as host bridge connection chip and device bridge connection chip. The Fig 2 shows the application.

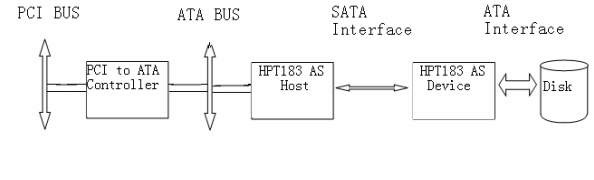

Fig.2 The Application of HPT183

B. The Architecture of the HPT183

The design of HPT183 chip employs partial integration, which firstly define integration scenario, secondly finish entire design, and finally choose MCU module, IP module

from PHY layer and IDE module etc., among of which MCU80C51 and IDE are IP exclusive use and universally use module, developed and built up by ourselves. PHY layer is a hard-core IP provided by Semiconductor Company. The other parts and software will be designed otherwise and connect together to undergo a system test. Partial integration partly makes use of the existing mature IP module, so the workload is relatively light and designing cycle is shorter. The Fig.3 shows the architecture of the HPT183.

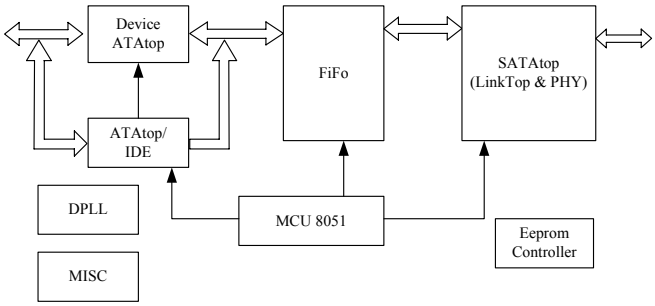

Fig.3 System Structure Diagram of HPT183

MCU 80C51 module is an embedded MCU, which will finish the protocol conversion from transport layer of SATA to command protocol of PATA. When the chip is configured as host, MCU will be used to convert command protocol of ATA to data packet protocol of SATA. When the chip is configured as device, MCU will be used to convert data packet protocol of SATA to interface protocol of ATA.

IDE module is a subsystem of interface controller, connecting ATA/ATAPI peripheral equipment, which mainly control transfer mode and may chose PIO or DMA mode. Besides, this module can also pass MCU to set control command to peripheral equipment, like the reading and clearing of status etc. This module only work on condition that chip is set as device.

DevATA module is a subsystem of interface control, connecting ATA/ATAPI host, which mainly respond to command, sent from the ATA interface host, of manipulating peripheral equipments. This module only work on condition that chip is set as host.

SATAtop module implements the function of the PHY layer and link layer of SATA protocol, including the sending and receiving of serial data, the conversion of serial to parallel and parallel to serial, data synchronizing, encoding and decoding, initiating device and flow control and so on.

FIFO module is realized through a bidirectional and double-end ram and its control circuit. The main task of this module is to buffer the data packet. The bandwidth of SATA does not match the bandwidth of PATA, so bidirectional FIFO will solve the unsynchronous transfer problem and make the transferring continuous and smoothly.

DPLL is an all-digital clock generating module, which will generate the system clock for the chip.

EEprom control module is used only when chip is configured as device. Program codes of 51, which are stored in peripheral equipment, will be downloaded to program RAM module of the chip.

MISC module determine the working mode of the chip, such as Host normal mode, Device normal mode, Host testing mode, Device testing mod, PHY testing mode and RAM BIST testing mode and so on.

C. Verifying System Structure of HPT183

Applica module will emulate the applications that operate on hard disk, reading and writing for instance. Drive module will convert this application to specific register command operation on hard disk to drive PCI Master to generate and respond to corresponding PCI protocol signal. PCI Slaver emulate the slave device on PCI bus, RAM module, storing the data for reading and writing of hard disk, is also equivalent to a slave device on PCI bus. PCI Bus Arbiter module arbitrates the bus occupying of host device on PCI bus. HPT372N is a multifunction UDMA controller from PCI bus to ATA/ATAPI peripheral equipment according to the IDE standard. HPT372N offers two IDE bus controllers, one for connecting two master and slave hard disk, one for connecting two SATA/PATA bridge connection chip (host), which link the device bridge connection chip through SATA bus. The device bridge connection chip is linked to An ATA/ATAPI device through IDE interface. The fig.4 shows the verifying system structure.

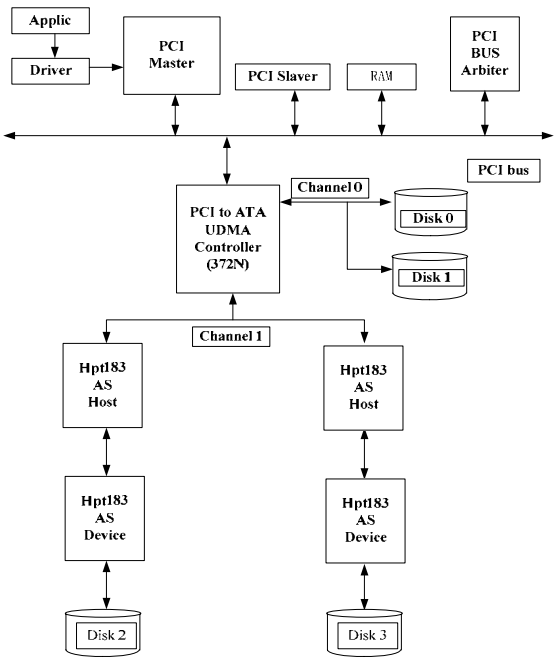

Fig.4 Verifying System Structure of HPT183

IV. TWO WAYS OF RECOVERING DATA FROM HIGH SPEED SERIAL BUS

A. *Clock & Data Recovery (CDR)*

CDR is used to lLL circuit/DLL circuit and take 1:1 sampling of the data on serial ock embedded clock signals on the serial bus at receiving end by Pbus with clock recovered [7]. Figure 1 shows the circuit structure of PPL. It is composed of Phase Detector (PD), Loop Filter (LF), Oscillator (OSC) and a frequency divider style (%M). Many circuits adopt PPL to recover clock data [8-10].

B *Over-sampling Data Recovery*

The technology of Over-sampling Data Recovery doesn't need to recover synchronous high speed clock signals from serial bus. Instead, it takes over-sampling with a high speed sampling signal at the receiving end and then removes redundancy bits of data after over sampling to get actual bit info. Jun-Young PARK puts forward an Over-sampling Data Recovery circuit [11]. The circuit adopts a local low speed clock (1/8 of serial transfer rate) to generate 32 same phase interval clock signals and take 4:1 over-sampling of serial data with the 32 clocks. Over-sampling data is disposed by transmission Detect circuit and data border selective circuit to recover actual data.

During two methods, the method of CDR needs to get a high speed clock signal from serial bus. PPL circuit uses analog circuit. Analog circuit takes up a lot of chip. Phase needs long time to lock [12-15], moreover, with increasing transfer rate, high speed PLL circuit is more and more difficult to implement. However, the method of Over-sampling Data Recovery needs at least 3:1 over-sampling rate so that a mass of redundancy info is generated, which needs a lot of circuit to remove redundancy bits [11].

V. ALL-DIGITAL CLOCK DOUBLING CIRCUIT DESIGN & HIGH SPEED SERIAL DATA RECOVERY CIRCUIT DESIGN

A. *All-digital Clock Doubling Circuit Design*

All-digital standard cell clock doubling circuit uses a net list related with the same specific standard cell library to describe an IP module. For most digital circuits, standard cell gate net list description simplifies the design. The circuit has been used in the PATA/ SATA bridge chip HPT183 which is manufactured on condition of 0.18CMOS.

Figure 5 shows the structure of clock doubling circuit. It is composed of Digital Controlled Oscillator (DCO)，Finite State Machine (FSM)，Counter and either/or circuit. An external reference clock source doubling frequency of 25MHz generates 75MHz system clock of chip. At every rising edge of 25MHz clock, DCO restarts to oscillate. At the beginning, DCO oscillates as fast as possible and counts output frequency of DCO circuit at the next rising edge of 25MHz clock. CNT is frequency-doubling coefficient, which is set as 3 by MCU. If the count is CNT, clock of 75MHz is got and control word of DCO will keep the same. If the count value is more than CNT, the control word of DCO circuit will be increased and the frequency of DCO clock output signal will be decreased.

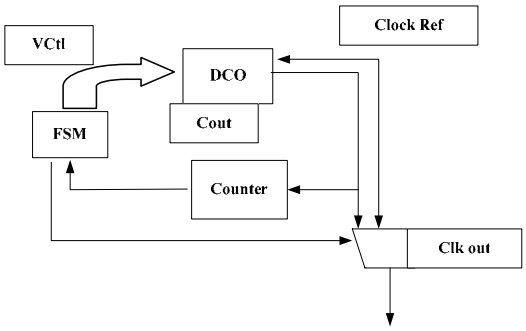

Fig. 5 the Structure of Clock Doubling Circuit

1) The Structure of DCO Circuit

Figure 6 shows the structure of DCO circuit. In every clock rising edge of Clkref clock signal will generate a narrow impulse Restart DCO circuit which is composed of level 5 delay time-varying cells, a fixed delay time cell and a reverse gate.

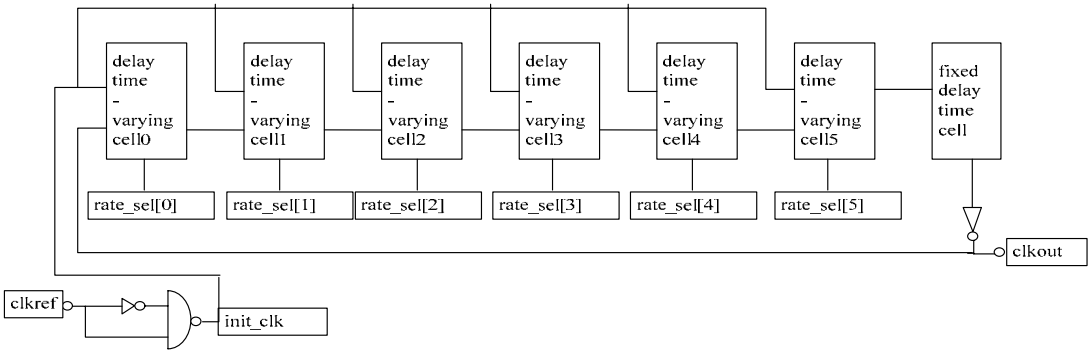

Fig 6. The Structure of DCO Circuit

Figure 7 shows the structure of delay time-varying cell circuit. Because of different digital control word sel[] signals, the path of signals from in to out is different so that time delay is different. The difference of time delay depends on Delay module.

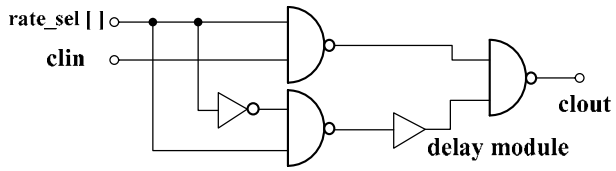

Fig.7 delay time-varying cell circuit

Reverse gate is used to implement Delay Module in the design. Delay time-varying cell 0 uses 2 reverse gates. Delay time-varying cell 1 uses 4 reverse gates. Delay time-varying cell 2 uses 8 reverse gates. Delay time-varying cell 3 uses 16 reverse gates.

Figure 8 shows the connection curve of Digital control word and clock period of DCO circuit output clock. It is a monotone increasing linear function curve. The slope is 400ps/bit. The rage of DCO circuit clock output frequency is from 35MHz to 300MHz.

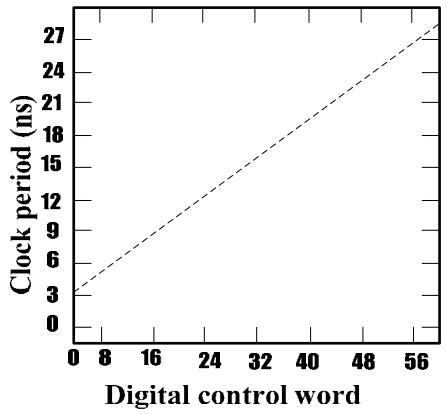

Fig 8. The connection curve of control word and clock period

2) Finite state machine state transition diagram of control circuit.

Figure 9 shows FMS state transition diagram. Sate A is system reset state. En-cnt is output clock counting enable signal. When reset is invalid, state A switches to state B. When state B reads the comparing result of clock counting value and preset value.

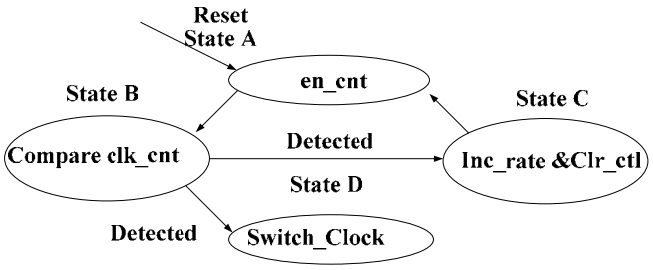

Fig. 9 FMS state transition diagram

If detected is 1, state B switches to state D, or it switches to state C. In state D, clock signal output switches to DCO circuit clock output from 25MHz exterior reference clock. State C won't switch to any other switches. In state D, Inc_rate increases DCO control word and Clr_cnt eliminates clock counting efficiently. State D switches to state A directly.

3) The Result of Simulation

The voltage of All-digital Clock Doubling Circuit is 1.8v. The reference clock frequency is 25MHz. The CNT is 3. Figure 10 shows the circuit control word response diagram of clock doubling frequency locking process. Control word starts at 0 after system reset. When control word keeps up 25 after 2880ns, lock clock is output.

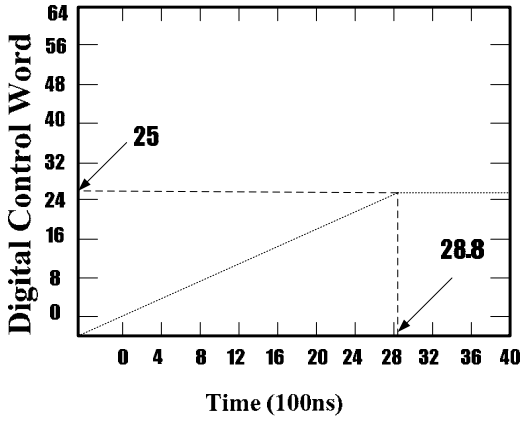

Fig 10. DCO circuit control word response curve

B *High Speed Serial Data Recovery Circuit Design*

1) The structure of high speed serial data recovery circuit.

This is a new high speed serial data recovery circuit. It adopts all-digital standard cell to implement SATA high speed data receiving, synchronization and switching from serial to parallel. Serial ATA interface is a high speed embedded clock serial interface, whose transmission bandwidth is 1.5Gbps. Serial ATA interface adopts 8B/10B encoding. It allows at most 5 bits with serial 0 and 1 when transferring. Figure 11 shows the structure of high speed serial data recovery circuit.

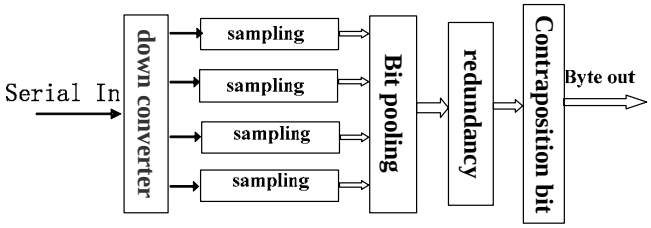

Fig. 11 The structure of high speed serial data recovery circuit.

In the circuit design, the time of recovering data is short. Data will be received as soon as it comes. Synchronous byte data will be got as long as there are synchronizing signals. The same clock is adopted in multi-path sampling data converging circuit and the following signal processing circuit. The clock signal is got from serial input wire level 8 Crossover. Clock

frequency decreases greatly. Moreover, signal frequency will change as serial input signal frequency changes, which can decrease power consumption. When equipment works in the state of sleep mode, namely, when there is no signal sent on serial bus, the clock signal will keep the same level, which can decrease power consumption greatly. The circuit is small and easy to implement.

2) Signal Processing Procedure on Circuit

(1) Down branching circuit

Figure 12 shows the signal graph of down branching circuit. The frequency of high speed serial input signal is decreased to divide into high level route 1, low level route 2, high level route 3 and low level route 4 in circuit. Route 2 and route 4 are reverse.

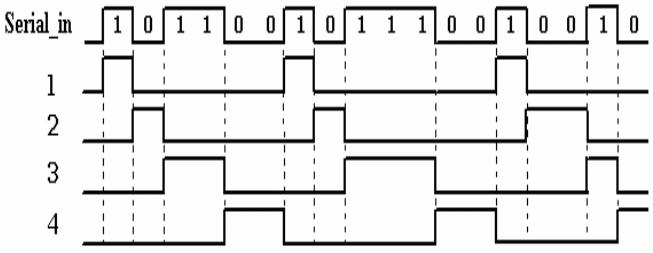

Fig 12. Down branching circuit signal graph

(2) Sampling/Bit count

As figure 11 shown, input signals is delayed half bit pulse width, 666ps for SATA, to get delay1, delay2, delay3 and delay4 signals. SATA adopts 8bit/10bit encoding. The maximum transmission signal bit wide is 5 bit. For SATA, only 5 signals are needed.

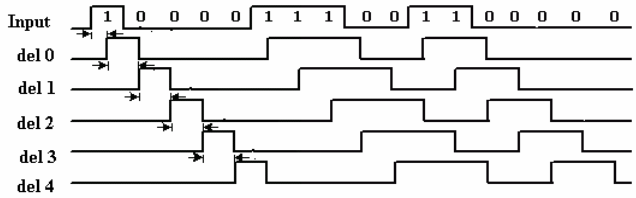

Figure 13 Sampling/Bit count circuit signal graph

In order to avoid parts of apparatus is influenced by craftwork, voltage and temperature when chip works, delay time-varying cell circuit is used. MCU controls the delay time. Figure 12 shows the structure of circuit. Input signals are used as flip-latch clock signals to lock and store time delayed signal delay0, delay1, delay2, delay3 and delay4 signals so that Q0，Q1，Q2，Q3 and Q4 signals can be got. The five signals describe pulse width: 00001 means 1 bit pulse width, 00011 means 2 bit pulse width, 00111 means 3 bit pulse width, 01111 means 4 bit pulse width, and 11111 means 5 bit pulse width.

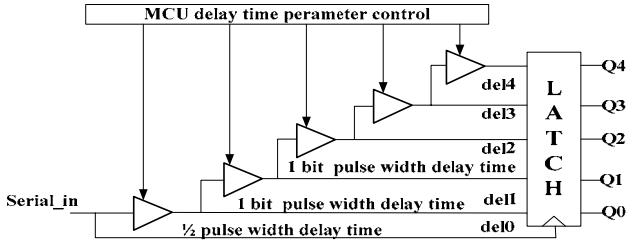

Fig 14 Serial signal sampling circuit

Figure 15 shows pulse width delay time adjustable cell circuit of 1 bit. Sel[2:0] signal, the control word set by MCU, is time delay from control signal din to signal dout. Time will be delayed to arrive or approach to 1 bit pulse width 666ps by controlling Sel[2:0].

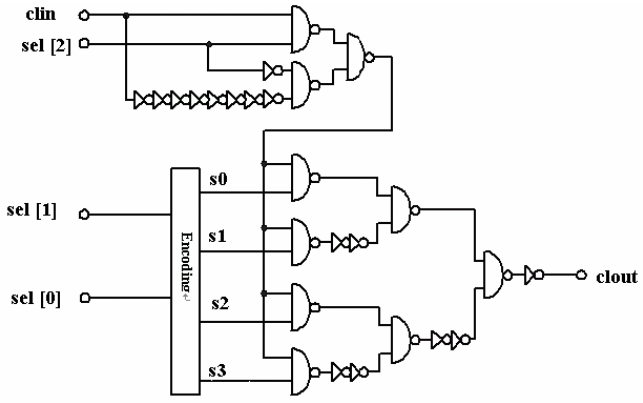

Fig.15. Pulse width delay time-varing cell circuit of 1 bit

(3) Multi-path sampling data converging circuit

In order to decrease the clock frequency of post-treatment circuit, multi-path sampling data converging circuit composes a group of data to output with 2 groups of 4 routes input data. Data processing is as followed.

Four rotes input:

	Rout 1	Rout 2	Rout 3	Rout 4
Group 2	00111	00001	00111	00011
Group 1	00011	00111	00001	01111

A group of bit sequence output:

00011 00111 00001 01111 00111 00001 00111 00011

1 2 3 4 1 2 3 4

(4) Remove info of redundancy bit

According to the info that bit width shows, info of redundancy bit will be removed. The data of Route 1 and Route 3 is the result of high level pulse width count. The data of Route 2 and Route of 4 is the result of low level pulse width count. Data processing is as followed.

Input bit sequence

Rout 1 Rout 2 Rout 3 Rout 4 Rout 1 Rout 2 Rout 3 Rout 4

00011 00111 00001 01111 00111 00001 00111 00011

Input bit sequence after removing redundancy

11 000 1 0000 111 0 111 00

(5) Bit integration and bit aligned

The digits of bit sequence are uncertain after removing redundancy bit. Therefore, data signals with the same bit width will be integrated. Data processing is as followed.

Input：…

1110101001100

10101010

111001110000110100

1011001010

Output：…

00110100101010101110

10110010101110011100

The output data after integrated is bit sequence on the actual transmission wire. In order to get actual byte info, bit should be aligned according to synchronizing info agreed by sending and receiving both sides protocol. In SATA, synchronizing info is ALIGN primitive, and bit sequence is 0011111010 or 1100000101. Data processing is as followed.

Input： …

00110010101100111010

11001110010101100010

10100001111101010010

Output： …

11001010110001000110

00111110101001011001

(6) Clock circuit

The same clock is adopted in both multi-path sampling data converging circuit and the following signal processing circuit. The clock is got from serial input wire level 8 Crossover. Clock frequency decreases greatly, moreover, the signal frequency will change as serial input signal frequency changes, which decrease power consumption. When there is no signal sent on serial bus, the clock signals will keep the same level, which can decrease power consumption greatly.

VI. PERFORMANCE TESTING

HPT183 chip is designed and made at 0.18 um of standard CMOS technology. The testing results of data transfer rate of HPT183 are compared as follows:

Table 2 shows the testing results of date transfer rate of hard disk at different connecting mode. HP372A is an interface chip form PCI to ATA. Like HPT183, Marvell is also a bridge connection chip for PATA/SATA, which can be deployed as a host chip to be connected to HPT372A or can be deployed as device chip to be connected to DISK. This test is carried in the same system with DISK INSPECTION Test of the software WINBENCH 99. In table1, Begin stands for data transfer rate at the beginning; End stands for data transfer rate at the end, Average stands for the average data transfer rage.

TABLE 2
Testing results of data transfer rate of hard disk

System connection type	Begin(KB/s)	End(KB/s)	Average(KB/s)
HPT372A - Marvell(host) -HPT183(device) - disk	35100	34400	13234
HPT272A - disk	35100	34500	13245
HPT372A - Marvell(host) -Marvell(device) - disk	35100	34500	13244

VII. CONCLUSIONS

The differences between parallel ATA protocol and serial protocol are compared in this document. Parallel ATA, adapting source synchronizing technology, has constrain of clock skew and is hard to enhance data transfer rate. Serial ATA protocol, adapting embedded clock technology instead, can increase data transfer rate greatly. Serial ATA employs hierarchical classification protocol module, with totally four layers: physical layer, link layer, transport layer and software layer. Despite the fact that serial ATA is compatible with parallel ATA on software layer, they are completely different in connection mode and unable to use universally. It means that the existing1 billion parallel equipments will not be used directly in serial ATA system properly. A bridge connector, therefore, is needed to finish the conversion of serial ATA to parallel TAT. In this document, we propose a design of this kind of bridge connection chip, which adopt all-digital circuit design and use standard cell to implement instead of PPL or DDL simulation circuit. In contrast to serial data recovery circuit implemented by simulation circuit, the circuit design is more simple, easy to use, smaller and lower consumption. The circuit is applied in the design of HPT183 bridge connection chip for PATA/SATA and manufactured using a 0.18um CMOS process.

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