# The Influence of the Nanometer Technology on Performance of CPL Full Adders

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***Abstract*— In this paper the performance of 8-transistor based Full adder is analyzed, evaluated, and compared with that of three different types of Full Adders based on Complementary Pass Transistor XOR Logic gate. Simulation results using nano-scale SPICE parameters are obtained for the above mentioned FAs. It is shown that the performance of the 8-transistor based Full adder in term of power dissipation is superior to that of the other FAs. Multi-Supply Voltage Technique is used to optimize the outputs of 8-Transistor Full Adder. A new technique based on minimum leakage vector is proposed to reduce the leakage current when the circuit is in its off state.**

***Index Terms*—Full Adder, Minimum Leakage Vector, Multi-Supply Voltage, Nano-Technology, Pass Transistor Logic, XOR logic gate.**

## I. INTRODUCTION

The increasing demand for portable devices and hand held equipments gives the low power design techniques more attention in the literature [1]. The battery which is the source of the power in these mobile systems is the key factor which determines the main characteristics of the mobile systems including the speed, the power dissipation, and the silicon area. In most cases these characteristics are chosen in order to increase the life time of the battery [3]. Therefore, it is highly demanded to propose efficient low power design techniques capable of driving the battery for long time operation [4].

The power dissipation in CMOS circuits can be classified into two types: dynamic and static. In digital systems that use 180nm technology and above, the dynamic power dissipation was the most significant source of power dissipation. However, scaling the technology from 130nm to less than 22nm in the next two decades will increase dramatically the static power dissipation, instead of dynamic power dissipation [1].

It becomes a fact that one of the basic blocks in most digital systems is the Full Adder (FA). In fact FAs form the basic components of digital signal processing, image processing, video processing systems. Moreover FAs are found in digital arithmetic & logic units. Therefore, FAs have been rapidly improved and studied by many researchers in the literature.. Minimizing the number of transistors in the FAs was the main concern to reduce the dynamic and static power dissipation as well as to improve the speed and the performance of the circuits[1][2].

Recently, the size of the CMOS transistor in nanometer Technology is reduced and the number of transistors per unit area is consequently increased. In effect the supply voltage has been reduced to maintain acceptable average dynamic power dissipation per silicon area. However, in order to maintain the high speed operations, some transistor parameters such as the threshold voltage and the thickness dioxide must be scaled down at the same rate as the supply voltage [5]. Consequently, the leakage current power dissipation is increased dramatically with each technology generation. Therefore trade off between different parameters should be made to achieve a given level of power dissipation. In general, the most efficient parameters that reduce the power dissipation are scaling both the supply voltage and the total load capacitance [6].

It is the main objective of this paper to study, analyze and optimize the Nano-scale SPICE parameters of CMOS transistor in most attractive FA circuits. These FAs are based on complementary pass transistor logic gate. These gates they are characterized as low power/high speed components. We show that that the number of transistors and their topology in the design are the most two parameters that affect the power dissipation for next generation Nano-scale CMOS transistor.

The organization of the paper is as follows: Analysis and description of the most recent FA designs published in literature are shown in section II. The 8-Transistor FA is described and discussed in section III. Section IV shows the performance of FA in terms of power dissipation and the delay time. Section V discusses the minimum leakage vector technique. section VI analyze the performance of the different FAs based on Nano-scale SPICE parameters. Simulation results of 4-bit FA (carry ripple adder) are discussed and analyzed in section VII. Section VIII concludes the paper.

## II. BASIC CIRCUITS OF FULL ADDERS

Several Full Adder designs are focused on low power dissipation published in the last decades [7][8][9], one of these designs is the Transmission gate Full Adder (TFA) [7], TFA consists from 16 transistors for pull-up and pull-down logic outputs. In this design, there are two possible short circuit paths to the ground; therefore it consumes dynamic power dissipation, as well as short-circuit power dissipation. Meanwhile, the design is characterized as low power Full Adder that used widely in multimedia and wireless applications.

The second type of Full Adder is called Static Energy-Recovery Full Adder (SERF) [8], it consists from 10 transistors; it has less number of transistors than TFA


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without direct path to the ground. For this reason, the design is better than TFA Full Adder in saving power and reducing delay time, the outputs of this design are degraded at logic low and high which are the main weaknesses of the design.

The last Full Adder studied, analyzed and compared with, is published in [9], it called 14_transistor Full Adder based on CMOS technology, the SUM circuit is implemented by using XNOR-XNOR logic gates, while the CARRY circuit is implemented using PMOS-NMOS transistors [9]. This design is capable to fix the weaknesses appeared in SERF design; it produces better results in threshold loss by inserting inverters between the XOR gate and its output to form an XNOR gate, it seems that this full adder consumes lower power than SERF one. Therefore, it is much better than all other mentioned designs in saving power, while it's not the best one regarding the delay time because of its critical path and the complex topology of its transistors.

After this simple introduction to three efficient Full Adders, its concluded that it is a trend to decrease the number of transistors which implement the Full Adder to achieve several advantages such as: reduce the silicon area, reduce the delay time and reduce the dynamic and static power dissipation [10].

## III. 8-Transistor Full Adder

The XOR gate forms the fundamental building block of the Full Adder; therefore enhancing the performance of the XOR gate is important issue to improve the performance of the Full Adder. One of the basic forms of the Full Adder could be shown from the following two Boolean algebra:

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = C_{in} \bullet (A \oplus B) + AB \quad (2)$$

### A. The Design of XOR Gate

Figure 1 shows an efficient 2_input XNOR logic gate published recently in the literature, it contains from one pMOS transistor to produce logic one while the other two nMOS transistors are used to produce logic 0.

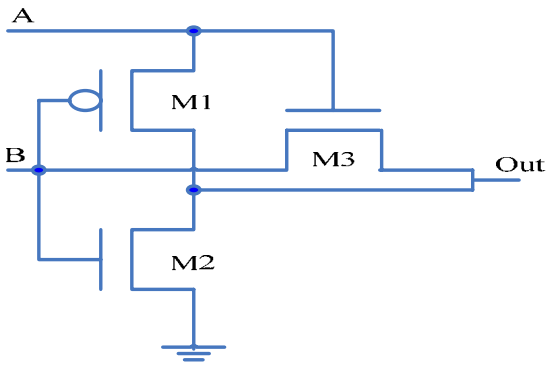


Figure 1: Three Transistors XNOR Gate

The main drawback of this gate that is when both inputs are 0, the output will not exactly 1, this is because when the input B is 0, the gate of M1 will be closed and the current from source will pass through drain within the gate of M1, in this case the output will be weak 1, instead of strong 1, as shown in Table I.

TABLE I.
Truth Table for XNOR Gate in Figure 1.a

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | |
| 0 | 0 | Week 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Even though the drawback of this design is appeared when the Output is at logic 1, but it is more preferable than any other XNOR logic gates, it seems that the total power dissipation and speed operation in this circuit is better than all other XNOR logic gates. Simulation results using HSPICE verified the logic operation of the XNOR logic gate.

The NMOS transistor (M3) in Figure 1 is a key transistor, if its replaced by pMOS transistor, then it will perform XOR logic gate, the new gate has good output in all its combinations, the new XOR gate is shown in Figure 2, while its true table is shown in Table II [10].

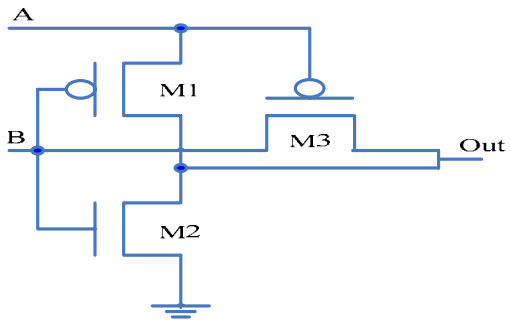


Figure 2.a 3_Transistor XOR Logic Gate

Table II shows the truth table of Figure 2.a with the new pMOS transistor, it seems that the output at logic inputs 0 & 0 yields good outputs as expected, which is the main advantage of the new design.

TABLE II.
Truth Table of 3_transistor XOR Gate

| A | B | OUTPUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Figure 2.b shows simulation results of the XOR logic gate of Figure 2.a, the first and second waveforms represent the inputs A & B, while the last one represents the evaluation of the XOR gate.

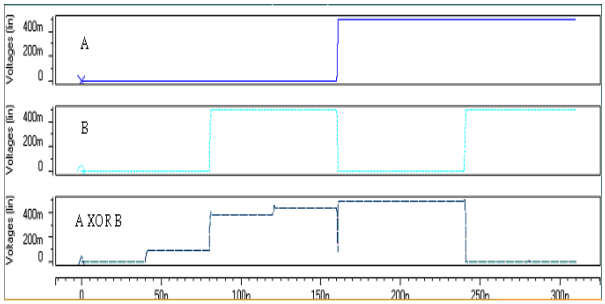


Figure 2.a: Simulation waveforms of the XOR Logic Gate

As shown from equations 1 and 2, the Full Adder could be implemented from SUM circuit which contains from two XOR gates, therefore, applying the 3_transistor XOR gate shown in Figure 2.a, could perform the SUM function by only 6 transistors, while the Carry out could be implemented using only one PMOS transistor and one NMOS transistor, as shown from Figure 3[8].

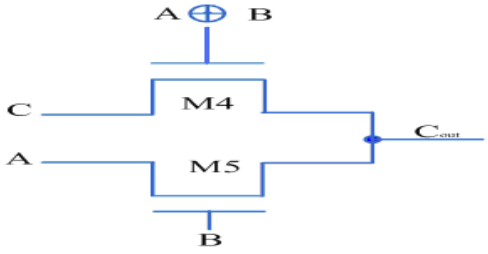


Figure 3: The carry out circuit of new Full Adder design

Figure 4.a shows Full Adder with 6 transistors that perform the SUM circuit, it consists from two XOR gates in series, and the output of ($A \oplus B$) is XORed again with the $C_{in}$ to perform the SUM. The Carry out circuit contains from two nMOS transistor built by CPL logic gate, the logic operation of the Carry out is very simple, it is ANDed the (A XOR B) with $C_{in}$ or it is ANDed the input A with the input B, this simple gate implemented by 2 transistors only to perform the Carry out successfully.

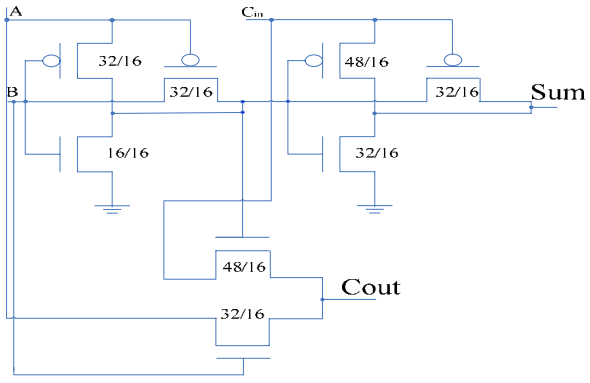


Figure 4. a: The 8-Transistor Full Adder Design[10]

Simulation results of three inputs are shown in Figure 4.b, from these waveforms, it seems that for three input combinations; there are corrected waveforms in the output which verifies the validity of the 8_Transistor Full Adder. The weakness of this Full Adder appears at the outputs when the inputs A is Low, B is High, & C is Low, or when the inputs A is High, B is High & C is Low. This problem could be solved if the size of XOR gate is modified properly as proposed in [10], unfortunately some disadvantages could be appeared when the size is not given correctly.

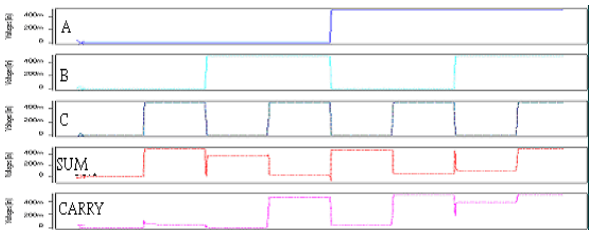


Figure 4. b. Input/Output waveforms of the 8-T Full Adder

### *B. Multi-Supply Voltage Technique*

To solve the degradation at the output, multi-supply voltage technique is applied on this Full Adder to get efficient results at the output. Multi-Supply voltage technique is an efficient technique used recently to reduce the total dynamic and static power dissipation [11], it based on using different levels of supply voltages in the circuit in order to reduce the power dissipation and increase the speed operation. In our case, Multi-Supply Voltage technique is applied in transistors which are suffered from weakness at High or Low at their outputs. In the 8_Transistor Full Adder case, three levels of supply voltages are used and applied in the Full Adder as shown in Figure 4.c, where V1, V2 and V3 are the three levels of supply voltages shown in table III.

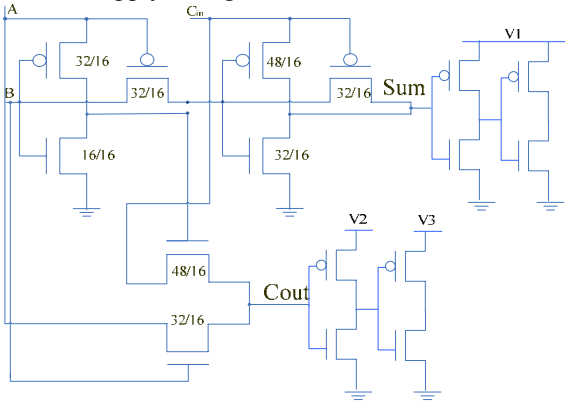


Figure 4. c: Multi Supply Voltage 8-Transisstors Full Adder

TABLE III.
PROPAIRE VALUES OF VOLTAGE SUPPLY

| Output voltage (V) | V1(V) | V2(V) | V3(V) |
|---|---|---|---|
| 0.8 | 0.8 | 0.5 | 0.8 |
| 1 | 1 | 0.6 | 1 |
| 1.2 | 1.2 | 0.8 | 1.2 |
| 1.4 | 1.4 | 1.1 | 1.4 |
| 2 | 2 | 1.8 | 2 |

Applying multi-supply Voltage Technique on the 8_Transistor Full Adder as shown in Figure 4.c will yield correct outputs as shown in Figure 4.d, it seems that the output operates correctly without any degradations.

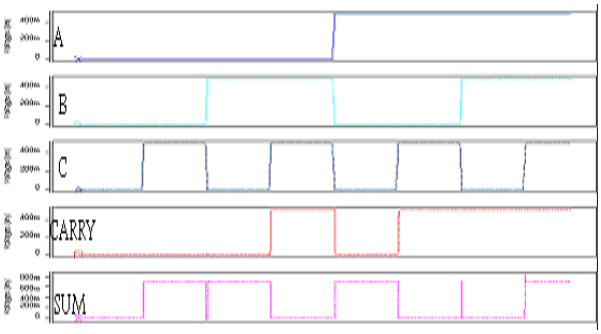


Figure 4. d: Simulation Result Waveforms of the 8-T Full Adder with Inverters

From above table it showed that the V2 must be approximately 60% of V3.

## IV. Simulation Results

In order to evaluate the performance of the 8_Transistor Full Adder, various evaluations and comparison results between this Full Adder with other types of Full Adders shown in Section II are discussed and analyzed, the simulation results are given under the same circumstances of SPICE parameters. The comparatives are given between the dynamic power dissipation with different values of load capacitor, delay time, and leakage power using 16nm technology SPICE Foundries[14].

### *A. Delay Time*

One of the most important parameters in the circuit level is the delay time, the delay time will be increased by decreasing the supply voltage[1], for this purpose, the logic high of three inputs is taken as 0.7V. This value is selected after different tests and simulations using the range between (0.6V to 1.2V). The difference between the delay time of these Full Adders appeared very clear around this value, Table IV shows the delay time of Four Full Adders using different values of load capacitance at their output, it shows clearly that the 8_Transistor Full Adder is fastest than all others, SERF Full adder shows it is so much comparable with the 8_Transistor Full Adder for load capacitance of 10fF and 20fF, but for higher values, the 8_Transistor Full Adder seems to be the fastest. Figure 5.a shows these results very clear.

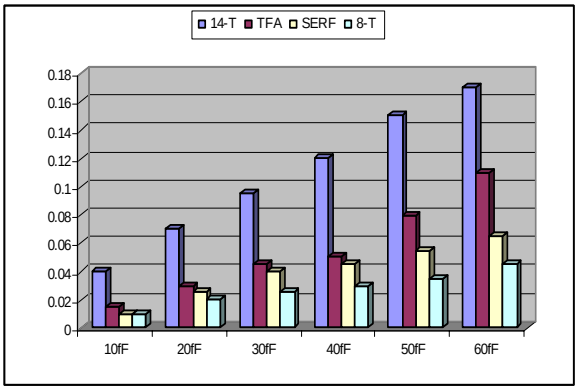


Figure 5.a. The delay time for each Full Adder under different values of load capacitors

The values in Table IV are the delay time of Figure 5.a as a chart to showing the difference between the Four tested Full Adders**.**

TABLE IV.
DELAY TIME IN DIFFERENT VALUE OF LOAD CAPACITOR ($E^{-007}$)

| Delay Time (nSec @ vcc=0.7V) | | | | |
|---|---|---|---|---|
| CL | 14 T | TFA | SERF | 8-Transistor |
| 10fF | 0.040 | 0.015 | 0.010 | 0.010 |
| 20fF | 0.070 | 0.030 | 0.025 | 0.020 |
| 30fF | 0.095 | 0.045 | 0.040 | 0.025 |
| 40fF | 0.120 | 0.050 | 0.045 | 0.030 |
| 50fF | 0.150 | 0.080 | 0.055 | 0.035 |
| 60fF | 0.170 | 0.110 | 0.065 | 0.045 |

### *B. Dynamic Power Dissipation*

Dynamic power dissipation is appeared when the transistor changes it is status from high to low or from low to high, the most efficient parameters of dynamic power dissipation is the supply voltage, for this purpose, Table V shows the dynamic power dissipation for each Full Adder at different values of load capacitor. Simulation results show that the 8_Transistor Full Adder has the lowest dynamic power dissipation; this is because it does not contain direct supply voltage ($V_{CC}$) within its circuit except the two added Inverters (in case they are added). Figure 5.b shows that the TFA Full Adder consumes higher than any other Full Adder, then SERF and 14-T Full Adder in order, while the 8-T Full Adder consumes the lowest power dissipation comparing with all other circuits.

TABLE V.
DYNAMIC POWER DISSIPATION FOR EACH FULL ADDER IN DIFFERENT VALUE OF LOAD CAPACITOR

| Dynamic Power Dissipation (nWatt) with different load capacitor @ $V_{cc}$=0.7V | | | | |
|---|---|---|---|---|
| $C_L$ (fF) | 8-T With (2 INV) | SERF | 14-T | TFA |
| 10 | 40 | 140 | 60 | 150 |
| 20 | 43 | 142 | 66 | 155 |
| 30 | 45 | 152 | 67 | 163 |
| 40 | 46 | 155 | 71 | 169 |
| 50 | 48 | 158 | 75 | 170 |

Figure 5.b shows the same results of dynamic power dissipation for different values of load capacitors.

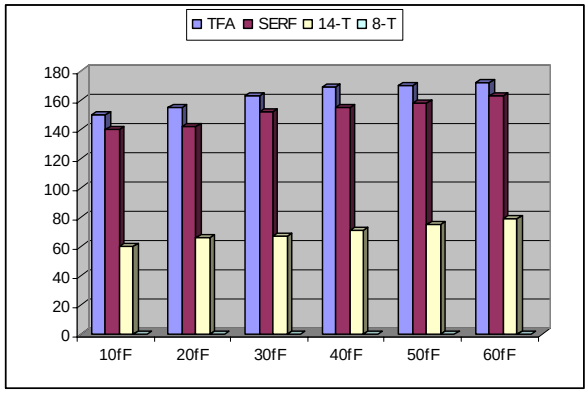


Figure 5.b: Dynamic power dissipation in deferent value of load capacitor

## V. MINIMUM LEAKAGE VECTOR TECHNIQUE

By scaling the SPICE parameters from micro-technology to nano-technology, the value of leakage current is increased, this is because some of the SPICE parameters are changed, such as the length of the gate, the thickness dioxide and threshold voltage. Therefore, it became a demand to look for new techniques that reduce the leakage power dissipation in nano-scale parameters. Leakage current which appears when the transistor is in *off* state plays semantic role in the nano-scale SPICE parameters, therefore, it is important issue to look for new techniques that reduce the leakage current without influence the delay time or the power dissipation. One of these techniques is the Minimum Leakage Vector [12] [13], the main concept of this technique is to select the proper input vector so that the major transistors of the circuit remain in ON state when the circuit is in *Off* state. In our case, for one single Full Adder, it is easy to test the proper input combination of three inputs manually; the second step of this technique is to calculate the leakage current of each transistor independently. For 16nm SPICE parameters, the subthreshold leakage current for NMOS is 28.8e-011A and the subthreshold leakage current for PMOS is $\left|7.37\text{e-}011\text{A}\right|$, therefore, the leakage power dissipation could be calculated from the following equation:

$$P_{Leakage} = I_{Leakage} \times V_{CC} \quad (3)$$

Table VI summarizes the proposed technique when it applied in SERF Full Adder, it declares the status of transistors for each input vector, where logic 1 represents (*ON* state), and Logic 0 represents (*OFF* state), the same approach could be applied for other Full Adders, where m(number)-p is the number of specific pMOS transistor and m(number)-n is the number of specific nMOS transistor in the circuit. From table VI, it shown that, for eight input vectors there are 24 NMOS transistors are *OFF* while there are 16 PMOS transistors are *ON*. The leakage current appeared in case of NMOS transistors is 24 × 28.8e-011 from NMOS transistors and 16 × $\left|7.37\text{e-}011\right|$ from PMOS transistors, therefore the total leakage current for both PMOS and NMOS transistors in this design is 124.832e-011W, of leakage power dissipation.

TABLE VI.
TRANSISTOR'S STATE IN DIFFERENT INPUT VALUE

| | *A* | *B* | *C* | M1-p | m2-p | m3-n | m4-n | m5-p | m6-p | m7-n | m8-n | m9-n | m10-p |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input Combinations** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| **TOTAL ON** | | | | 4 | 4 | 4 | 4 | 4 | 6 | 2 | 4 | 2 | 6 |
| **TOTAL OFF** | | | | 4 | 4 | 4 | 4 | 4 | 2 | 6 | 4 | 6 | 2 |

In case of equation (3) is applied, the leakage power dissipation will be 124.832e-011× 0.9 =1.12.nW. The same procedure could be implemented for all other Full Adders. Table VII shows the states of transistor: how many transistors are *ON* and how many transistors are *OFF* for the Four Full Adders given in this paper. It seems that the 8_Transistor Full Adder dissipates lowest leakage power dissipation. This result is expected because the number of transistors in the 8_Transistor Full Adder is fewer than any other Full Adders discussed in this paper.

TABLE VII
NUMBER OF ON/OFF TRANSISTOR IN EACH FULL ADDER

| | TFA | | 14-T | | SERF | | 8-Transistor | |
|---|---|---|---|---|---|---|---|---|
| | PMOS | NMOS | PMOS | NMOS | PMOS | NMOS | PMOS | NMOS |
| **ON State** | 24 | 24 | 21 | 21 | 24 | 16 | 16 | 16 |
| **OFF State** | 40 | 40 | 21 | 21 | 16 | 24 | 16 | 16 |
| **Leakage current(Am)** | 2.95E-11 | 1.15E-11 | 1.55E-11 | 6.08E-11 | 1.18E-11 | 6.91E-11 | 1.18E-11 | 4.61E-11 |
| **Total leakage current(Am)** | 410e-011 | | 154.866-011 | | 124.832e-011 | | 122.052e-011 | |

Figure 5.c shows the difference between the leakage current power dissipation for each type of Full Adders under different values of Voltage Supply

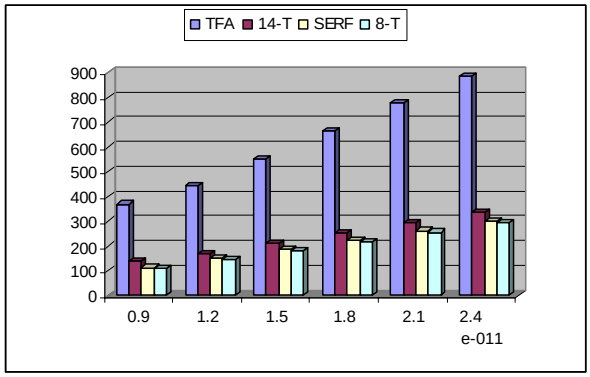


Figure 5.c. leakage current power dissipation for each FA in different value of power supply

## VI. The Characteristics of Full Adders in Nano Technology Scale.

In order to show the behavioral of the 8_Transistor Full Adder using various SPICE parameters in Nano-scale, we compared it with the other three Full Adders, simulation results show that the 8_Transistor Full Adder has lowest delay time for various load capacitor in 45nm and 90nm, this gives the validity of this Full Adder to be used in high speed applications, Table VIII.A shows these results in more details.

Table VIII.B shows the power dissipation at the output of each Full Adder using different values of load capacitor under two SPICE parameters which are 45nm and 90nm. It shows that the power dissipation in the 8_Transistor case is lowest power dissipation comparing with all other Full Adders.

TABLE VIII.A
DELAY TIME IN NSEC AT DIFFERENT NANO-METER SCALE

| | **45 nm technology** | | | | **90 nm technology** | | | |
|---|---|---|---|---|---|---|---|---|
| $C_L$(*f*F) | SERF | TFA | 14-T | 8-T | SERF | TFA | 14-T | 8-T |
| 10 | 0.009e-7 | 0.010e-7 | 0.029e-7 | 0.007e-7 | 0.006e-7 | 0.008e-7 | 0.020e-7 | 0.004e-7 |
| 20 | 0.019e-7 | 0.019e-7 | 0.045e-7 | 0.014e-7 | 0.010e-7 | 0.010e-7 | 0.035e-7 | .0090e-7 |
| 30 | 0.027e-7 | 0.030e-7 | 0.069e-7 | 0.019e-7 | 0.018e-7 | 0.018e-7 | 0.052e-7 | 0.012e-7 |
| 40 | 0.036e-7 | 0.045e-7 | 0.085e-7 | 0.026e-7 | 0.026e-7 | 0.026e-7 | 0.067e-7 | 0.020e-7 |
| 50 | 0.045e-7 | 0.064e-7 | 0.10e-7 | 0.029e-7 | 0.033e-7 | 0.033e-7 | 0.089e-7 | 0.024e-7 |

TABLE VIII.B.
POWER DISSIPATION μWATT AT DIFFERENT NANO-METER SCALE

| $C_L$(*f*F) | 14 T | TFA | SERF | 8-T. |
|---|---|---|---|---|
| 10 | 5.5 | 1.11 | 1.03 | 0.98 |
| 20 | 8 | 2.01 | 1.96 | 1.88 |
| 30 | 10 | 2.62 | 2.65 | 2.5 |
| 40 | 12.5 | 3.31 | 3.29 | 3.23 |
| 50 | 14 | 4.68 | 4.35 | 4.15 |

## VII. Simulation Results for 4_bit Full Adder (Carry Ripple Adder)

In order to test the performance of the modified 8_Transistor Full Adder, it was compared with the other Four FAs discussed in this paper, using 4_bit Ripple Carry Adder as shown in Figure 6. The tested circuit is simulated under 16nm SPICE Parameters.

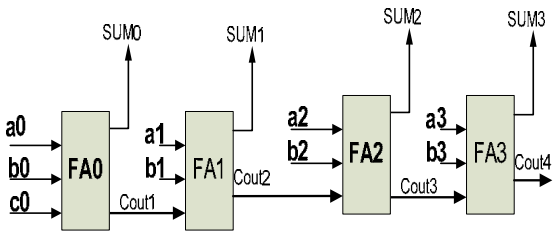


Figure 6: 4_bit Ripple Carry Adder

### *A. Delay Time*

Table VIII.C shows the delay time for each Full Adder under different values of load capacitor using two types nano-scale SPICE paramters, from the simulation results, it shows that the 8_Transistor Full adder, SERF, and TFA have somewhat equally delay time, but the 14_Transistor Full Adder has much longer delay time than other three types.

TABLE VIII.C. DELAY TIME FOR EACH FA IN DIFFERENT LOAD CAPACITOR VALUE (E-007)

| | 45 nm technology(nSec) | | | | 90 nm technology(nSec) | | | |
|---|---|---|---|---|---|---|---|---|
| $C_L$(*f*F) | SERF | TFA | 14-T | 8-T | SERF | TFA | 14-T | 8-T |
| 10 | 220 | 238 | 88 | 68 | 262 | 281 | 119 | 98 |
| 20 | 229 | 242 | 93 | 76 | 266 | 286 | 124 | 103 |
| 30 | 235 | 245 | 95 | 85 | 272 | 289 | 128 | 110 |
| 40 | 238 | 252 | 99 | 84 | 275 | 292 | 132 | 119 |
| 50 | 244 | 257 | 102 | 97 | 279 | 297 | 136 | 122 |

Figure 7 shows the delay time of the 4-bit Full Adders at various load capacitors. It indicates that the 8-T Full Adder is faster than all other types of Full Adders

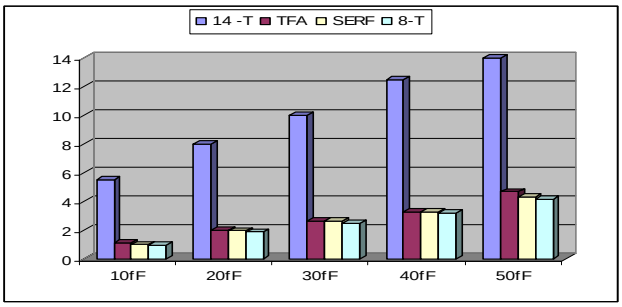


Figure 7: delay time for each FA in different load capacitor value.

### *VII. b: Dynamic Power Dissipation*

The same simulations are repeated to test the power dissipation for each type of Full Adder using 4_bit Ripple Carry Adder, Table VIII.D shows that the power dissipation for each Full Adder at different value of load capacitor, it shows that the 8_Transistor Full Adder has the lowest power dissipation, the second design is 14_Transistor and the worst design is SERF Full Adder.

TABLE VIII.D: DYNAMIC POWER DISSIPATION FOR EACH FA IN DIFFERENT VALUE OF LOAD CAPACITOR(@NW)

| Power Dissipation with different values of Load Capacitor (**V***cc*=0.7V) | | | | |
|---|---|---|---|---|
| CL(*f*F) | 8_T | SERF | 14_T | TFA |
| 10 | 0 | 720n | 240n | 650n |
| 20 | 0 | 742n | 270n | 684n |
| 30 | 0 | 788n | 300n | 710u |
| 40 | 0 | 801n | 310n | 723n |
| 50 | 0 | 830n | 320n | 740n |

Figure 8 shows the dynamic power dissipation using the information of table VIII.D for each full adder with different value of load capacitor.

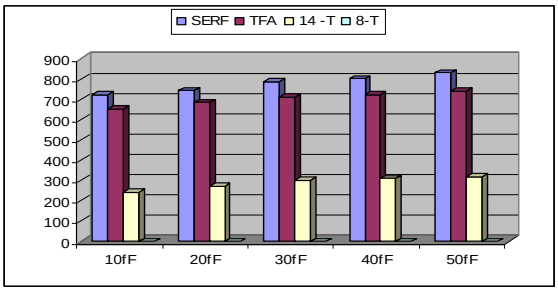


Figure 8: Power dissipation in different load capacitor value

### *VII.c: Leakage Power:*

Table VIII.E shows the leakage power dissipation for each Full Adders (carry ripple) using different values of supply voltage ($V_{CC}$), as its indicated the lowest leakage power is appeared in case of 8_T Full Adder, the second adder is the SERF adder and worst adder in leakage is the TFA Full Adder.

TABLE VIII.E.
LEAKAGE POWER FOR EACH FA IN DIFFERENT VALUE OF LOAD CAPACITOR (NA)

| $V_{CC}$ | TA | 14-T | SERF | 8-T. |
|---|---|---|---|---|
| 2.4 | 3540 | 1336 | 1196 | 1171.2 |
| 2.1 | 3116 | 1170 | 1048 | 1024 |
| 1.8 | 2656 | 1000 | 898.6 | 878.4 |
| 1.5 | 2210 | 835.5 | 748.2 | 732 |
| 1.2 | 1768 | 868 | 597.8 | 583 |
| 1 | 1476 | 557 | 449.1 | 439 |

Finally, all simulation results shown in this paper are given from [14][15], these predictive SPICE parameters, declare that the next generation of power dissipation will be the leakage current power dissipation, for this reason, the number of transistors and their topology in the design are playing the main role of the power dissipation in the design.

## VIII. CONCLUSIONS

Three different Full Adder circuits based on Complementary Pass Transistor Logic has been compared with newest 8_Transistor Full Adder in this paper. The 8_Transistor is known as the lowest number of transistors Full Adder. The comparison results between these transistors in power dissipation, delay time, and leakage power, are measured, it seems the 8-transistor Full Adder has superiority in reducing the power dissipation of dynamic and leakage current as well as the delay time. In order to verify these results, three various predictive SPICE parameters are tested in this paper (90nm, 45nm and 16nm). Multi supply voltage technique is used to get exact levels of high and low at it is output. The 8-transistor Full Adder seems to be the most usable Full Adder for next decade's applications.

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