A 105 dB DR, -101 dB THD+N Sigma-Delta Audio D/A Converter with A Noise-shaping Dynamic Element Matching Technique

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Abstract—A Sigma-Delta audio digital-to-analog (D/A) converter with a noise-shaping dynamic element matching (NSDEM) technique is presented. The proposed NSDEM technique has the advantage of less computation and also can be implemented with all-digital circuits easily. The converter is fabricated in a 0.35 μm CMOS process, occupies 2.85 mm², and achieves 105 dB dynamic range - 101 dB total harmonic distortion plus noise.

Index Terms—NSDEM, multi-bit switched capacitor DAC, Sigma-Delta, tree structure, RISC

I. INTRODUCTION

Sigma-delta analog-to-digital (A/D) and digital-to-analog (D/A) converters are widely used in high precision, low bandwidth application, and they have the characteristics of more digital circuits and less analog circuits [1], [2]. At present, along with the rapid development of manufacturing technology for integrate circuit, sigma-delta A/D and D/A converters tend toward high speed for conversion. They are used in many domains, such as in consumption, industrial control, communication and so on [3], [4].

To improve the stability for sigma-delta modulator used in converters and the SNR (Signal Noise Ratio) for converters, multi-bit Sigma-delta modulator has recently been applied to implement high performance Sigma-Delta A/D and D/A converters [5]. The use of multi-bit quantization in a multi-bit Sigma-Delta modulator can reduce the power of the quantization noise which must be shaped out of signal band. Therefore, a multi-bit Sigma-Delta modulator can achieve the same SNR as a 1-bit Sigma-Delta modulator with a lower modulator order and a reduced oversampling ratio [6]. But when using multi-bit Sigma-Delta modulator, the converters need to contain multi-bit DAC. The multi-bit DAC is made of switched capacitor, and the output of quantizer within Sigma-Delta modulator controls switched capacitor to open or close

![Figure 1. The frame of the proposed audio Sigma-Delta D/A converter.](image-url)
through encoding. Because of the limitation of manufacturing technology, it’s too hard to make every capacitor in the same size accurately. In this way, the converters will produce nonlinear error and big amplitude of harmonic in signal band, which will reduce the SNR of entire converters [7], [8].

To avoid these problems, the technique of dynamic element matching (DEM) has been developed. The DEM block with the technique of DEM is used in conjunction with the quantizer of Sigma-Delta modulator and DAC [9]. The main classes of the DEM blocks include individual-level averaging [10], vector feedback [11], data-weighted averaging [12], butterfly shuffler [13] and tree structure [14].

In this paper, we present a new audio D/A converter which uses a 3rd-order 5-bit Sigma-Delta modulator and a tree-structured noise-shaping DEM block. The DEM block encodes the output of quantizer, and then the output can switch the switched capacitors in multi-bit switched capacitor DAC randomly, introducing random noise to smooth the nonlinear distortion. But the introduced random noise will raise the level of background noise in signal band [15]. Considering that, the technique of noise-shaping is used in this block to push the noise out of signal band, expecting the improvement of the converters’ performance [16].

In this paper, the frame of the proposed Sigma-Delta audio D/A converter is shown in Fig. 1. The D/A converter includes audio serial port block, de-emphasis/interpolation block, volume control block, multi-bit Sigma-Delta modulator block, switched capacitor DAC block, analog low pass filter block, clock manager block, serial control port block, digital soft power block, and zero detector/mute block. The data formats of the input signal include I2S, LJ, RJ16~RJ32, and DSD. The amplitude of the volume can range from 24dB to -103.5dB stepped by 0.5 dB, and the converter also has the function of auto-mute. It supports the interface standard of I2C and SPI, so the converter can be controlled by an external processor. It can detect the sampling frequency of the input signal automatically.

### A. Clock manager block

The frame of the clock manager block is shown in Fig. 2.

![Figure 2. The frame of the clock manager block.](image)

<table>
<thead>
<tr>
<th>The estimation frequency of “external MCLK”</th>
<th>The ratio between “external MCLK” and “LRCK”</th>
</tr>
</thead>
<tbody>
<tr>
<td>The estimation frequency of “external MCLK”</td>
<td>128</td>
</tr>
<tr>
<td>256×50KHz</td>
<td>1 (48KHz)</td>
</tr>
<tr>
<td>256×50KHz</td>
<td>4 (192KHz)</td>
</tr>
<tr>
<td>384×50KHz</td>
<td>3 (96KHz)</td>
</tr>
<tr>
<td>384×50KHz</td>
<td>6 (192KHz)</td>
</tr>
<tr>
<td>256×100KHz</td>
<td>4 (96KHz)</td>
</tr>
<tr>
<td>256×100KHz</td>
<td>8 (192KHz)</td>
</tr>
</tbody>
</table>

This paper is organized as following. Section II discusses the overall architecture of the proposed audio D/A converter and the architecture of main blocks in this audio D/A converter. Section III discusses the proposed DEM technique in detail. Section IV presents the measured results of the proposed audio D/A converter, and section V is a conclusion.
ensure the internal MCLK synchronize the external MCLK. Also, through controlling the bypass block, the internal clock can equal the external clock directly. The function of the state machine is shown in Table I.

In the clock manager block, the external master clock is divided, synchronized and delayed to produce the internal master clock automatically; making sure the ratio between the frequency of internal master clock and 48 KHz is 128.

B. Digital signal processing block

To simplify circuit of the converter, we design a digital signal processing block which is a Reduced Instruction Set Computer (RISC). The implementation circuit of the RISC is shown in Fig. 3. When the clock manager block determines the sampling frequency of the input data, the 32-bit RISC implements the function of volume control and interpolation filtering using most simplified instruction set. The schematic diagram is shown in Fig. 4.

![Figure 3. The implementation circuit of the RISC.](image)

![Figure 4. The flow of signal processing in different sampling rates of input data.](image)

The RISC has two kinds of instruction: math instruction and assignment instruction. The math instruction includes SADD (shift and add), SSUB (shift and subtract), SPR1 (shift register R1 and assign value), and SPR2 (shift register R2 and assign value). The assignment instruction includes LD (load), ST (set) and NOPMOE (null). The RISC executes a math instruction and an assign instruction in every clock cycle.

C. Switched capacitor DAC block and DEM block

The switched capacitor DAC block shown in Fig. 1 is made of switched capacitor array. It is a 4-bit 16-level DAC, whose configuration is shown in Fig. 5. Because every capacitor (shown as c1~c16 in Fig. 5) couldn’t be made in the same size accurately, it will reduce the digital-to-analog converted precision [17]. The proposed converter uses a 4-layer tree-structured noise-shaping DEM block to eliminate the noise which is produced by switched capacitor mismatching. The introduction of this DEM block is presented in section III in detail.

D. Sigma-Delta modulator block

In the proposed D/A converter, the structure model of multi-bit Sigma-Delta modulator is shown in Fig. 6. It is
a 3rd-order 5-bit 16-level Sigma-Delta modulator. The signal transfer function (STF) of Sigma-Delta modulator is:

\[
\text{STF}(z) = \frac{a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3}}{1 + b_0 z^{-1} + b_1 z^{-2} + b_2 z^{-3}}
\]

The noise transfer function (NTF) of Sigma-Delta modulator is:

\[
\text{NTF}(z) = \frac{c z^{-1} - 2 c z^{-2} + 3 c z^{-3}}{1 + 2 b_0 z^{-1} + b_1 z^{-2}}
\]

In the structure model, \( a = 0.9596 \), \( b = 0.4096 \), \( c = 0.0738 \), \( f = 2^{(-12)} \). When the input signal of the Sigma-Delta modulator is 1000 Hz, the SNR of the output signal versus the amplitude of the input is shown as Fig. 7. The result of simulation shows that the SNR of the Sigma-Delta modulator is 125 dB in signal band.

For the proposed sigma-delta D/A converter, every capacitor, in the switched capacitor array which structures the 4-bit DAC, can’t be made in the same size because of the limitation of manufacturing technology. Due to element mismatching, nonlinear error will be introduced to this system, reducing its performance greatly [19].

Based on the above depiction, a NSDEM block with the technique of NSDEM is designed in the proposed D/A converter. This NSDEM block is 17-level, tree-structured, shown in Fig. 9, the input of which is 5-bit 16-level digital signal, and the output is 16 switching signals. The output of this block is to control the switched capacitor array of multi-bit DAC. The nodes of Fig. 9 are called switching blocks, each switching block is labeled \( S_{k,r} \), where \( k \) and \( r \) represent the switching block’s layer number and position within the layer, respectively. Each switching block \( S_{k,r} \) has a single \((k+1)\) bits input \( y_{k,r} \), and two \( k \) bits outputs: \( y_{k-1,2r-1} \) and \( y_{k-1,2r} \). Every switching block must satisfy

\[
y_{k-1,2r-1}(n) + y_{k-1,2r}(n) = y_{k,r}(n),
\]

\[0 \leq y_{k,r}(n) \leq 2^k\]  \hspace{1cm} (1)

The switching sequence \( s_{k,r} \) is defined as the difference between the two outputs of the \( S_{k,r} \)

\[
s_{k,r} = y_{k-1,2r-1} - y_{k-1,2r} \]  \hspace{1cm} (2)

From (1) and (2), the input/output relationships of switching block \( S_{k,r} \) are

\[
y_{k-1,2r-1}(n) = \frac{1}{2}(y_{k,r}(n) + s_{k,r}(n)),
\]

\[
y_{k-1,2r}(n) = \frac{1}{2}(y_{k,r}(n) - s_{k,r}(n)) \]  \hspace{1cm} (3)

The structure model of \( S_{k,r} \) is shown in Fig. 10.

If all switching sequences \( s_{k,r} \) are non-correlative and have the same frequency characteristic, the multi-bit DAC will also have the same frequency characteristic. So
the switching sequence \( S_{k,r} \) not only satisfies (2), but also has the frequency characteristic of noise-shaping.

\[
S_{k,r} = \begin{cases} 
0 & y_{k,r} = 2i \\
\pm 1 & y_{k,r} = 2i - 1
\end{cases} \quad i = 1, 2, 3 \ldots \quad (4)
\]

So \( S_{k,r} \) represents the sequence which is made up of 0, +1, -1, as (4). A zero-input 2nd-order sigma-delta modulator can produce the same sequence.

In this paper, \( o_{k,r} \) represents the least significant digit (LSB) of \( y_{k,r} \), so \( |s_{k,r}| = o_{k,r} \), and we define \( q_{k,r} = \begin{cases} 
0 & s_{k,r} > 0 \\
1 & s_{k,r} < 0
\end{cases} \). In this way, \( o_{k,r} \) denotes the amplitude of \( s_{k,r} \), and \( q_{k,r} \) denotes the sign of \( s_{k,r} \). So

\[
s_{k,r} = \begin{cases} 
0 & o_{k,r} = 0 \\
-1 & o_{k,r} = 1 \quad q_{k,r} = 0 \\
1 & o_{k,r} = 1 \quad q_{k,r} = 1
\end{cases} \quad (5)
\]

The 2nd-order sigma-delta modulator is shown in Fig. 11.

![Figure 11](image1.jpg)

**Figure 11.** The structure model of switching sequence generator.

Fig. 11 is a zero-input 2nd-order sigma-delta modulator, which is made up of two integrators (1, 2), a quantizer (3) and a multiplier (4). It implements the mathematic function of (5) and produces the switching sequence \( S_{k,r} \).

![Figure 12](image2.jpg)

**Figure 12.** The PSD of sigma-delta modulator’s output.

The PSD of the output of the multi-bit DAC without NSDEM block.

![Figure 13](image3.jpg)

**Figure 13.** The PSD of the output of the multi-bit DAC with NSDEM block.
To the different quantizer which quantizes different number of bit, the system produces different number of layer in the tree-structured error correcting block and different number of $S_{k,r}$ in the system. But the ratiocinative method of producing the random sequence which has the characteristic of noise-shaping is the same as above, the rest may be deduced by analog.

Figure 15. The SNR of multi-bit DAC under different error correcting method and different mismatch ratio.

In this way, the switched capacitor of multi-bit DAC will be controlled to open or close randomly, and thereby random noise is introduced to smooth the nonlinear error caused by element mismatching [20]. Because the switching sequence generator of the error correcting block contains noise-shaping that can push the noise out of the signal band, the SNR of system is improved effectively.

Table II. The area comparison of simplified algorithm and non-simplified algorithm

<table>
<thead>
<tr>
<th>DEM block area</th>
<th>The structure of non-simplified NSDEM algorithm</th>
<th>The structure of simplified NSDEM algorithm</th>
</tr>
</thead>
<tbody>
<tr>
<td>5935</td>
<td>1310</td>
<td></td>
</tr>
</tbody>
</table>

A. The simplified algorithm of 2nd-order NSDEM

In every switching block of the DEM block, if a zero-input 2nd-order sigma-delta modulator is used as a switching sequence generator, the switching block will occupy more hardware area when the hardware of the system is realized from the design. So the hardware configuration of the switching sequence generator must be simplified [14].

![Graph](image)

Figure 17. THD+N versus frequency without NSDEM block.

$y_{k,r}(n)$ is defined as the input of switching block at the time $n$, the $k$ and $r$ of every signal’s suffix represent the switching block’s layer number and position within the layer, respectively. A function is defined as follows:

$$o_{k,r}(n) = \begin{cases} 0 & \text{LSB}(y_{k,r}(n)) = 0 \\ 1 & \text{LSB}(y_{k,r}(n)) = 1 \end{cases}$$

Figure 18. DR versus frequency with NSDEM block.

The symbol of the above function, $\text{LSB}(y_{k,r}(n))$, represents the least significant digit of $y_{k,r}(n)$.

So the zero-input 2nd-order sigma-delta modulator can be implemented through the simplified algorithm in the following:

1. A 3-state accumulator will substitute for the integrator $I_i$ in switching sequence generator. The state machine that implements an accumulator restricted to the following three states: $\{-1, 0, 1\}$.

$y_{k,r}(n)$ will be controlled to open or close randomly, and thereby random noise is introduced to smooth the nonlinear error caused by element mismatching [20].

![Graph](image)

Figure 19. THD+N versus frequency without NSDEM block.

$\begin{align*}
I_i(n-1) + 1 & \quad o_{i,r}(n-1) = 1 \\
I_i(n-1) - 1 & \quad o_{i,r}(n-1) = 0
\end{align*}$

$\begin{align*}
I_i(n-1) & \quad \bar{o}_{i,r}(n-1) = 1 \\
\bar{I}_i(n-1) & \quad \bar{o}_{i,r}(n-1) = 0
\end{align*}$
Some variables based on the value of $I_1(n)$ are defined as follows:

$$MAG_1(n) = |I_1(n)|$$  \hspace{1cm} (8)

$$SGN_1(n) = \text{sign}(I_1(n)) = \begin{cases} 1 & I_1(n) > 0 \\ 0 & I_1(n) < 0 \\ 0 & I_1(n) = 0 \end{cases}$$  \hspace{1cm} (9)

(2) An M-state accumulator will substitute for the integrator $I_1$ in switching sequence generator. The state machine that implements a saturating accumulator restricted to the $M$ integers in the set \{-\frac{M - 1}{2}, ..., \frac{M - 1}{2}\}.

$$I_1(n) = \begin{cases} \text{min}(I_1(n-1) + 1, N_{\text{max}}) & MAG_1(n-1) = 0 \\ \text{max}(I_1(n-1) - 1, N_{\text{max}}) & MAG_1(n-1) = 1 \end{cases}$$  \hspace{1cm} (10)

$$N_{\text{max}} = \frac{M - 1}{2}, \quad N_{\text{min}} = -(M - 1)$$

Some variables based on the value of $I_2(n)$ are defined as follows:

$$MAG_2(n) > 0' = \begin{cases} 1 & |I_2(n)| > 0 \\ 0 & |I_2(n)| = 0 \end{cases}$$  \hspace{1cm} (11)

$$SGN_2 = \text{sign}(I_2(n)) = \begin{cases} 1 & I_2(n) > 0 \\ 0 & I_2(n) < 0 \\ 0 & I_2(n) = 0 \end{cases}$$  \hspace{1cm} (12)

(3) So

$$q_{k,1}(n) = \begin{cases} SGN_1(n) & MAG_1(n) = 1 \\ 0 & MAG_1(n) = 0 \end{cases}$$  \hspace{1cm} (13)

$$s_{k,1}(n) = \begin{cases} 0 & q_{k,1}(n) = 0 \\ 1 & q_{k,1}(n) = 1 \end{cases}$$  \hspace{1cm} (14)

$$y_{k+1,2r-1}(n) = \frac{(y_{k,r}(n) + s_{k,r}(n))}{2}$$  \hspace{1cm} (15)

$$y_{k+1,2r}(n) = \frac{(y_{k,r}(n) - s_{k,r}(n))}{2}$$  \hspace{1cm} (16)

B. Simulation results

We use MATLAB to simulate the NSDEM block based on the simplified algorithm of NSDEM, the Sigma-Delta modulator shown as Fig. 6 and the multi-bit DAC shown as Fig. 5. Under the condition that the capacitor mismatch ratio of switched capacitor DAC is 0.5%, the -60dB 1000Hz sine wave is as input signal to the proposed Sigma-Delta modulator, simulation is made and the figures below compare the output of the multi-bit DAC with NSDEM block with the output of the one without NSDEM block. Fig. 12 illustrates the PSD (Power Spectral Density) of sigma-delta modulator’s output. Fig. 13 illustrates the PSD of the output of the multi-bit DAC without NSDEM block when capacitor mismatch ratio is 0.5%. Fig. 14 illustrates PSD of the output of the multi-bit DAC with NSDEM block in the same condition as Fig. 13. From the figures, we will find out that the noise level in Fig. 14 is lower than that in Fig. 13, and is almost the same as that in Fig. 12.

The result of simulation shows that it eliminates basically the nonlinear error caused by element mismatch when the NSDEM block based on the simplified 2nd-order NSDEM method is added to the system.

Fig. 15 is the simulation result when the capacitor mismatch ratio varies from 0% to 1%, under the condition that the proposed D/A converter is without NSDEM block, with non-simplified NSDEM block or with simplified NSDEM block respectively. From the figure, we will find out that the simplified NSDEM block’s error correcting effect is close to that of the non-simplified NSDEM block.

Using the standard cell library of Co. Chartered to synthesize the simplified algorithm of 2nd-order NSDEM and the non-simplified algorithm of 2nd-order NSDEM respectively, the area occupied by DEM block is shown in table II. (The DEM area is the standard cell area.)

From Fig. 15 and table II, we find out that the NSDEM block using simplified NSDEM structure could be implemented at a low hardware cost to correct the nonlinear error, and a good correcting effect is obtained.

IV. MEASURED RESULTS OF THE PROPOSED D/A CONVERTER

We designed a Sigma-Delta audio D/A converter with the NSDEM block using simplified NSDEM technique in 0.35 µm CMOS process. A test circuit is designed in this converter, through serial communicating interface, we can write command to the converter, make it include the NSDEM block or not. When we use the NSDEM block, the THD+N versus frequency is shown as Fig. 16, the DR versus frequency is shown as Fig. 18. When we don’t use the NSDEM block, the THD+N versus frequency is shown as Fig. 17, the DR versus frequency is shown as
Fig. 19. We find that the THD+N shown in Fig. 16 is below -90 dB in signal band, better than the one in Fig. 17, and the DR shown in Fig. 18 is above 103 dB in signal band, it is 104.5 dB when the frequency is 1 KHz, these are both better than the one in Fig. 19.

V. CONCLUSION

This paper reports the proposed Sigma-Delta audio D/A converter employing a tree-structured NSDEM block to achieve a high performance for D/A converting. Using the presented simplified NSDEM technique, the converter can use less space and calculation to implement a high performance audio D/A converter. Fig. 20 shows the micrograph of the converter.

REFERENCES


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