# A Charge-Sensing-Capable Source Driver for TFT Array Testing in System-on-Panel Displays

Chen-Wei Lin and Jiun-Lang Huang
Graduate Institute of Electronics Engineering
Department of Electrical Engineering
National Taiwan University, Taipei 106, Taiwan
Email: jlhuang@cc.ee.ntu.edu.tw

***Abstract*— Inside a modern flat-panel display, the TFT array acts as the analog memory that stores the image information. To ensure high overall yield, it is crucial to thoroughly test the TFT array before it enters the assembly line. However, TFT array testing gets complicated in system-on-panel displays because the peripheral circuits integrated on the same substrate as the array limit the access to the array's inputs and outputs. This paper presents a built-in source driver design to facilitate TFT array testing for system-on-panel displays. In addition to writing data to the TFT array pixels, the proposed source driver is capable of executing the charge-sensing test and serial read-out of the charge-sensing results—both help reduce the required test equipment performance and complexity. The proposed source driver has been designed in LTPS technology. Circuit simulation results are shown to validate its performance.**

***Index Terms*— TFT-LCD, TFT array testing, source driver, design-for-test, charge-sensing**

## I. Introduction

Flat-panel displays have become the market mainstream because they are much lighter and thinner than the traditional CRT (cathode ray tube) displays. In general, flat panel displays have a layered structure. For example, a liquid crystal display (LCD) (Figure 1) is comprised of the light source, polarizers, circuit plate, liquid crystal solution, and color filters. Among them, the circuit plate is responsible for receiving and storing the image information.

### A. TFT array testing

Figure 2 shows the simplified block diagram of a typical LCD circuit plate. It consists of the TFT (thin-film-transistor) array, the timing controller (T-CON), and the source and gate drivers. T-CON serves two purposes. First, it translates the received image data to a high-speed serial stream, which is the input to the source drivers. Second, it provides the timing and control signals to the source and gate drivers. The TFT array (called array hereafter for convenience) is basically a two-dimensional pixel cell array. Each pixel cell in general consists of a storage capacitor and a TFT switch. Each time, the gate drivers activate one row of the TFT array by setting the corresponding gate line voltage high; this turns on the pixel switches (see Figure 2 where one pixel is shown) so that the source drivers can write data to the storage capacitors in the selected row.

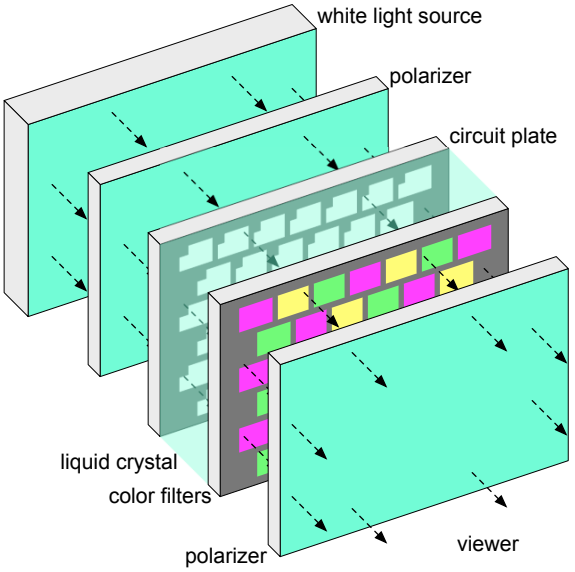


Figure 1. The TFT-LCD structure.

Array testing characterizes the electrical performance of the two-dimensional pixel array. Its most important goal is to identify and report the nature and location of the defects. (Common TFT array defects include opened or shorted wires [1], [2] and defective pixels [3], [4].) Comprehensive array testing is crucial in yield management and quality control since it is the first opportunity to evaluate the electrical performance of a display and the last reliable opportunity to perform repair on defective pixels and gate/data lines. A defective array that enters the assembly line is a waste of not only the assembly cost but also the other defect-free components.

The most commonly used electrical tests for the TFT

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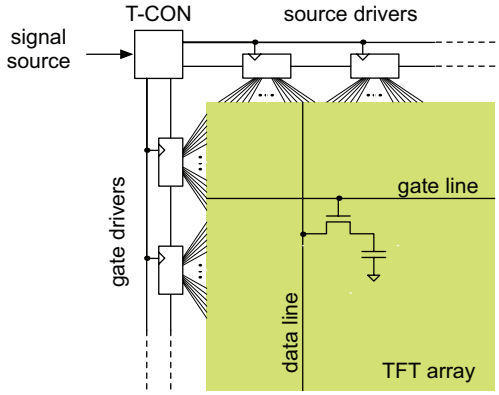


Figure 2. The circuit plate structure.

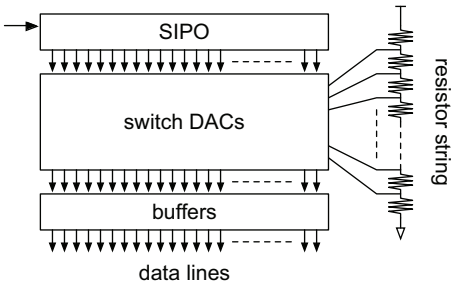


Figure 3. The source driver.

array include the voltage imaging scheme, the electron beam scheme [5], and the electrical testing scheme. Although the voltage imaging and electron beam schemes are able to inspect all the TFT devices on entire substrate at once, only a few kinds of faults can be detected. Besides, both schemes are limited by the high instrument stability requirement and the long working time. Electrical testing schemes, on the other hand, can perform at-speed testing of the array and evaluate more TFT parameters. Among them, charge sensing is a manufacturing proven approach—it characterizes the array devices as well as locates many types of opened and shorted wires defects. The limitation is that it requires access to all data and gate lines.

Several design-for-test (DfT) techniques have been reported to facilitate electrical testing. In [6], a number of lines are probed as a group and connected "head to tail" in series to form a transmission line. Measuring the resistance of the transmission lines will reveal wire defects. In [7], multiplexers realized with a-Si (amorphous silicon) TFT's are integrated on the glass so as to reduce the required probe count.

Conventionally, the array is fabricated using the low-temperature poly-Si (LTPS) or a-Si process on glass while the other peripheral and control circuits are fabricated using the popular CMOS technology. Assembly of these components is expensive and error prone. To lower the assembly cost and reduce the display form factor, the trend is to integrate the peripheral circuits and the TFT array on the same substrate (usually glass). Recently, system-on-panel displays with built-in drivers and even the control and timing circuits have been reported [8], [9], [10], [11]. While these highly integrated systems have reduced form factors and enhanced robustness, they pose new challenges to array testing. For example, direct access to the gate and source lines is no longer guaranteed.

### B. Contributions

In this paper, we propose to utilize the built-in source drivers to facilitate TFT array charge-sensing testing. To reach this goal, a new source driver design is developed. In addition to writing offset-compensated data to the pixel cells, the proposed source driver is capable of performing charge-sensing test as well as serial read-out of the test results. Both the charge-sensing and serial voltage read-out schemes reuse the analog buffers in the source drivers to reduce the area overhead. Moreover, the charge-sensing scheme is able to compensate for the opamp offset voltage due to the $V_t$ variations commonly seen in LTPS and a-Si process. Using the proposed source driver design, the external ATE (automatic test equipment) only needs two analog channels (one to supply the DC reference and the other to sense the serial read-out results) instead of one analog channel for each data line.

The proposed source driver has been designed with LTPS technology and circuit simulation results are shown to validate its performance. The main limitation is the induced area and performance overhead which may be unacceptable for very fine pitch and high refresh rate displays.

### C. Paper organization

This paper is organized as follows. In Section II, we will briefly review the offset compensated buffer and the charge-sensing test. The proposed source driver design, the charge-sensing test procedure, and the serial read-out scheme are illustrated in Section III. Finally, circuit simulation results are given in Section IV and we conclude this paper in Section V.

## II. Preliminaries

In this section, we will briefly review the source driver, the offset-compensated buffer, and the charge-sensing test.

### A. The source driver

Figure 3 illustrates the block diagram of the source driver. Each source driver consists of a switch digital-to-analog converter (DAC) and an analog buffer. The inputs to the driver DACs are from the serial-in-parallel-out (SIPO) blocks; the outputs from the DACs are properly buffered to drive the data lines. In the proposed source driver, the analog buffer is modified to attain the charge-sensing and serial read-out capabilities.

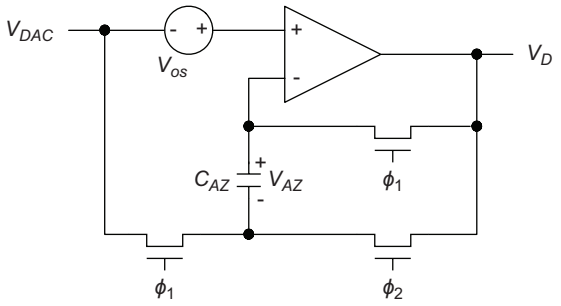


Figure 4. An offset compensated buffer.

### B. The offset-compensated analog buffer

Most TFT arrays are fabricated using the LTPS or a-Si technology. Compared to the mainstream CMOS technology, LTPS and a-Si TFT devices suffer low mobility and $V_t$ variations [12], [13], [14], [15]. In particular, LTPS process is prone to spatial $V_t$ variations while a-Si process is prone to temporal $V_t$ variations.

To compensate for the opamp offset voltage caused by $V_t$ variations, [15] proposed an offset-compensated analog buffer design which is shown in Figure 4. The buffer has two operation phases. In the auto-zero phase, $\phi_1$ is high and $\phi_2$ is low. This way, the offset voltage $V_{OS}$ is stored in the auto-zero capacitor $C_{AZ}$. In the functional phase, $\phi_1$ is low and $\phi_2$ is high. The buffer output $V_D$ will be the same as the buffer input $V_{DAC}$.

### C. The TFT array charge-sensing test

Charge sensing is a common capacitor testing technique [7], [16], [17]. A typical charge-sensing circuit is shown in Figure 5. The charge-sensing procedure consists of three steps: write, hold, and read.

In the write step, SW2 connects the data line to the external test voltage source $V_{test}$ and the pixel's TFT switch is turned on by bringing $V_{scan}$ to high. This way, $V_{test}$ is written to the pixel capacitor $C_{pix}$. At this time, the charge-sensing output $V_{out}$ is initialized by shorting the opamp's negative input and output terminals using SW1. In the hold step, $V_{scan}$ is brought to low to disconnect the pixel capacitor from the data line. If the pixel is leaky, the pixel voltage will gradually goes down. Finally, in the read step, SW2 connects the data line to the charge detecting circuit. Let $Q$ be the charge stored in the pixel at this time. A voltage drop $\Delta V = Q/C_{int}$ will be observed at $V_{out}$.

In the ideal case, the charge stored in $C_{pix}$ is $Q = V_{test} \cdot C_{pix}$ and we have $\Delta V = V_{test} \cdot C_{pix}/C_{int}$. In practice, the pixel is leaky and some of the charge will be lost during the hold period. Let the leakage current be $I_{leak}$. The voltage drop becomes

$$\Delta V = \frac{V_{test} \cdot C_{pix} - I_{leak} \cdot T_{hold}}{C_{INT}} \qquad (1)$$

where $T_{hold}$ is the length of the hold duration. Thus, one can monitor the degree of leakage from $\Delta V$.

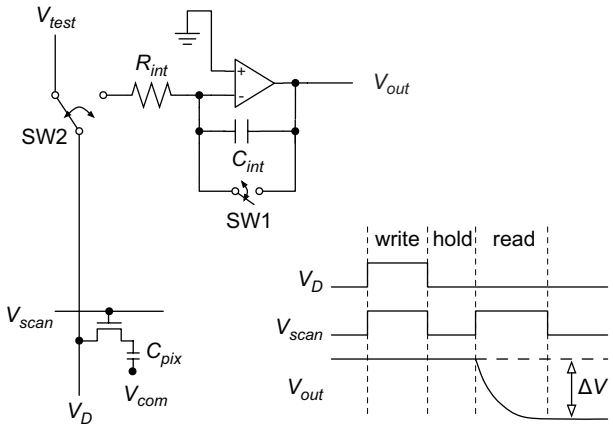


Figure 5. A simplified charge sensing circuit and its timing diagram.

In addition to monitoring pixel leakage, the charge-sensing test also helps identify opened/shorted wires. For example, if the data line of a column is broken between row $n$ and $n+1$, no voltage drop will be observed for pixels below row $n$ at that column.

## III. The Proposed Charge-Sensing-Capable Source Driver

In the proposed source driver, the analog buffer is utilized to facilitate charge-sensing test and serial read-out of test results. In this section, the CS-buffer design will be depicted first. Then, the charge-sensing and serial read-out procedures will be illustrated.

### A. The proposed source driver architecture

The proposed source driver architecture is depicted in Figure 6. In this figure, each "CS-buffer" block represents a charge-sensing-capable analog buffer, called CS-buffer in the following discussion. In additional to the functional input from the DAC and the functional output to write the data line, the following I/O's and circuitry are added to each CS-buffer:

$T$. $T$ is the control signal bus; it is shared among all the CS-buffers.

$V_{test}$. $V_{test}$ is an analog reference signal shared among all the CS-buffers. Via this port, the external tester supplies the reference voltage $V_{ref}$ to each CS-buffer.

$M$. When performing serial voltage read-out, the CS-buffers are divided into two groups that are configured differently. The $mask$ signal is used to differentiate between these two groups. A D-type flip-flop (DFF) is added to each CS-buffer to store its own copy of $mask$ value. The DFFs are connected as a shift register and the desired $mask$ values are delivered to each CS-buffer via the shift operation.

$V_{out}$. The $V_{out}$ port is the analog read-out port where the charge sensing results can be measured by external ATE. To speed up the read-out process, one may utilize multiple read-out ports.

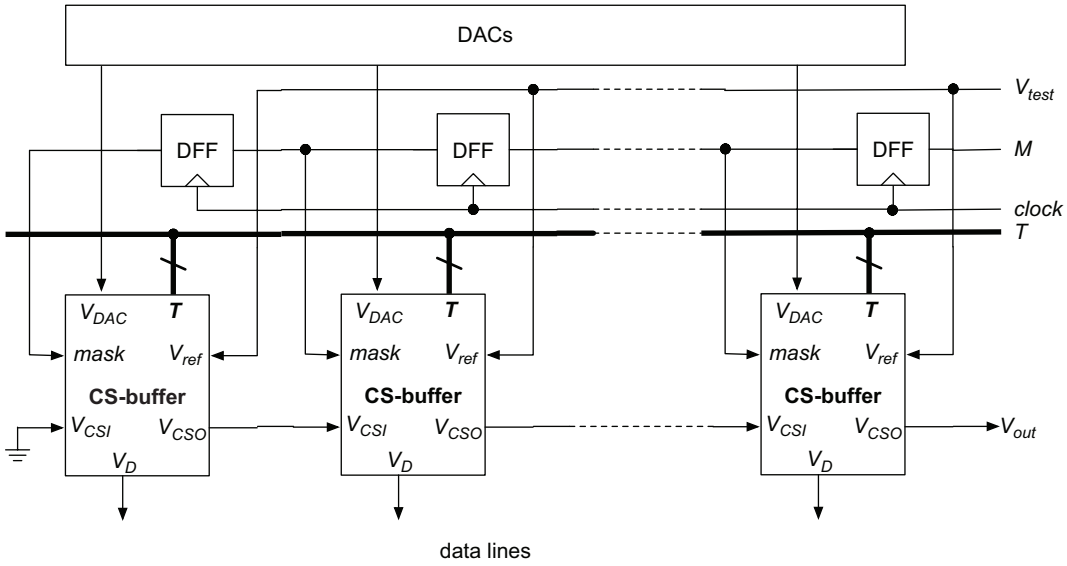


Figure 6. The proposed source driver architecture.

$V_{CSI}$/$V_{CSO}$. The CS-buffers are concatenated by connecting the $V_{CSO}$ port of each CS-buffer to the $V_{CSI}$ port of the CS-buffer at its right-hand side. $V_{CSO}$ of the rightmost CS-buffer is then connected to the array's $V_{out}$ port.

***Control circuitry***. Not shown in the figure, the digital control circuitry inside each CS-buffer produces the proper configuration signals according to the shared $T$ and its own $mask$ signals.

The proposed source driver architecture realizes three operation modes: the functional mode, the charge-sensing mode, and the serial read-out mode. In the functional mode, the CS-buffers act the same as the offset compensated buffer in Figure 4. In the charge-sensing mode, the CS-buffers perform charge-to-voltage conversion. Finally, the serial read-out mode supports serial readout of the charge-sensing results.

The proposed charge-sensing-capable buffer is shown in Figure 7. Compared to the offset compensated buffer in Figure 4 [15], five more switches are added. Among the switches, $\phi_1$ to $\phi_6$ facilitate the functional mode and charge-sensing mode operations; the $\phi_7$ switch, on the other hand, is activated only during the serial read-out mode.

### *B. The functional mode operations*

Like the offset-compensated buffer in Figure 4, there are two configurations in the functional mode: the auto-zero (AZ) and the write-pixel (WP) configurations. The AZ configuration is shown in Figure 8. (For convenience, only the on-switches are shown.) In this configuration, the opamp offset $V_{OS}$ is stored in the auto-zero capacitor $C_{AZ}$. The WP configuration is shown in Figure 9. Since the opamp offset voltage has been stored in $C_{AZ}$, the buffer output $V_D$ will be the same as the buffer's input, $V_{DAC}$.

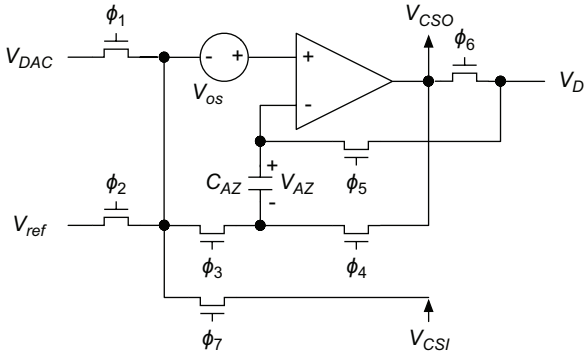


Figure 7. The charge-sensing-capable buffer design.

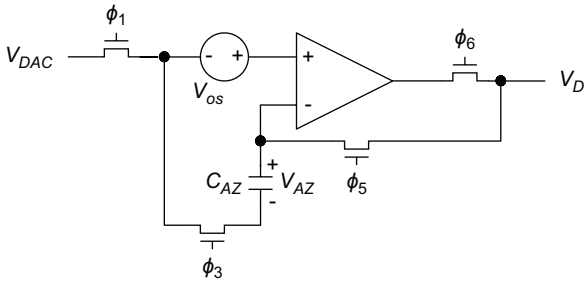


Figure 8. The auto-zero (AZ) configuration.

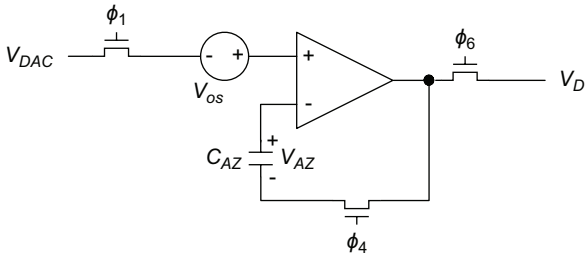


Figure 9. The write-pixel (WP) configuration.

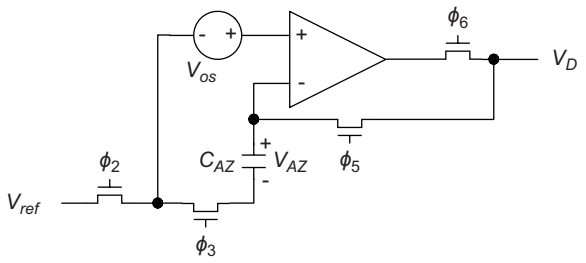


Figure 10. The write data line (WDL) configuration.

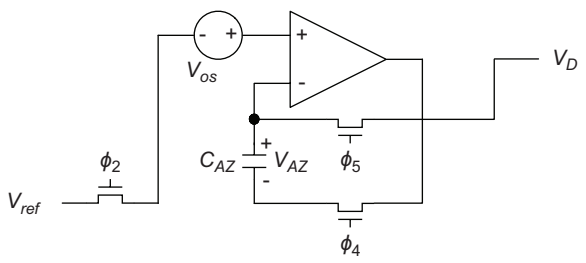


Figure 11. The charge-to-voltage (CTV) configuration.

### C. The charge-sensing mode operations

There are three charge-sensing specific configurations: charge-sensing-write-pixel (CWP), write-data-line (WDL), and charge-to-voltage (CTV). A complete charge sensing session involves four configurations in the following order:

$$\text{AZ} \rightarrow \text{CWP} \rightarrow \text{WDL} \rightarrow \text{CTV}$$

Note that a pre-defined hold period may be inserted between the CWP and WDL configurations to accentuate the pixel leakage effect.

***Charge-sensing-write-pixel (CWP) configuration***. This configuration is the same as the WP configuration except that the CS-buffer input is from $V_{ref}$ rather than $V_{DAC}$, i.e., $\phi_2$ is on and $\phi_1$ is off. The reason is to gain better control over the test voltage.

***Write-data-line (WDL) configuration***. This configuration is intended to pre-charge the data line to a proper voltage level so that the charge stored in the data line does not affect the measurement results. It should be noticed that the pixel TFT switches must be turned off in this configuration so that the pixel voltages remain intact. The write-data-line configuration is shown in Figure 10. Let the test voltage be $V_{ref} = V_{base}$. The data line will be written with $V_{base} + V_{OS}$ and the opamp offset voltage is stored in $C_{AZ}$.

***Charge-to-voltage (CTV) configuration***. In this configuration, the stored pixel charge is converted to voltage. The CTV configuration is shown in Figure 11 where the same $V_{base}$ as in WDL is applied to $V_{ref}$. Since in this configuration, the voltage at the negative input of the opamp remains at $V_{base} + V_{OS}$ which is the same as the data line voltage, the charge stored in the data line has no effect on the measurement results. Let the pixel voltage at the time of the charge-to-voltage operation be $V_{pix}$. The charge-sensing result is:

$$V_{opamp} = V_{base}\left(1 + \frac{C_{pix}}{C_{AZ}}\right) - (V_{pix} - V_{OS}) \cdot \frac{C_{pix}}{C_{AZ}} \quad (2)$$

where $V_{opamp}$ is the voltage at the opamp's output terminal. Define $R$ as the ratio of the pixel capacitance to the auto-zero capacitance, i.e., $R = C_{pix}/C_{AZ}$. (2) can be further simplified as the following.

$$V_{opamp} = (1 + R) \cdot V_{base} - R \cdot (V_{pix} - V_{OS}) \quad (3)$$

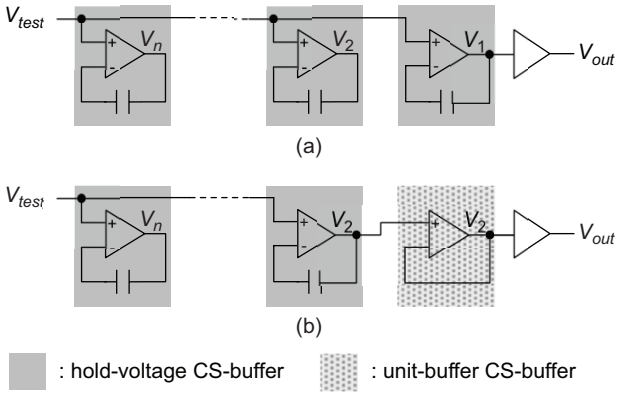


Figure 12. The serial voltage read-out scheme.

In (3), there are two unknowns: $R$ and $V_{OS}$. A calibration procedure (described later) is applied to derive or cancel out these two terms. Note that one can add a DC offset to $V_D$ by adjusting $V_{base}$.

### D. The serial read-out mode operations

After the pixel charge has been converted to DC voltage, the test architecture enters the serial read-out mode to transfer the voltages to the $V_{out}$ port one by one.

The basic idea of the serial read-out operation is depicted in Figure 12, where each shaded block corresponds to one CS-buffer. First, after the charge-to-voltage operation, all CS-buffers are configured to hold the test results at their output terminals, as shown in Figure 12a. At this time, the first CS-buffer's output voltage $V_1$ can be directly read out from the $V_{out}$ port. Then, to read out $V_2$, we configure the first CS-buffer as a unit buffer and let its input be from the $V_{CSI}$ terminal (Figure 12b). This way, $V_2$ is made available at the $V_{out}$ port for measurement. Note that offset compensation must be performed to cancel out the opamp offset voltage. Similarly, to read out $V_3$, we configure the first and second CS-buffers as unit buffers. To summarize, to transfer a CS-buffer's charge sensing result to $V_{out}$, all the CS-buffers between $V_{out}$ and itself are configured as unit buffers.

From Figure 12, one can see that not all the CS-buffers are in the same configurations—some are configured as unit buffers while the others are in a charge-sensing like configuration. (In the functional or charge-sensing mode, all CS-buffers are in the same configuration.) The $mask$

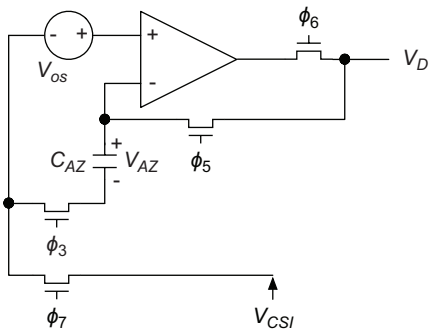


Figure 13. The read-out-auto-zero (RAZ) configuration.

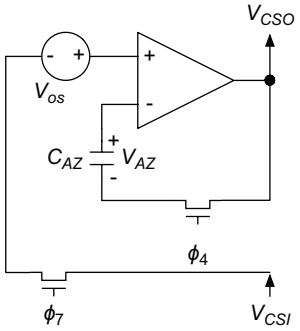


Figure 14. The unit-buffer (UB) configuration.

signal is used to differentiate between these two groups of CS-buffers. As shown in Figure 6, each CS-buffer has a DFF to store its own $mask$ value, and the DFFs form a shift register. During the functional and charge-sensing modes, the $mask$ signal is set to zero for all CS-buffers. In the serial read-out mode, $M$ is set to one. This way, a march sequence of 1 will go through the shift register to realize the serial read-out scheme in Figure 12.

Three configurations are needed to realize the serial read-out operation: hold-voltage (HV), read-out-auto-zero (RAZ), and unit-buffer (UB).

***Hold-voltage (HV) configuration***. This configuration is the same as the CTV configuration in Figure 11 except that $\phi_5$ is turned off to disconnect the opamp output terminal from the data line. This way, further leakage in the pixel will not affect the measurement results.

***Read-out-auto-zero (RAZ) configuration***. As shown in Figure 13, the RAZ configuration is similar to the auto-zero operation except that the input to the opamp's positive terminal is from the $V_{CSO}$ output of the previous CS-buffer.

***Unit-buffer (UB) configuration***. This configuration is shown in Figure 14. If read-out-auto-zero is performed in advance, $C_{AZ}$ will store the opamp's offset voltage $V_{OS}$. Then, the CS-buffer's $V_{CSO}$ output will be the same as its $V_{CSI}$ input.

### *E. The charge-sensing test flow*

The complete charge sensing test flow consists of three charge-sensing sessions. The two additional charge-sensing sessions are needed to derive $R$ and for opamp offset cancellation. The flow is depicted in Figure 15 in which each grey block represents a complete charge-sensing test session, with or without the hold duration.

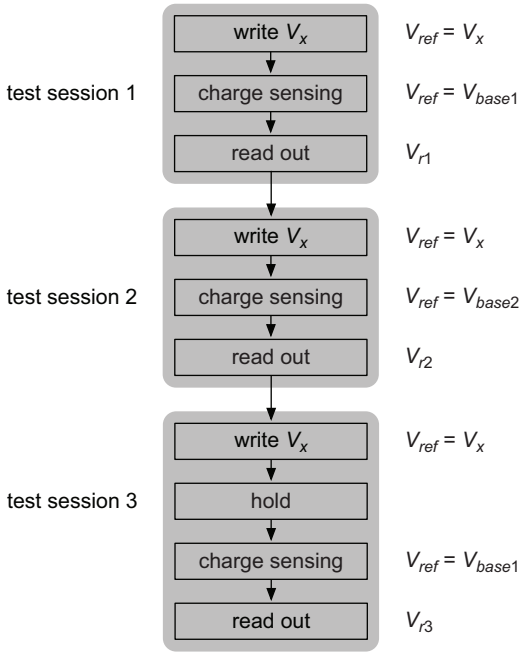


Figure 15. The charge-sensing test flow.

Let $V_x$ be the test voltage to be written to the pixels. In the first test session, charge sensing is performed using $V_{base1}$ as the base voltage, i.e., $V_{ref} = V_{base1}$, and the read-out voltage of the pixel of interest is $V_{r1}$. In the second test session, charge sensing is performed using $V_{base2}$ as the base voltage, and the readout voltage is $V_{r2}$. The third test session is similar to the first one except that a hold period is inserted between "write $V_x$" and "charge sensing." The read-out voltage is $V_{r3}$.

From (3), the three voltage read-out results are as follows.

$$V_{r1} = (1+R)\cdot V_{base1} - R\,(V_{pix} + V_{OS}) \quad (4)$$

$$V_{r2} = (1+R)\cdot V_{base2} - R\,(V_{pix} + V_{OS}) \quad (5)$$

$$V_{r3} = (1+R)\cdot V_{base1} - R\,\left(V'_{pix} + V_{OS}\right) \quad (6)$$

$V_{pix}$ in (4) and (5) represents the pixel capacitor voltage at the time when the first and second charge sensing operations are performed. If the pixel is leakage free or the amount of leakage is negligible, $V_{pix}$ will be the same as $V_x$. $V'_{pix}$ in (6) is the pixel voltage when the third charge sensing is performed. Since there is a hold period between the write and charge-sensing operations, the leakage effect, if present, should be more apparent in $V'_{pix}$.

From (4) and (5), $R$, the ratio of $C_{pix}$ to $C_{AZ}$, can be derived as follows.

$$R = \frac{V_{r1} - V_{r2}}{V_{base1} - V_{base2}} - 1 \quad (7)$$

TABLE I.
SUMMARY ON CONTROL SIGNALS

| | functional | | charge-sensing | | | serial read-out | | |
|---|---|---|---|---|---|---|---|---|
| | AZ | WP | CWP | WDL | CTV | HV | RAZ | UB |
| $\phi_1$ | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| $\phi_2$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $\phi_3$ | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| $\phi_4$ | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| $\phi_5$ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| $\phi_6$ | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| $\phi_7$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

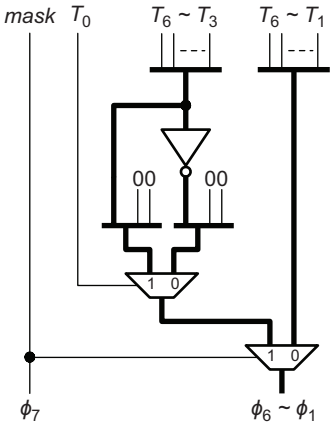


Figure 16. Control signal generation.

Then, from (4), (6), and the derived $R$, the voltage drop during the hold period can be derived.

$$\Delta V = V_{pix} - V'_{pix} = -\frac{V_{r1} - V_{r3}}{R} \tag{8}$$

The $\Delta V$ readings allow one to monitor the pixel leakage.

### F. Control signal generation

The control signal values with respect to each CS-buffer configuration are summarized in Table I.

One possible implementation of the CS-buffer control logic needed to generate these signals is shown in Figure 16. The $T$ control bus is 7-bit wide, from $T_6$ to $T_0$. Except for the $M$ signal, the other signals are the same for all CS-buffers.

In this implementation, the $\phi_7$ signal is directly connected to the CS-buffer's $mask$ signal. When $\phi_7$ equals 0, signals $\phi_6$ to $\phi_1$ are the same as $T_6$ to $T_1$. When $\phi_7$ equals 1, the CS-buffer may be in the read-out-auto-zero (RAZ) or the unit-buffer (UB) configuration. The $T_0$ signal is used to differentiate between these two configurations. If $T_0$ equals 1, the CS-buffer is in UB configuration—$\phi_1$ and $\phi_2$ are set to 0 and $\phi_3$ to $\phi_6$ are the same as $T_3$ to $T_6$. If $T_0$ equals 0, the CS-buffer is in RAZ configuration—$\phi_1$ and $\phi_2$ are set to 0 and $\phi_3$ to $\phi_6$ are obtained by complementing $T_3$ to $T_6$. Note that the $T_0$ signal has no effect on CS-buffers of which the $mask$ signal is 0.

### G. Discussions

One circuit implementation issue is the value of $C_{AZ}$. For convenience, let's rewrite (3) below.

$$V_{opamp} = (1 + R) \cdot V_{base} - R \cdot (V_{pix} - V_{OS}) \tag{9}$$

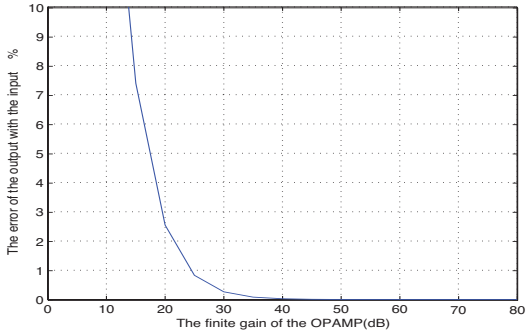


Figure 17. Finite opamp gain effect.

In the right hand side, one can see that the pixel voltage $V_{pix}$ is amplified by $R$. If $R$ is too large, $V_{opamp}$ will easily become negative and exceed the opamp's normal operating range. In the following, we choose $R = 1$, i.e., $C_{AZ} = C_{pix}$. In practice, $R$ will deviate from 1 due to process variations. Since $R$ will be derived in the post-processing process, the deviation is acceptable if only it does not cause the opamp to malfunction.

In addition to $R$, the charge-sensing results are also affected by the charge sensing base voltage $V_{base}$. Let $R$ be unity. To prevent the charge-sensing results from exceeding the opamp's operating range, the test voltage $V_x$ and the charge-sensing base voltage $V_{base}$ must meet the following constraints.

$$V_{DD} > 2 \cdot V_{base} - V_x + V_{OS} > V_{SS} \tag{10}$$

The finite opamp gain can lead to measurement errors. The simulation results in Section IV show that when the opamp gain is 20 dB or above, the measurement error is less than 2.5%. If better opamp is used, the error can be further reduced.

## IV. SIMULATION RESULTS

To validate the proposed technique, the CS-buffer is designed using LTPS technology. The simulation setup is as follows. According to [18], $C_{DL}$ and $C_{pix}$ are set to 500 and 700 fF, respectively. $C_{AZ}$ is set to 700 fF so that $R = 1$.

### A. The finite opamp gain effect

To estimate the impact of finite opamp gain, behavior simulation is performed using an opamp with -1.5 V offset voltage [15]. In Figure 17, the $x$ and $y$-axes are the opamp gain (dB) and the resulting measurement error (%), respectively. The error is about 2.5% with 20 dB opamp gain, and less than 1% when the gain is more than 25 dB, which is rather easy to achieve in LTPS process.

### B. The opamp performance

The opamp is the most important element of the CS-buffer. An LTPS opamp has been designed. To validate its performance, it is configured as a unit buffer. The I/O

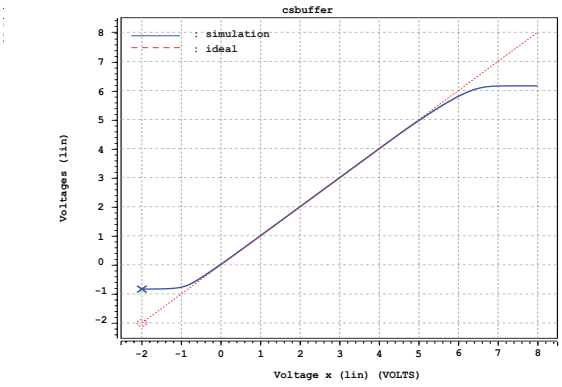


Figure 18. The unit buffer I/O curve.

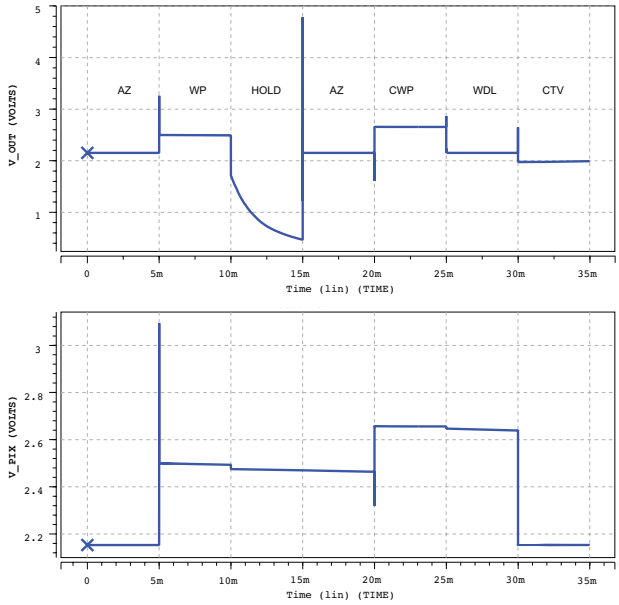


Figure 19. The transistor level simulation results.

relation of the unit buffer, obtained via circuit simulation, is shown in Figure 18. Within the target operating range, 0–5 V, the output tracks the input well.

### C. Transient simulation results

Transient simulation results of the transistor-level CS-buffer design are shown in Figure 19 where the top and bottom plots correspond to the pixel and the CS-buffer output voltages, respectively. The base voltage is set to be $V_{base} = 2.5$ V and an offset voltage of $V_{OS} = 0.35$ V is purposely added to the opamp to stress the auto-zero function during the write-data and charge-sensing operations. Also, the pixel is leaky—pixel voltage droop is observed when not driven.

The simulation is divided into 7 phases as marked. The first two phases (AZ and WP) correspond to the functional operations that write 2.5 V to the pixel. In the first AZ, the CS-buffer and pixel outputs are 2.153 V due to the 0.35 V opamp offset. Once the the opamp offset is stored in $C_{AZ}$, it is canceled in WP—the pixel voltage becomes 2.494 V which is very close to the ideal value 2.5 V.

From the second AZ to the CTV phases correspond to the charge-sensing operation. In the AZ and CWP phases, the offset compensated test data from $V_{ref}$ is written to the pixel. Then, in WDL, the data line is pre-charged. At the end of WDL, the pixel voltage is 2.642 V. Finally, in CTV, the remaining charge in the pixel is converted to voltage—the simulation result is 1.993 V which is close to the ideal value $2 \cdot V_{base} - V_{pix} - V_{OS} = 2.008$ V.

## V. Conclusion

In this paper, we have presented a built-in source driver design to facilitate TFT array testing. The proposed source driver is capable of executing charge-sensing test as well as serial test results read-out; it helps reduce the ATE performance requirement and the number of analog channels. In the future, we will investigate ways to reduce the induced area and performance overhead due to the CS-buffer.

## References

[1] Y. M. Liu, M. Miller, F. Henley, M. Nguyen, J. Levine, and H. Steemers, "Line open and short defect classification methodology for AMLCD array test Using voltage imaging," *SID Symposium Digest of Technical Papers*, 1995.

[2] S. L. Wright, K. W. Warren, P. M. Alt, R. R. Horton, C. Narayan, P. F. Greier, and N. Kodate, "Active Line Repair for Thin-Film-Transistor Liquid Crystal Displays," *IBM Journal of Research and Development*, 1998.

[3] L. C. Jenkins, R. J. Polastre, R. R. Troutman, and R. L. Wisnieff, "Functional Testing of TFT/LCD Arrays," *IBM Journal of Research and Development*, 1992.

[4] Y. C. Lin and H. D. Shieh, "In-Process Functional Testing of Pixel Circuit in AM-OLEDs," *IEEE Transactions on Electron Devices*, 2005.

[5] J. C. Hunter, M. Brunner, R. Schmid, and F. Abboud, "Issues and Challenges Associated with Electrical Testing of Large LCD-TV Arrays," *SID Symposium Digest of Technical Papers*, 2005.

[6] S. L. Wright and R. Nywening, "A Transmission-Line Approach for Line-Continuity Testing of Active-Matrix Arrays," *SID Symposium Digest of Technical Papers*, 1995.

[7] M. Kodate, F. R. Libsch, T. Iwami, L. Jenkins, M. Mastro, Y. Mekata, R. Polastre, and T. Taguchi, "Next Generation TFT-Array Testing for High Resolution/High Content AMLCDs," *SID Symposium Digest of Technical Papers*, 1999.

[8] T. Nagano, H. Kageyama, H. Akimoto, Y. Mikami, and H. Sato, "A 5-Inch SVGA Low-Temperature Poly-Si TFT-LCD with Integrated Digital Interface Driver," in *International Conference on Solid-State and Integrated-Circuit Technology*, 2001.

[9] T. Nakamura, M. Karube, H. Hayashi, K. Nakamura, N. Tada, H. Fujiwara, J. Tsutsumi, and T. Motai, "Low-Temperature Poly-Si TFT-LCD with an Integrated Analog Circuit," *Journal of the Society for Information Display*, 2002.

[10] Y. S. Yoo, J. Y. Choi, H. S. Shim, and O. K. Kwon, "A high accurate analog buffer circuit using low tem-perature poly-Si TFT," *SID Symposium Digest of Technical Papers*, 2004.

[11] C. W. Lin, T. K. Chang, C. K. Jan, M. H. Hsieh, C. Y. Tsai, S. C. Chang, and Y. M. Tsai, "LTPS Circuit Integration for System-on-Glass LCDs," *Journal of the Society for Information Display*, 2006.

[12] A. Nathan, G. R. Chaji, and S. J. Ashtiani, "Driving Schemes for a-Si and LTPS AMOLED Displays," *Journal of Display Technology*, 2005.
[13] S. H. Jung, H. S. Shin, J. H. Lee, and M. K. Han, "An AMOLED Pixel for the $V_T$ Compensation of TFT and a p-Type LTPS Shift Register by Employing 1 Phase Clock Signal," *SID Symposium Digest of Technical Papers*, 2005.
[14] G. R. Chaji, D. Striakhilev, and A. Nathan, "A novel a-Si:H AMOLED Pixel Circuit Based on Short-Term Stress Stability of a-Si:H TFTs," *IEEE Electron Device Letters*, 2005.
[15] M.-D. Ker, C.-K. Deng, and J.-L. Huang, "On-Panel Output Buffer with Offset Compensation Technique for Data Driver in LTPS Technology," *Journal of Display Technology*, 2006.
[16] A. Laknaur and H. Wang, "Built-In-Self-Testing Techniques for Programmable Capacitor Arrays," in *International Symposium on Quality of Electronic Design*, 2005.
[17] S. R. Durbha, A. Laknaur, and H. Wang, "Investigating the Efficiency of Integrator-Based Capacitor Array Testing Techniques," in *VLSI Test Symposium*, 2006.
[18] Y. Dai, *Design and Operation of TFT Panels*. Wu-Nan Culture Enterprise.

**Chen-Wei Lin** received his B.S. degree in Electronics Engineering from National Chiao Tung University, Taiwan, in February 2006, after which he received his M.S. degree in Electronics Engineering from National Taiwan University, Taiwan, in July 2007.

Since then he has been working in Thin-Film Transistor Technology Department of Panel integration Division I in Display Technology Center of Industrial Technology Research Institute (ITRI), Taiwan.

**Jiun-Lang Huang** received the B.S. degree in Electrical Engineering from National Taiwan University, Taiwan, in 1992, and the M.S. and Ph.D. degrees in Electrical and Computer Engineering from the University of California at Santa Barbara in 1995 and 1999, respectively.

From 2000 to 2001, he served as an assistant research engineer in the ECE department, UCSB. In 2001, he joined National Taiwan University and is currently an associate professor in the Graduate Institute of Electronics Engineering and the Department of Electrical Engineering. His main research interests include design-for-test (DfT) and fault/variation-tolerant design for digital and mixed-signal circuits.