DL(2*m*): A New Scalable Interconnection Network for System-on-Chip

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***Abstract*—With the feature size of semiconductor technology reducing and intellectual properties (IP) cores increasing, on chip communication architectures have a great influence on the performance and area of System-on-Chip(SoC) design. Network-on-Chip(NoC) has been proposed as a promising solution to complex SoC communication problems and has been widely accepted by academe and industry. Focusing on decreasing node degrees, reducing links and reusing router nodes, a regular NoC architecture, named Double-Loop(DL(2*m*)) interconnection network, is proposed. The topology of DL(2*m*) is simple, symmetric and scalable in architecture, and it is 3-regular plane graph with 4m nodes. The nodes of DL(2*m*) adopt Johnson coding scheme that can make the design of routing algorithms simple and efficient. The DL(2*m*) was compared with Ring and 2D Mesh by simulating and analysing, both under uniform load and under more realistic load assumptions in the several network size scenarios. The results show that the DL(2*m*) topology is a good trade-off between performance and cost, and it is a better NoC topology when there are not too many network nodes.**

***Index Terms*—system-on-chip, network-on-chip, network topology, routing algorithms**

I. INTRODUCTION

Driven by the advances of semiconductor technology, the realization of the future complex System-on-Chip (SoC) consisting of billions of transistors fabricated in technologies characterized by 65 nm feature size and less will soon be reality[1-3]. Such SoC implies the seamless integration of hundreds, or ever more, intellectual properties (IP) cores including processing resources and storage resources performing different functions and operating at different clock frequencies.

Existing on-chip interconnect architectures will give rise to some problems. The most frequently used on-chip interconnect architecture is the shared medium arbitrated bus, where all communication devices share the same transmission medium. Every additional IP core connected to the bus adds to this parasitic capacitance, in turn causing increased propagation delay. As the bus length increases and/or the number of IP cores increases, the associated delay in bit transfer over the bus may will increase and eventually exceed the targeted clock period. This thus limits, in practice, the number of IP cores that can be connected to a bus and thereby limits the system scalability[4].

Consequently，Several research groups have advocated the use of a communication-centric approach to integrate IP cores in complex SoC. This new SoC model allows the decoupling of the processing elements (i.e., the IP cores) from the communication fabric (i.e., the network). The need for global synchronization can thereby disappear. This new approach employs explicit parallelism, exhibits modularity to minimize the use of global wires, and utilizes locality for power minimization[5]. In a communication-centric approach, the communication between IP cores can take place in the form of packets. Packet switched Network-on-Chip (NoC) has been proposed in [6,7] as a viable and attractive alternative to future complex SoC.

The ability of the NoC to efficiently disseminate information depends largely on the underlying topology. Besides having a paramount effect on the network latency, throughput, area, fault-tolerance and power consumption, the topology plays an important role in designing the routing strategy and mapping the cores to the network nodes [5,8].

Generally speaking, determining the optimal topology to implement any given application does not have a known theoretical solution[8]. Although the synthesis of customized architectures is desirable for improved performance, power consumption and reduced area, altering the regular grid-like structure brings into the picture significant implementation issues, such as floorplanning, uneven wire lengths (hence, poorly controlled electrical parameters), etc. Consequently, ways to determine efficient topologies that trade-off high-level performance issues against detailed implementation constraints at micro- or nano-scale level need to be developed.

A network topology can be regular or irregular and it is non-blocking if it can manage all the requests that are offered to it. In a packet switched case this kind of

network is also called as non-interfering network. Non-interfering network can deliver all the packets in guaranteed time[9]. In NoC, some basic regular network topologies have been proposed, such as 2D Mesh, 2D Torus, Folded 2D Torus, Fat-tree, Chordal Ring, Bi-directional Ring etc. 2D Mesh is the most studied topologies (over 50% of the cases)[10,11].

In this paper, a regular NoC architecture, named Double-Loop(DL(2*m*)) interconnection network, is proposed. The topology of DL(2*m*) is simple, symmetric and scalable in architecture, which is 3-regular plane topology with 4*m* nodes. The nodes of DL(2*m*) apply Johnson coding scheme that can make the design of routing algorithms more simple and efficient. The DL(2*m*) was compared with Ring and 2D Mesh （which are planar graph topologies, torus is a non-planar topology）by simulating and analysing. The results show that DL(2*m*) is a better NoC topology, when there are not too many network nodes.

The remainder of the paper is organized as follows. Section 2 describes the topology architecture and the properties of DL(2*m*). In section 3, we present a routing algorithm in DL(2*m*). Section 4 compares the performance of DL(2*m*), Ring and 2D Mesh by simulating and analysing. Section 5 summarizes the results and concludes the directions for future research.

II. TOPOLOGY OF DL(2m)

A. Topology of DL(2m)

Definition 1. Binary unit-distance cyclic code is a binary code whose each two adjacent codes have one and only one bit different(unit distance characteristic), and the first code and the last one in those codes have one and only one bit different(cycle characteristic).

Definition 2. Binary code represents each number in the descending sequence of integers {*n*-1,*n*-2,…,2, 1, 0} as a binary string of length $m=\lceil n/2 \rceil$ by an order. The binary code has the properties of definition 1 and as follows: i) for $0<k<m$, $Q=Z_{m-1}\ldots Z_k\ O_{k-1}\ldots O_0$($Z_i$ stands for 0, O_j stands for 1, $k\le i\le m-1, 0\le j\le k-1$) is the code of integer *k*; ii) for $k>m$, $Q=O_{m-1}\ldots O_{k-m}\ Z_{k-m-1}\ldots Z_0$($Z_i$ stands for 0, O_j stands for 1, $0\le i\le k-m-1, k-m\le j\le m-1$) is the code of integer *k*; iii) for $k\equiv m$, $Q=O_{m-1}\ldots O_0$(O_i stands for 1, $0\le i\le m-1$) is the code of integer *k*; iv) for $k\equiv 0$, $Q=Z_{m-1}\ldots Z_0$(Z_i stands for 0, $0\le i\le m-1$) is the code of integer *k*. This binary code is called Johnson code.

Definition 3. Double-Loop (DL(2*m*)) interconnect-tion network is a kind of network topology with the following characteristics: 1) DL(2*m*) has 4*m* nodes and 6*m* links, which consists of two rings, an outer ring and an inner ring, each containing 2*m* nodes; 2) The nodes of the outer/inner ring of DL(2*m*) can be marked with *m* bits Johnson code and 1 bit ring sign at most significant bit, where the outer ring is marked sign 1 and the inner ring is 0; 3) In which the coding rules of the nodes are as follow: When there is just one bit different between any two nodes, there will exist a link between them, that is to say, these two nodes are neighboring to each other.

An example of a DL(2*m*) is shown in figure 1, where *m* equals to 4, which is composed of $4\times4=16$ nodes and $6\times4=24$ links. The nodes of the outer/inner ring of DL(2*m*) can be marked with 4 bits Johnson code and 1 bit ring sign at most significant bit, where the outer ring is marked sign 1 and the inner ring is 0.

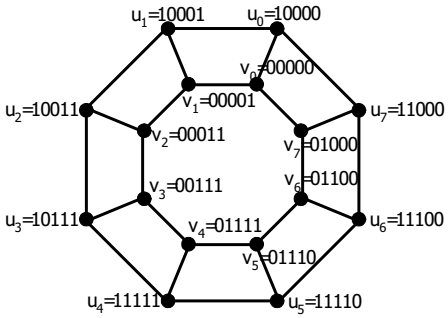


Figure 1. DL(2m) network, where m equals to 4.

B. Network properties of DL(2m)

Some of the most common NoC architectures belong to the classes of the Ring and *k*l* 2D Mesh. This section addresses these principle properties of DL(2*m*) and compares it with 2D Mesh and Ring.

Some of the most interesting characteristics of the DL(2*m*) are: ①network with regular topology, ②vertex symmetry (same topology appears from any node), ③ edge-transitivity, ④constant node degree (equals to 3), which make the router hardware design more simple and effective, ⑤ homogeneous building blocks (the same router structure can be used to compose the entire network), ⑥ the codes sequence of each circuit of DL(2*m*) is a binary unit-distance cyclic codes, ⑦ the node of DL(2*m*) has three and only three adjacent node codes, ⑧ DL(2*m*) has better scalability, the granularity of size scaling is 4, ⑨ the distance of two random $A(A_mA_{m-1},\ldots,A_1A_0)$, $B(B_mB_{m-1},\ldots,B_1B_0)$ $(A_i,B_i\in\{0,1\}, i\in\{0,1,\ldots,m\text{-}1,m\})$ is $d(A,B)=\sum_i A_i\oplus B_i$, and ⑩simple routing scheme. By assuming a NoC of bidirectional links and $N=4*m=k*l$ nodes, the number of links, network degree, network diameter, average distance and symmetry is shown in table I. A significant worst case index, named the network diameter is defined as the maximum shortest path length between any pair of nodes in the topology. The average network distance is defined as the average path length of all different paths in the network.

The network diameter of real 2D Mesh($N=k*l$) topologies with *N* nodes shows quite unpredictable fluctuations between the ideal Mesh($N=k*l$, $k\equiv l$) values and the Ring diameter values, as shown in figure 2. In figure 3, we show the average network distance for Ring, ideal and real 2D Mesh, and DL(2*m*). Ideal Mesh behavior is obtained by real Mesh only under specific N values (that is when $N=k*l$ and $k\equiv l$). These results are quite indicative of the difference that may exist between theory results in ideal cases and real scenarios, for Mesh topologies. Results in figures 2 and 3 show that DL(2*m*)

is expected to have competitive and linear behavior, on the average and worst case scenarios, due to node symmetry and regular topology with respect to Ring and real Mesh topologies.

TABLE I. Comparison of topology properties of four planar interconnection network[13-15]

Type of Network	Network node degree	Number of links	Diameter	Average distance	Symmetry
DL(2*m*)	3	6*m*	*m*+1	$2(m^2+1)/(4m-1)$	Yes
Ring	2	4*m*	2*m*	*m*	Yes
2D Mesh(*ideal*)	4	$4(2m-\sqrt{m})$	$2(2\sqrt{m}-1)$	$(4m-1)/3\sqrt{m}$	No
2D Mesh(*real*)	4	2*kl*-(*k*+*l*)	*k*+*l*-2	(*k*+*l*)/3	No

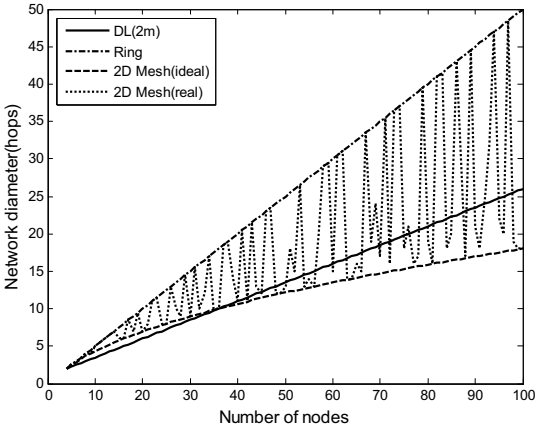


Figure 2. Comparison of network diameter in Ring, ideal and real 2D Mesh and DL(2m).

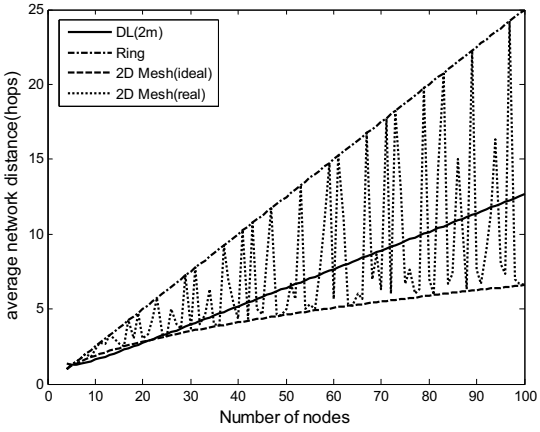


Figure 3. Comparison of network average distance in Ring, ideal and real 2D Mesh and DL(2m).

The zero-load latency is proportional to the network average distance. Increasing network degree can reduce the average distance of an interconnection network. So it is very difficult to accurately evaluate the latency of interconnection networks with different degree, if only using the average distance without taking into account the network degree. We use the normalized average distance when analyzing the latency. The normalized average distance of an interconnection network is the result of the network average distance multiplied by the network degree[16]. Figure 4 compares the normalized average distance generated by DL(2m), Ring and 2D Mesh, respectively. Figure 4 indicates that the zero-load latency of DL(2m) is lower than 2D Mesh when the scale of network is not greater than 44.

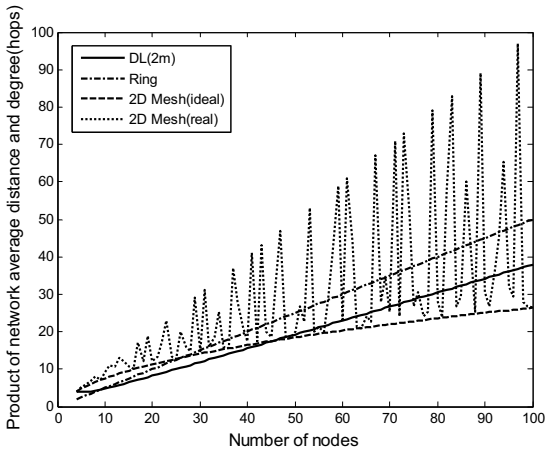


Figure 4. Comparison of product of network average distance and degree.

The analysis results show that when there are not too many nodes, DL(2*m*) is a better candidate for constructing the interconnection network for SOC, taking into account the node degree, number of links and diameter.

III. ROUTING ALGORITHM OF DL(2m)

Routing algorithm is a key factor which affects the efficiency of the communication of NoC. The distributed dimension-order routing is adopted in this paper. The characteristic of DL(2*m*) and nodes code is fully utilized in the routing. In this approach, each node, upon receiving the packet, decides whether the packet should be delivered to the local node or forwarded to adjacent node. During the routing decision process, the routing algorithm needn't the state information of the complete network, and just uses code of the current and destination node, thus it can reduce the network communication overhead and node storage overhead.

A source node $S(S_mS_{m-1},\ldots,S_1S_0)$ sends data packet to a destination node $D(D_mD_{m-1},\ldots,D_1D_0)$. The routing algorithm of the shortest path of DL(2m) is described as follows.

i) Computing of the shortest path. For DL(2*m*), the shortest path between *S* and *D* is denoted: *SP*=Hamming(S ⊕ D), where "⊕" represents

nonequivalence operation and function Hamming means Hamming distance which is the sum of the total number of 1 in binary number. The operation is simple in the implementation of hardware mechanism.

ii) Computing of the number of the shortest path. The number of the shortest path between node S and node D is N_{SP} as follows. a) If Hamming $(S_m \oplus D_m) \equiv 0$ and Hamming ($S_{m-1}\ldots S_1S_0 \oplus D_{m-1}\ldots D_1D_0) \equiv m$, then N_{SP}=2, else N_{SP}=1. b) If Hamming $(S_m \oplus D_m) \equiv 1$ and Hamming ($S_{m-1}\ldots S_1S_0 \oplus D_{m-1}\ldots D_1D_0) \equiv m$, then N_{SP}=4, else N_{SP}=2 (especially, the number of the shortest path is infinite when Hamming $(S_mS_{m-1}\ldots S_1S_0 \oplus D_mD_{m-1}\ldots D_1D_0)$ equals to 0).

iii) Generation of routing information in nodes. When Johnson coding is used in DL(2m) topology, the node code implies the routing information of complete network. The node S has three adjacent nodes according to section 3.3. It has two adjacent nodes in the same ring, that is, S_{S1}= S_m $\overline{S_0}$ $S_{m-1}\ldots S_2S_1$, S_{S2}= S_mS_{m-2} $S_{m-3}\ldots S_1S_0$ $\overline{S_{m-1}}$, and one adjacent node in the dissimilar ring, S_D= $\overline{S_m}$ $S_{m-1}S_{m-2}\ldots S_1S_0$. Then the distance between the three adjacent nodes and destination node is obtained: d_{S1}=Hamming $(S_{S1} \oplus D)$, d_{S2}=Hamming $(S_{S2} \oplus D)$, d_D=Hamming $(S_D \oplus D)$. if $d_D \equiv 0$, then $d_{\min}=d_D$, else $d_{\min}=\min\{d_{S1},d_{S2}\}$. Source node S sends packet to the $d_{\min}$ corresponding adjacent node, S is modified whose value is the code of $d_{\min}$ corresponding adjacent node. Computing the value of d, if $d\equiv 0$, then node S is destination node, else iterate the process.

In the same ring, the adjacent node is generated by simply implementation of register shift. The adjacent node of the dissimilar ring is performed *NOT* operation for the most significant bit. The node coding of DL(2m) network can be dynamically changed. The nodes codes only show relative position between nodes. In worst case，the longest path of routing can't exceed network diameter. The routing mechanism is very simple and easy to be implemented in hardware with low implementation cost, and the complexity of the algorithm is O(m+1).

IV. Performance Evaluation

One key aspect about NoC is the performance evaluation. To compare and contrast different NoC architectures, a standard set of performance metrics can be used. For example, it is desirable that an MPSoC interconnect architecture exhibits high throughput, low latency, energy efficiency, and low area overhead [17]. Generally, the performance metrics of the average network latency and the average network throughput are of great importances [15]. To evaluate the proposed DL(2m) architecture, the DL(2m) was compared with Ring and 2D Mesh by simulating and analyzing in three different network sizes(16,32,64 nodes).

We have developed a discrete event, cycle accurate NoC simulator. It provides substantial support to experiment with NoC design in terms of routing algorithms and applications on various topologies. The simulator is written in systemC. The dimension-order routing and wormhole packet-switching is adopted in three topologies, which ensure the justness of analyses. DL(2m), Ring and 2D Mesh nodes have been defined with the same node architecture, excepted the number of links.

Each node has an external network interface to connect the IP core to the NoC. The external IP core can act as a packet source and/or as a packet destination (sink) depending on the simulated scenario. In our simulations, each source IP core generates packets and sends them to other IP cores. Each packet has three 32-bit flits(flow control unit, flit). The first (head) flit of a packet is sent to the routing mechanism of the node, and then transferred on the output of the target channel (if next node input channel is room). Once the head flit has been processed by the routing element of a node, a switching mechanism is defined to forward all immediately following packet-flits to the outgoing links of the target path to the destination node. We changed the flit rate injection from 0.05 flit/cycle/node to 0.5 flit/cycle/node. Each input channel consists of 8 flits fifo buffer. Each output channel consists of one flit buffer. The clock frequency of NoC is 1GHz.

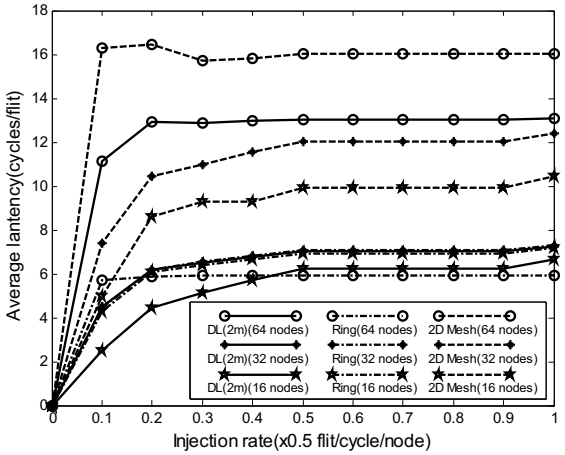
For single hot-spot destination scenario and homogeneous destinations scenario, we simulated and analysed the performance of Ring, DL(2m) and 2D Mesh in three different network sizes as follows.

A. Single hot-spot destination scenario

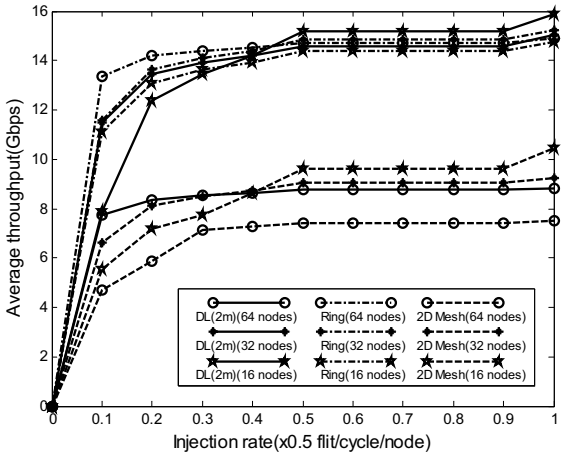
The destination node of single hot-spot have been taken in different points on the Mesh topology (in symmetric Ring and DL(2m), this would not have any difference). Figure 5 shows the performance index of the average latency and average throughput as a function of the injection rate parameter of the source nodes and the number of network nodes when hot-spot destination is present in the system (that is, one single destination node for all packets). All the source nodes send packets to single hot-spot destination except destination node.

Figure 5 shows the average latency and the average throughput obtained by DL(2m), 2D Mesh and Ring topologies under one single hot-spot destination node, as a function of the number of nodes N and the injection rate parameter of multiple source nodes. By assuming a homogeneous injection rate, the result shows that the bigger the network size, the worse the performance of the average latency and the average throughput in same topology. And the simpler the topology, the better the performance in same network size. When all the sources homogeneously increase the injection rate, the average latency and the average throughput increase with the injection rate of source nodes, and the destination node saturation is obtained.

Therefore, the system bottleneck under single hot-spot traffic destination scenarios is the destination node and NoC topologies. The performance of DL(2m) is much better than 2D Mesh. The scalable and symmetric architecture of DL(2m) would give the same advantages of simple Ring, under the hot-spot communication viewpoint.



a）Average latency of NoC



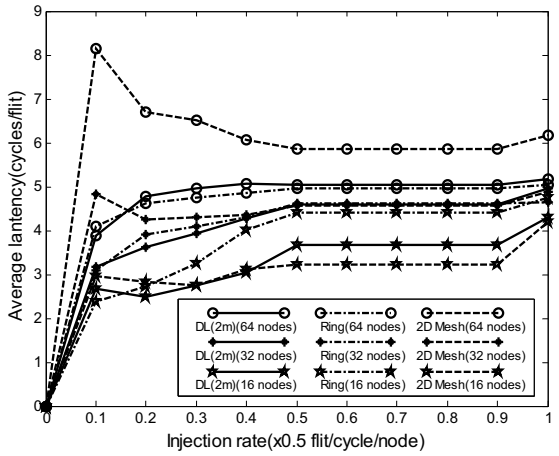
b）Average throughput of NoC

Figure 5. Comparison of performance, one hot-spot destination node.

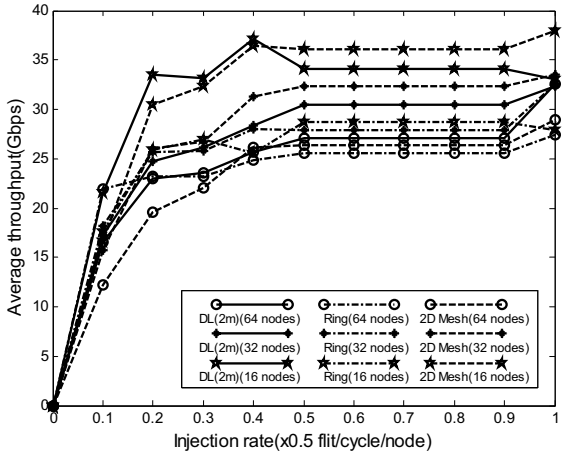
B. Homogeneous destinations scenario

Figure 6 a) shows the average latency obtained by DL(2*m*), 2D Mesh and Ring topologies under homogeneous source and destination distribution scenarios. All the nodes behave like sources and can be addressed as destination for packets with uniform probability distribution. Latency is shown as a function of the number of nodes N and the injection rate parameter of multiple source nodes. The result shows that DL(2*m*) and Ring topologies outperform 2D Mesh, and scale better when the number of nodes is high. Under this scenario, 2D Mesh shows a smaller average latency than DL(2*m*) only with not many nodes and when the local injection rate of all source nodes is greater than 0.2 flits/cycle/node. Figure 6 b) shows the throughput results with respect to the NoC topology and the number of nodes, under homogeneous scenarios with uniform distribution of sources and destinations. Specifically, all the nodes behave like sources and can be addressed as destination for packets, with uniform probability distribution.

When all node sources increase the injection rate, the average latency and the average throughput increase with the injection rate of source nodes, up to the set of destination nodes and/or the network becomes saturated. This performance index shows that DL(2*m*) and 2D Mesh topologies outperform Ring, and scale better when the number of nodes is low. Under this scenario, 2D Mesh shows a better throughput than DL(2*m*) only with many nodes and when the local injection rate of all source nodes is greater than 0.15 flits/cycle/node. On the other hand this scenario is hardly obtained in real systems, and this does not constitutes a good motivation to prefere the adoption of 2D Mesh in favour of the DL(2*m*) topology. As expected, the bottleneck emerging in this scenario is basically given by the communication infrastructure. This is confirmed also by the worst performances obtained by the Ring topology.



a）Average latency of NoC



b）Average throughput of NoC

Figure 6. Comparison of performance, homogeneous system with all nodes working as packet sources and destinations.

V. CONCLUSION

Focusing on decreasing node degrees, reducing links and reusing IP cores, we have proposed a new topology architecture DL(2*m*) for NoC. The topology of DL(2*m*) is very simple, planar, symmetric and scalable in architecture, and it is 3-regular plane graph with 4*m* nodes.This paper presents a novel Johnson coding

method for nodes coding which adapts to DL(2*m*) topology architecture. The nodes of DL(2*m*) apply Johnson coding scheme that makes the design of routing algorithm more simple and efficient. The DL(2*m*) was compared with Ring and 2D Mesh by simulating and analysing, both under uniform load and under more realistic load assumptions in the several network size scenarios. The results show that the DL(2*m*) topology is a good trade-off between performance and cost. It is a better candidate for NoC topology, when there are not too many network nodes.

In future research, we will map the application of wireless communication on DL(2*m*) topology architecture. When applications behaviors can not be predicted at compile time, on-line scheduling approaches are usually needed. Significant work is needed to develop efficient performance and energy-aware on-line scheduling algorithm for NoC.

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