

Design Overview Of Processor Based Implantable Pacemaker

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Abstract—Implantable pacemaker is a battery operated real time embedded system, which includes software/hardware codesign strategy. As it is placed within the heart by surgery, battery life is an important constraint to extend device lifetime. In this paper, pacemaker's functionalities like basic pacing, pulse width, refractory period in VOO mode has been realized using ultralow power processor MSP 430F1611 and IAR workbench. Software related instruction level instantaneous current is measured and Current/Energy performance, battery longevity is tested. It is verified that, change in pure cost and interinstruction cost (current/Energy) varies from 2.0 to 3.0 %. This methodology seems to be an innovative concept in software related energy estimation of such power critical real time system.

Index Terms — ultra low power, implantable pacemaker, real time system, current consumption, low power modes, VOO mode

I. INTRODUCTION

A. Implantable pacemaker [13, 17]

Heart consists of Sinoatrial node (SA); called pacemaker generates electrical impulses, which are responsible for the contraction and dilation of heart muscles. These electrical impulses take care of heart muscle synchronization and hence blood pumping. Although, all the heart cells possess the ability to generate electrical impulses or action potentials, SA node is responsible for the whole heart's beat. After contraction of the atria, the impulse proceeds to the Atrioventricular (AV) node. The impulse slows at the AV node, which allows time for contraction of the atria. Just below the AV node, the impulse passes quickly through the bundle of His, the right and left bundle branches and the Purkinje fibers and lead to contraction of the ventricles as shown in figure 1. In case of damaged intrinsic conduction system, an artificial device known as pacemaker is implanted within the heart. Device monitors the heart rate and stimulates heart when it beats too slow

or does not beat. Main goal of cardiac pacing is to artificially stimulate a diseased heart to operate at normal rate.

An artificial pacemaker is real time embedded system with hermetically sealed titanium encapsulation that delivers a synchronized rhythmic electric stimulus to the heart muscle in order to maintain an effective cardiac rhythm for long periods of time. Pacemaker system consists of device and leads. Flexible insulated unipolar/bipolar leads with electrode tip are inserted through vein into the heart. These carry impulses from the pacemaker device to the heart, to stimulate. Similarly information is transferred from heart to the device. Implanted pacemaker is battery operated real time embedded system which must be smaller in size and less in weight and must operate with low power to increase battery life and surgery period too. Pacemaker works in three operating modes [8, 14].

(i) Free running (fixed or asynchronous): It is insensitive to any rhythm that may develop in paced chamber (VOO mode).

(ii) Inhibited: It senses cardiac activity and does nothing if this is present, but delivers a stimulus after an elapsed time if no further cardiac activity occurs to inhibit operation.

(iii) Triggered: It senses activity and delivers a stimulus in a desired way.

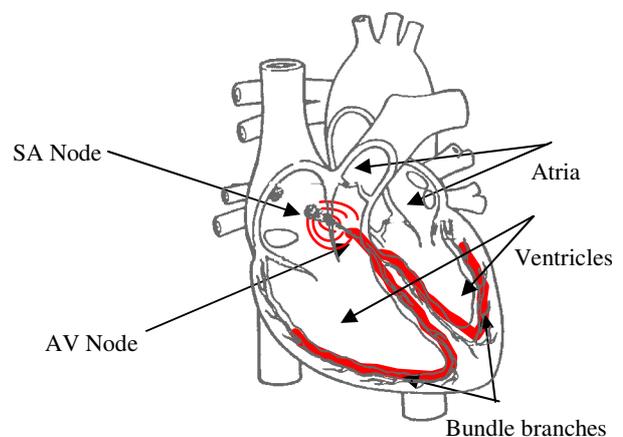


Figure 1. Electrical conduction system of heart.

This paper is based on "Hardware/software codesign techniques in low power embedded system," and "Design overview of low power implantable pacemaker using MSP430F1612" by S. D. Chede and K. D. Kulat, which is appeared in proceedings of IMECS 2007, held at Hong Kong, during 21-23 March, 2007 and SPIT-IEEE international conference held at Mumbai, during 4-5 February, 2008 respectively.

B. Pacemaker timing parameters

- **Basic pace interval:** The basic pace interval is the period of time that pacemaker awaits to apply stimulus to the heart. It is measured in beats/min.
- **Escape interval:** The escape interval is the period of time that the pacemaker awaits after a spontaneous QRS has been generated. It is measured in ms.
- **Ventricular Refractory period (VRP):** The VRP is the amount of time that the sense circuit is turned off. This is done to avoid sensing the pacemaker own stimulus, the paced QRS complex, T wave and after potentials. If the sensing circuit is turned on, then it will generate stimuli to all these events, causing ventricular fibrillation. It is measured in msec.
- **Pulse width:** It is the amount of time the pulse generator will supply the stimulus to the heart. This parameter is important to capture heart. Capture is the action of generating a potential that develop chain reaction through out the ventricle. The pulse width is measured in msec.

C. Modes of operation

North American Society of Pacing and electrophysiology (NASPE) and British pacing and Electrophysiology (BPEG) used nomenclatures to classify pacemakers like VVI, VVT, VOO, AAI, AAT and AOO is given in table I [6]. VVI means pacemaker sense the ventricle and pace the ventricles in inhibited mode. VOO means an asynchronous mode in which ventricle is paced with no chamber sensed and no response to sensing i.e. irrespective of the heart signal, pacemaker generates pacing pulses.

TABLE I.
NASPE/BPEG CODE REVIEW

Position	Category	Code
I	Chamber(s) Paced	O=None
		A= Atrium
		V=Ventricle
		D=Dual (A+V)
II	Chamber(s) sensed	O=None
		A=Atrium
		V=Ventricle
		D=Dual (A+V)
III	Response to sensing	O=None
		T=Triggered
		I=Inhibited
		D=Dual (A+V)
IV	Rate Responsive	O=None
		R=Rate Modulation
V	Multirate Pacing	O=None
		A= Atrium
		V=Ventricle
		D=Dual (A+V)

II. PACEMAKER DESIGN GOALS : BENCHMARKS TEROS MODEL SSIR 603 [15]

Pacing Modes: VVI, VVT, VOO, OVO, AAI, AAT, AOO, OAO, VVIR, VVTR, VOOR, AATR, AORR, AAIR

Basic Pacing Rates: From 32 to 120 bpm in steps of 2 bpm.

Pulse Widths: 20 values from 0.07 to 1.50 msec.

Pulse Amplitudes: 36 values from 0.2 to 7.5 Volts

Pacing Polarity: Unipolar/Bipolar

Sensitivities: From 0.4 to 6.4 mV in steps of 0.4 mV

Sensing Polarity: Unipolar/Bipolar

Refractory Periods: From 200 to 500 msec in steps of 15 msec.

Hysteresis: From 2 to 40 min⁻¹ in steps of 2 min⁻¹ or disabled.

Hysteresis Search: When enabled, every 700 stimuli produces a Hysteresis period.

Upper Rate in Trigger Mode: From 80 to 180 min⁻¹ in steps of 2 min⁻¹

Upper Rate: From 80 to 180 min⁻¹

Response to Activity: From 1 to 16

Reaction Time: From 10 to 60 sec, in steps of 10 sec to increase the rate 80 min⁻¹

Recovery Time: From 1 to 10 min in steps of 1min to decrease the rate 80 min⁻¹

Automatic refractory Switch: When programmed, if the rate is greater than 120 min⁻¹, the refractory period switches to 250 msec.

Temporary Programming: Asynchronous pacing with rates from 32 to 380 min⁻¹

Mode: VOO (Magnet response)

Rate: BOL (Beginning of life): 96 min⁻¹

ERI (Elective replacement):84 min⁻¹

ERI (Effective replacement): When the remaining capacity of the battery is between 3.5% and 7% of the initial capacity, the pacing rate switches to 84 min⁻¹ when a magnet is applied.

EOL (End of Life): When the remaining capacity of the battery is under 3.5 % of the initial capacity, the pacing rate slows 10 min⁻¹ and if programmed in an activity response mode, this mode is deactivated.

Battery Chemistry and Model: Lithium Iodine WG 8711

Initial Voltage: 2.8 Volts

Maximum Available Capacity: 0.85 Ah

Dimensions: 53×40.5×7.5 mm

Mass: 25.1 gram

Case Material: Titanium

Connector: 3.2mm, IS-1

III. PACEMAKER SYSTEM OVERVIEW AND DESIGN REQUIREMENTS

Embedded computer system is hardware/software codesign with dedicated processor. As most of the embedded portable devices are battery operated, low power design methodology plays a crucial role in design. A large number of embedded computing applications are power critical and power constraints form an important

part of the design specification. Processor is an important computing element in battery operated real time embedded system and consumes most of the battery energy [7]. Even with advanced battery technology, power budget is limited. Appropriate /optimized software design and analysis became a latest trend in modern embedded systems.

Basic blocks of implantable pacemakers are ECG front end circuitry, ultra low power microcontroller, battery and output circuitry to stimulate heart. Heart signal is sensed by electrodes. Main emphasis must be given on size, weight, encapsulating material and increase in life span of battery i.e. up to 10 to 12 years. The front end senses voltage generated by the pumping action of the heart which is small signal with many noise components. This circuit consists of differential amplifier, filter, level shifter, synchronizing circuit etc. To pace abnormal heart with a pulse of 5 to 7.5 volts, multiplier along with switch network is used.

Implantable pacemaker consists of external comparator. Cardiac signal is sensed by unipolar or bipolar electrodes and is amplified by a low noise pre-amplifier, gain amplifier. It is filtered by second order low pass filter to get appropriate ECG. This signal is applied to the comparator. Comparator is used as a threshold detector, to detect the heart beat event executed by the heart and generates a pulse with every heartbeat. External comparator consists of two inputs i.e. ECG and threshold voltage. It generates pulse depending on the threshold voltage level. In the absence of heart signal no pulse is generated. Comparator output (synchronizing pulse) is connected to the 2.0 port of the MSP 430F1611 processor. Output stage called charge pump, consists of voltage multiplier/pulse generator to stimulate heart. A high voltage pulse of 5 to 7.5Volts is delivered to the heart through pacing electrodes. The amplitude and pulse width must be customized for each patient. Supply Voltage Supervisor (SVS) is necessary to monitor battery voltage. Various blocks customized as shown in figure 2, are integrated in MSP 430F1611 ultra low power microcontroller.

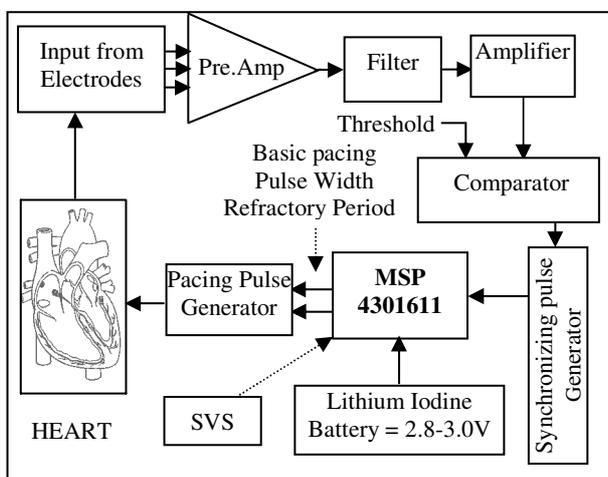


Figure 2. Implantable pacemaker block diagram..

VLSI based analog/digital custom processor and interfacing peripherals are used in implantable pacemaker [1]. It increases cost and time to market. Some ultra low power microcontrollers are available today which will be better choice for crucial biomedical applications. Pacemaker is a computer controlled real time system with predefined tasks priority. Microcontroller with optimized software is basic component in it. Microcontroller to be chosen must have low power consumption and required memory space. ARM is very important processor in modern embedded system. It has features like low power consumption, high speed, code size optimization using thumb and ARM mode, Dynamic voltage Scaling (DVS) functionality for energy consumption optimization [5]. In comparison with ARM, MSP430F1611 is a 16 bit RISC processor which has features like ultralow power consumption, speed of 8 MHz lesser than ARM, but suitable to handle heart signal, and various power down modes. It has standby current , lesser than that for PIC181f242, and Maxq 2000 processors. Lithium Iodine batteries are standard in modern pacemaker [9, 10].

IV. ADVANCED FEATURES OF MSP 430F1611 ULTRALOW POWER PROCESSOR

The Texas instruments MSP430 family of mixed signal microcontroller has 3-stage pipe line, 16 bit data processing (RISC), Von Neumann CPU architecture. It consists of inbuilt peripherals. The MSP 430F1611 has two 16 bit timers, a high performance 12 bit A/D converter, dual 12 bit D/A converters, one USART, DMA, 48 I/O pins, comparator and supply voltage supervisor. The device is a powerful 16 bit RISC CPU with 16 registers. The digitally controlled oscillator (DCO) has a wake up time of 6 micro second to shift from low power modes to active mode. Current drain for the modes is given in table II.

It has five low power modes to extend battery life in portable biomedical applications. Low power modes are among the most important features, enabling the microcontroller to meet the current budget. Low power modes LMP0 turned off CPU and leave everything else functional. Modes LPM1 and LPM2 add various clocking functions to the list of disabled functions. LPM3 is the most used low power mode leaving only a low frequency clock oscillator running and any peripheral that uses that clock. LPM3 is often called the real time clock mode because it allows a timer to operate for low power 327658 Hz clock source consuming less than 1 μ A and periodically wake the system for activity. Finally LPM4 turns off all clocks on the device thus turning off any peripheral that used clocks automatically. LPM4 current consumption is only 0.1 μ A. MSP 430F1611 processor has special features like 1.1 μ A standby current, Low supply range (1.8 to 3.6 V), ultra low power consumption, five power saving modes, wakeup time from standby to active mode is less than 6 μ sec, 12 bit A/D converter with internal reference, sample and hold and auto scan feature, supply voltage supervisor, 48KB+256B flash memory and 10 KB RAM, comparator [11, 15].

TABLE II.
POWER DOWN MODES OF MSP 430 SERIES

Power Down Modes	Description	Current consumption	
		VCC= 3V	VCC= 2V
AM	All clocks are active	340 μA	225μA
LMP0	CPU , MCLK are disabled, SMCLK and ACLK are active	70 μA	μA 65
LPM2	CPU, MCLK, SMCLK, DCO osc. are disabled. DC generator remains enabled, ACLK is active	17μA	11μA
LPM3	CPU,MCLK,SMCLK , DCO osc. are disabled. DC generator disabled, ACLK is active	2 μA	1 μA
LPM4	CPU and all clocks are disabled	0.1 μA	0.1μA

V. SOFTWARE RELATED CURRENT /ENERGY MEASUREMENT METHODOLOGY[2,3,4]

There are two basic components such as pure base cost and interinstruction cost, necessary for the software related energy estimation. Pure base current cost is defined as instantaneous current drawn by the processor during repeated execution of the instruction.

Let P = {I₁, I₂, I₃-----, I_n}
 I₁.A₁ μA, C₁ cycles
 I₂.A₂ μA, C₂ cycles
 I₃.A₃ μA, C₃ cycles
 I_n.A_n μA, C_n cycles

(i) Average pure base current cost is given as

$$I_{av} = \frac{A_1 \times C_1 + A_2 \times C_2 + A_3 \times C_3 + \dots + A_n \times C_n}{C_1 + C_2 + C_3 + \dots + C_n} \quad (1)$$

$$Battery\ life = \frac{Battery\ rating\ in\ AmpHour}{Average\ current} \quad (2)$$

Pure base energy cost of each instruction is given as

$$E_i = V \times N \times I_{inst} \times T \quad (3)$$

Average pure base energy cost is given as

$$E_{av} = V \times N_T \times I_{av} \times T \quad (4)$$

$$\sum E_i = E_{av} \quad (5)$$

where,

- P----Program
- I₁, I₂, I₃,-----I_n ----Instructions
- A₁, A₂, A₃,----A_n----Pure base current cost values
- C₁, C₂, C₃,----C_n ----Cycles to execute each Instruction
- V-Core Voltage (2.21V)

- N-Number of Clock Cycles
- N_T-Total number of cycles to execute program
- I_{inst}- Pure current base cost for each instruction
- T- Clock period (125 nanosec.)

(ii) When sequences of instructions are executed, certain inter instruction effect exists which are not reflected in the pure base cost. Instantaneous current measured for such sequence execution is called as interinstruction cost. Difference between pure base cost and inter instruction cost is termed as circuit state overhead. Energy E_i consumed during the execution of instruction is modeled in [3] as

$$E_i = b_i + \sum a_{i,j} \times N_{i,j} \quad (6)$$

The overall energy consumed for running a program of n instructions can be estimated as

$$PE = \sum_1^n E_i + \sum O_{i,i+1} + \sum \epsilon \quad (7)$$

Here separately interinstruction cost is considered and added in overall base cost to calculate total energy for program execution but as mentioned in Tiwari's paper [2] interinstruction cost includes circuit state overhead.

Neglecting a_{i,j} , N_{i,j} and ε, interinstruction cost would be

$$E_i^* = E_i + O_h \quad (8)$$

Hence

$$E_{avoh} = V \times N_T \times I_{avoh} \times T \quad (9)$$

$$E_{oh}^* = E_{avoh} - E_{av} \quad (10)$$

$$I_{oh}^* = I_{avoh} - I_{av} \quad (11)$$

where,

- b_i- is pure base energy cost of i instruction
- a_{i,j}- coefficient
- N_{i,j} - number of ones of j energy sensitive factor of the i instruction respectively.
- O_{i,j}- is the interinstruction cost of the instructions i and j
- ε -is the cost of pipeline stall.
- oh- circuit state overhead.
- E_{avoh},-Average energy cost
- I_{avoh}-Average interinstruction current cost.
- E_{oh}*-circuit state overhead with respect to Energy
- I_{oh}*- circuit state overhead with respect to current

For example:

Expected base current cost calculated for the sequence given in table III, using individual base costs from (1) is given as

$$I_{av} = \frac{325.3 \times 04 + 334.2 \times 04 + 385.4 \times 02 + 385.6 \times 04}{04 + 04 + 02 + 04} = 353.7$$

TABLE III.
INSTRUCTIONS AND PARAMETERS

Instructions	Base current cost (μA)	Base Energy cost (nJ)	No. of cycles	Inter instruction current cost (μA)
mov.w TBCCR1,&TBCCR2	325.3	0.359	04	362.9
add.w R8,&TBCCR2	334.2	0.369	04	
bic.w #BIT2,&TBCCTL2	385.4	0.212	02	
bis.b #BIT0,&P6SEL	385.6	0.426	04	
	I _{av} = 353.7	ΣE _i = 1.366	ΣN = 14	I _{avoh} = 362.9

E_i, E_{av}, E_{avoh}, E_{oh*}, and I_{oh*} are calculated using (3), (4), (9), (10) and (11) respectively.

E_{av}=1.36 nJ

E_{avoh}=1.40 nJ

E_{oh*}= 0.04 nJ

I_{oh*} = 9.2 μA

% E_{oh*} change with respect to E_{av} = 2.94

% I_{oh*} change with respect to I_{av} = 2.60

Actual instantaneous current measured (inter instruction cost) when processor executes this sequence repeatedly is 362.9 μA, giving circuit state overhead of 9.2 μA. This cost is always greater than base cost and circuit state overhead is the effect of switching that occurs during instruction transaction. Instruction level current measurement scheme discussed in [2, 4] is used to measure the processor current consumption. Measurement set up is as shown in figure 3. To measure pure current base cost, test instruction is executed in infinite loop and downloaded with the help of emulator in MSP430F1611 processor. Voltage waveform across precision resistor is observed on DSO i.e. figures 5 and 6 give value of voltages for Push R11 and bis.b # BIT 1, & P2OUT instructions respectively. Base current cost through precision resistor is then calculated. Same method is used to measure interinstruction current cost.

To calculate base cost, instruction set is

```
L1 Test Instruction
    jmp L1
end
```

To calculate interinstruction cost, instruction set is

```
L1 Test Instruction Sequence
    jmp L1
end
```

Cycles needed for execution of instruction /instruction sequence are observed, while debugging with IAR workbench. MSP430 series has 27 basic instructions and base cost /interinstruction cost of each instruction can be measured. MSP430F1611 needs 2.21Volts core voltage and has clock period of 125 nanosec. Accordingly Current/Energy components have been calculated.

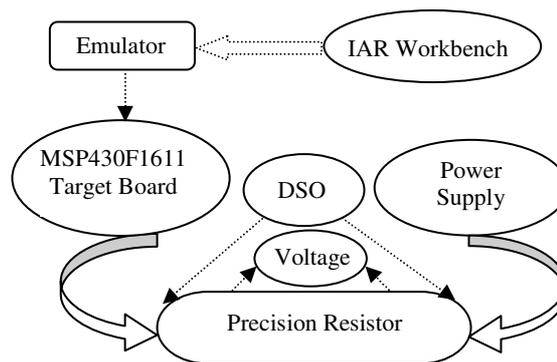


Figure 3. Set up for instantaneous current measurement.

VI. STRATEGY IMPLEMENTATION

In this research work software functionalities like basic pacing rate, refractory period and pulse width with VOO mode as explained in section II, has been realized using MSP430F1611 target board, as shown in figure 4 and IAR workbench. Programmable pacemaker parameters to generate a pulse to stimulate the heart are mentioned in the program. Mode selection switch is connected in between pin 16 & 64. Output of external comparator is connected to pin number 20 (port 2.0). To provide basic pacing and refractory period pulse, pin number 38 (port 4.2) and pin number 39 (port 4.3), respectively are configured.

In VOO mode, irrespective of the heart signal, pacemaker generates a pacing pulse. In this, comparator switches to OFF state and no synchronizing signal is applied to the port 2.0. When another mode like VVI is selected, comparator switches ON and in the absence of heart signal, pacemaker operates in VOO mode. Basic Pace interval, Ventricular refractory period, pulse width interrupt needs timer. There are two timers, Timer A and Timer B in MSP430. Timer B is used to count intervals and generate interrupts accordingly. In this paper Basic Pace, Pulse width and Refractory interrupts are used to pace heart in abnormal heart situation. These interrupts are mostly operated by hardware. Timer B interrupts uses TBCCR1, TBCCR2, and TBCCR3 registers for basic pacing, Pulse width, and refractory pulses. Timer counts the programmed parameters and generates interrupts to apply stimulus to the heart. Flow chart is given in figure 7. Digital Storage Oscilloscope is used to observe waveforms of software functionalities. Advanced version of schemes given in [2,3,4] has been used to measure base and interinstruction current cost. With reference to these costs, software related energy consumption has been derived.

VII. AVERAGE CURRENT DISTRIBUTION

Out of various power down modes, LMP3 Mode which has 2 μA standby current is used in this application. As shown in figure 8, if 1 mA activity occurs for 1 msec. average current will be 3 μA [12]. Same strategy is implemented in this paper to investigate average current for each pacemaker parameter program and to estimate battery longevity.



Figure 4. MSP 430F1611 Target Board.

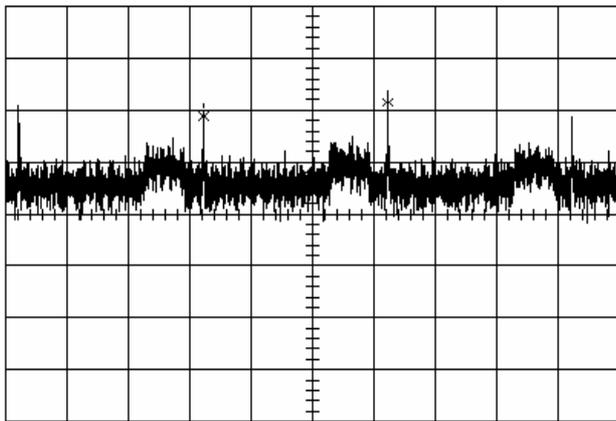


Figure 5. Voltage waveform for Push R11 across precision resistor.

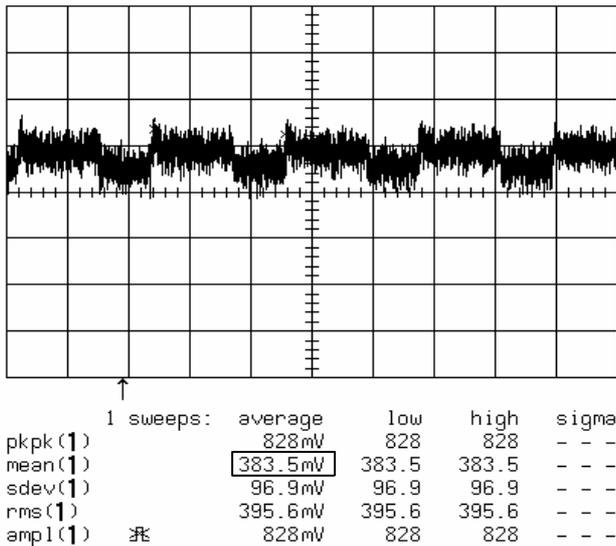


Figure 6. Voltage waveform for bis.b# BIT1, &P2OUT across precision resistor.

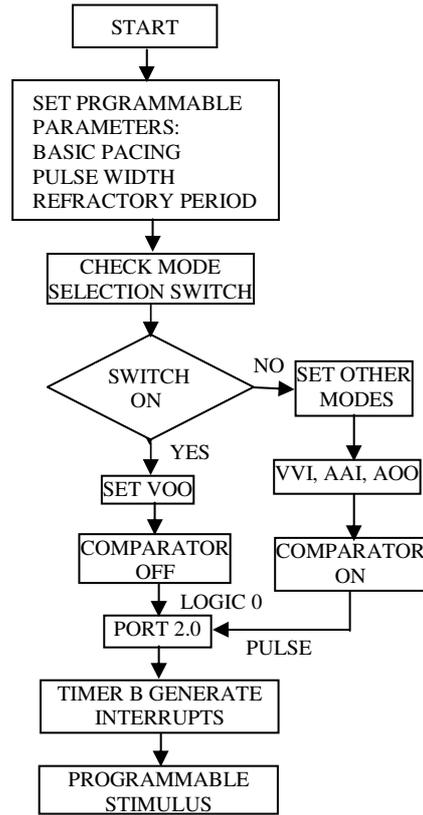


Figure 7. Flow chart.

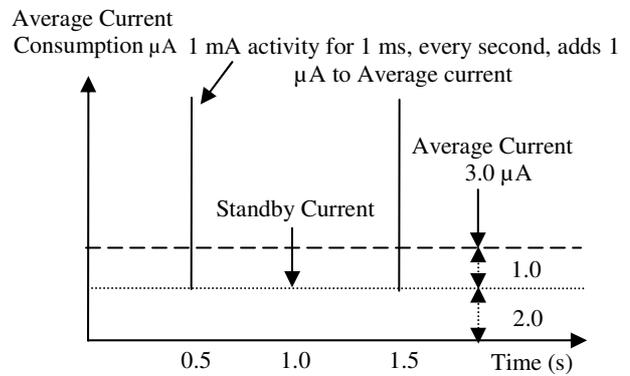


Figure 8. Average current distribution in MSP.

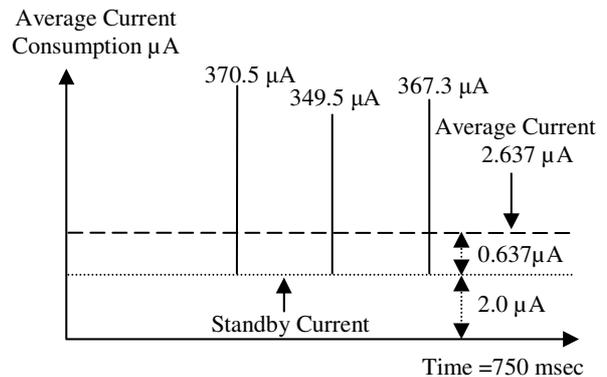


Figure 9. Average current distribution considering interinstruction cost.

For the basic pacing rate of 80 bpm, the time interval is $60000/80\text{bpm} = 750$ msec. For basic pacing, pulse width and refractory period as shown in table IV, V, VI, interinstruction current cost is 370.5 μA , 349.5 μA , 367.3 μA respectively to generate a pulse of 0.445 msec. to stimulate heart. The average current will be 2.212 μA i.e. 2 μA is LPM3 mode standby current and 0.212 μA is the current addition in every 750 msec. For pulse width and refractory period of 0.207 μA , 0.218 μA current is added in every 750 msec. interval. Hence, average current consumption is 2.637 μA which is shown in figure 9. Considering pure base current cost of each instruction, average base current cost would be 2.626 μA , as shown in table VII.

VIII.EXPERIMENTAL RESULTS

Control word is written to set pacemaker parameters like Basic pacing rate = 80 bpm, Pulse width = 0.445 msec. Refractory period = 245 msec. Codes shown in tables IV, V, VI for these parameters in VOO mode are tested using IAR workbench and MSP430F1611 target board. Base current/energy cost of each instruction, interinstruction cost and other values are calculated as explained in section V.

Waveforms in figures 10, 11, 12 gives programmable basic pacing, pulse width and refractory period of 752 msec., 400 μsec . and 248 msec. respectively with negligible precision error. Measured and estimated numerical values of pacemaker parameters have been given in table VII. Investigated distributed current checks battery longevity. For these functionalities in VOO mode, considering base /interinstruction cost, battery life will be 36 years approximately. It provides margin for hardware and other functionalities in various pacemaker modes, to have desired battery life for 12 to 15 years. Change in pure cost and interinstruction cost (current/Energy) varies from 2.0 to 3.0 %.

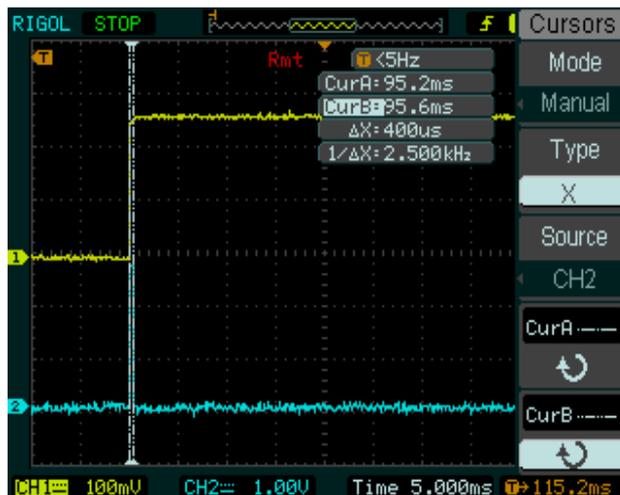


Figure 11. Pulse width (400 μsec .)

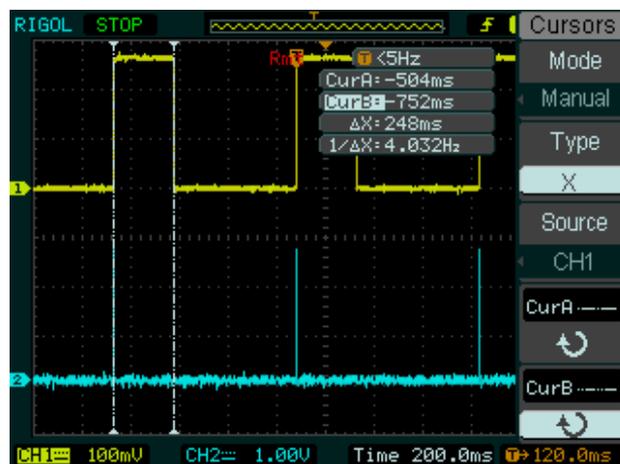


Figure 12. Refractory period (248 msec.).

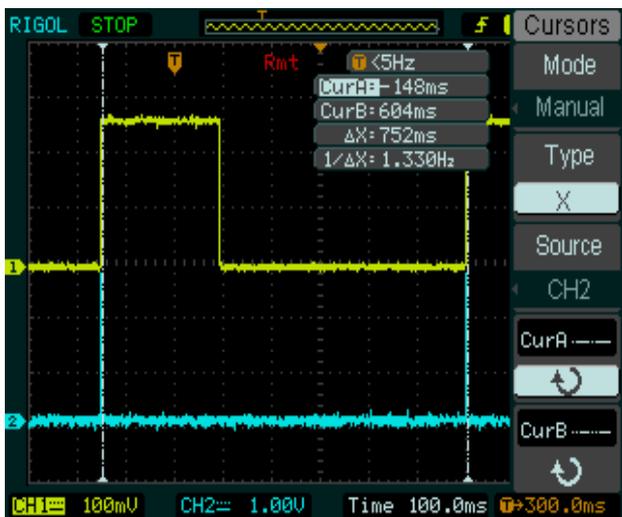


Figure 10. Basic pacing (752 msec.).

TABLE IV.
INSTRUCTIONS AND PARAMETERS FOR BASIC PACING

Instructions (Register TBCCR1)	Base current cost μA	Base Energy cost nJ	No. of cycles	Inter instruction current cost μA
push R11	318.1	0.263	03	370.5
push R12	318.1	0.263	03	
bit.w #BITB, R4	341.9	0.184	02	
Jnz Basic_Pacing	339.0	0.187	02	
add.w R7,&TBCCR1	334.2	0.369	04	
bis.b #BIT4,&P1IE	383.5	0.529	05	
bic.b #BIT0,&P2IE	385.8	0.426	04	
bic.b #BIT1,&P2OUT	385.1	0.425	04	
bis.w BIT2,&TBCCTL2	385.5	0.423	04	
bis.w BIT2,&TBCCTL3	385.5	0.423	04	
bis.b #BIT1,&P5OUT	383.6	0.423	04	
pop R12	320.5	0.177	02	
pop R11	320.6	0.177	02	
	$I_{av} = 360.3$	$\sum E_i = 4.27$	$\sum N = 43$	

TABLE V.
INSTRUCTIONS AND PARAMETERS FOR PULSE WIDTH

Instructions (Register TBCCR2)	Base current cost μA	Base Energy cost nJ	No. of cycles	Inter instruction current cost μA
mov.w.&TBCCR1,&TBCCR2	325.3	0.359	04	349.5
add.w R8,&TBCCR2	334.2	0.369	04	
bic.w#BIT2,&TBCCCTL2	385.5	0.212	02	
	$I_{av} = 340.1$	$\sum E_i = 0.94$	$\sum N = 10$	$I_{avoh} = 349.5$

TABLE VI
INSTRUCTIONS AND PARAMETERS FOR REFRACTORY PULSE

Instructions (Register TBCCR3)	Base current cost μA	Base Energy cost nJ	No. of cycles	Inter instruction current cost μA	
mov.w &TBCCR2,&TBCCR3	325.3	0.359	04	367.3	
add.w R9,&TBCCR3	334.2	0.369	04		
bic.w#BIT2,&TBCCCTL3	385.4	0.523	05		
bit.b #BIT4,&P1IN	335.1	0.185	02		
jnz Comp	339.0	0.374	04		
bis.b #BIT1,&P2OUT	383.5	0.211	02		
bit.w #BITB,R4	335.2	0.185	02		
jnz Comp	339.2	0.184	02		
bis.b #BIT0,&P2IE	383.6	0.423	04		
bic.b #BIT0,&P2IFG	385.5	0.425	04		
	$I_{av} = 357.06$	$\sum E_i = 3.238$	$\sum N = 33$		$I_{avoh} = 367.3$

TABLE VII.
CURRENT/ENERGY COMPONENTS FOR VARIOUS FUNCTIONALITIES

Parameters	Basic Pacing	Pulse width	Refractory Period
I_{av}	360.3 μA	340.1 μA	357.06 μA
I_{avoh}	370.5 μA	349.5 μA	367.3 μA
E_{av}	4.27 nJ	0.94 nJ	3.25 nJ
E_{avoh}	4.40 nJ	0.96 nJ	3.34 nJ
E_{oh}^*	0.13 nJ	0.02 nJ	0.09 nJ
I_{oh}^*	10.2 μA	9.4 μA	10.24 μA
% E_{oh}^* change	3.0	2.1	2.86
% I_{oh}^* change	2.83	2.76	2.86
Distributed Current (Pure base cost).	0.213	0.201	0.212
	Average distributed current with processor standby current=2.626 μA		
Distributed current (interinstruction cost).	0.212	0.207	0.218
	Average distributed current with processor standby current = 2.637 μA		
Battery longevity for battery of 0.85 Ah ratings.	(i)Considering average distributed current for pure base cost = 36 years approx. (ii)Considering average distributed current for interinstruction cost = 36 years approx.		

IX.CONCLUSION

Low power consumption is a crucial constraint in implantable pacemaker. Hence instantaneous Current consumption by hardware and software must be minutely considered. Cost and time to market of modern VLSI based implantable pacemaker design will be more. In this paper some functionalities, like basic pacing, pulse width and refractory period in VOO mode, has been realized using MSP430F1611 ultralow power processor. These functionalities include set of instructions. Appropriate

measuring and modeling scheme has been implemented to measure instantaneous current and to derive energy consumption. Especially, values for software related current/energy components i.e. base and interinstruction cost were presented, analyzed and discussed. The work is aimed towards development of low power processor based implantable pacemaker and estimation of software related current/ energy consumption.

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