Analysis of Block Oxide Height Variations for a 40nm Gate Length bFDSOI-FET

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***Abstract*—In this paper, a novel device architecture called the fully depleted silicon-on-insulator field-effect transistor with block oxide (bFDSOI-FET) is proposed to investigate the influence of block oxide height (H_{BO}) on the electrical characteristics. According to the two-dimensional (2-D) simulation results, the characteristics of the proposed structure are similar to those of the ultra-thin (UT) SOI-FET, due to the presence of block oxide enclosed silicon body. Moreover, although the high H_{BO} associated with the thick silicon body results in somewhat poor device performance because of increased charge sharing from the source/drain (S/D), the self-heating effects (SHEs) for the bFDSOI-FET can be reduced.**

***Index Terms*—FDSOI, block oxide, charge sharing, self-heating.**

I. Introduction

In order to achieve the improved performance and enhanced speed, the dimensions of the conventional complementary metal-oxide semiconductor field-effect transistor (CMOS-FET) are decreased. Furthermore, the semiconductor industry has already entered into a new era called the nanotechnology for achieving the customers' needs. To further improve the electrical characteristics of the device, some structures or techniques have been developed [1-2]. Particularly, planar fully depleted silicon-on-insulator (FDSOI) MOSFET with ultra-thin (UT) body structure is considered as a potential contender for CMOS scaling [3]. However, several undesirable effects are associated with this structure, such as the high source/drain (S/D) parasitic resistance [4] and the thermal instability [5]. The former is due to the ultra-thin S/D regions that act as a limit of the doping depth. As a result, the drain current of the device decreases. The latter affects the long-term reliability of nanoscale transistor because the generated heat in the channel region cannot efficiently be dissipated via the buried oxide (BOX) layer thus resulting in the mobility reduction. Besides, in the case of a UTSOI MOSFET, the short-channel effects (SCEs) need uniform ultra-thin body (UTB) thickness to be diminished significantly. Hence, the UTSOI MOSFET will finally become a super-thin body (STB) structure and totally lose its advantages owing to that the threshold voltage of the device is very sensitive to the fluctuations of the body thickness.

In this work, we have analyzed the influence of block oxide height variations for a newly-designed 40 nm gate length FDSOI MOSFET with block oxide namely bFDSOI-FET. With this structure, the sidewall spacer process is utilized to form the block spacers on the sidewalls of the silicon body which can work as a current and an electric field blocking layer between the silicon body and the S/D regions. This gives the rise that alleviate the SCEs and the junction leakage current. Moreover, the body of the bFDSOI-FET consists of silicon and poly-Si that will function as a buffer layer to ameliorate the self-heating effects (SHEs) when compared with the UTSOI structure.

II. Process Simulation

In this study, we have used ISE-TCAD process simulator, FLOOPS, to design and verify the process of the new device. Fig. 1 shows the main process flow of the bFDSOI. To fabricate the bFDSOI-FET, a commercial SIMOX-SOI wafer was used as a starting wafer, which has a buried oxide (BOX) thickness of 50 nm and an initial silicon-film thickness of 50 nm. First, the silicon body was defined by the electron beam (EB) lithography techniques. A 60 nm thick oxide layer was deposited by chemical vapor deposition (CVD) and etched back to form the block spacers on the sidewalls of the silicon body. Then, a 10 nm thick polysilicon (poly-Si) film was deposited with a low-pressure CVD (LPCVD) process before the body implantation (BF_2, $1.15\text{x}10^{13}/\text{cm}^2$, 2 keV). It is believed that the deposited poly-Si could be recrystallized after the body implantation because of the presence of the silicon (body) seed crystal. After the active region formation, the gate oxide was thermally grown and the poly-Si was deposited to serve as a gate structure. The oxide layer was then deposited and etched back to form the sidewall spacers. Next, the second oxide layer was deposited as a screen layer. The S/D regions were implanted by arsenic ions ($5.1\text{x}10^{14}/\text{cm}^2$, 8 keV). The implanted wafer was then inserted into a spike annealing tool. The following steps would end up by a conventional SOI process.

In this paper, the height of the block oxide (H_{BO}) equals to the original silicon body thickness (T_{Si}) will be

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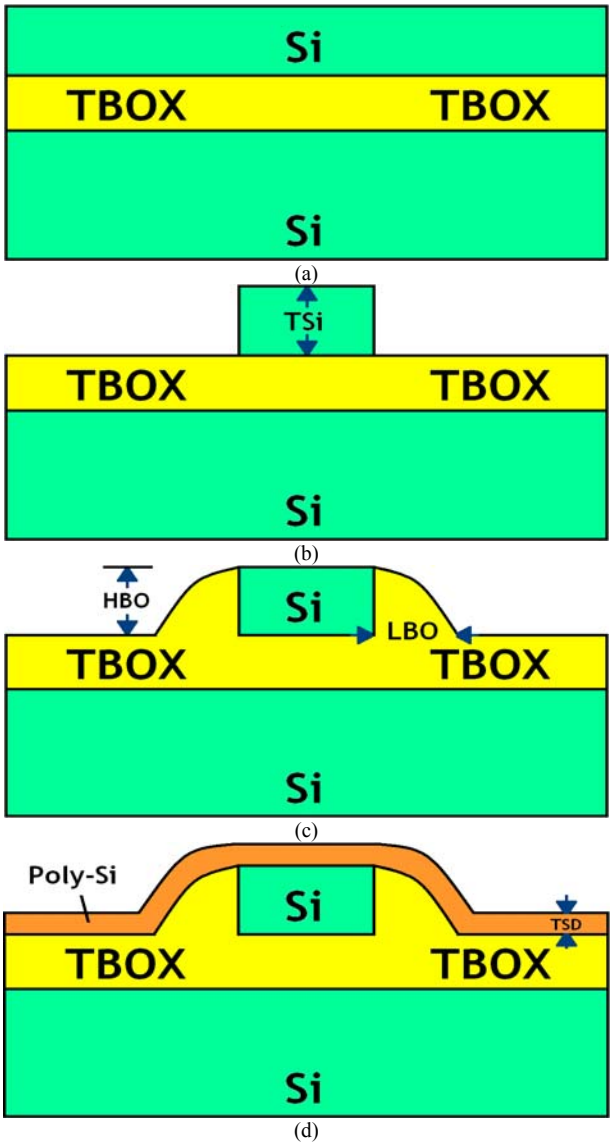


Figure 1. Simplified schematic of bFDSOI fabrication process. (a) The SOI wafer having a BOX layer of 50 nm and a thin active region of 50 nm. (b) Electron beam (EB) lithography techniques used to pattern the silicon body. (c) Spacer oxide formation. (d) Polysilicon (poly-Si) deposited as the surface of the wafer.

investigated with a wide-range from 5 nm to 52 nm when compared with the 10 nm thick body UTSOI-FET. In Fig. 2, it shows the 2-D view of the bFD and UT SOI devices implemented in the FLOOPS-ISE. The scanning electron microscope (SEM) top view of the bFDSOI-FET fabricated is also presented as shown in Fig. 3.

The device parameters are listed in the following. For the bFDSOI-FET, the S/D thickness ($T_{S/D}$) is taken as 10 nm. For the UTSOI-FET, the $T_{S/D}$ is also taken as 10 nm which is equal to the $T_{S/D}$ of the bFDSOI-FET. Other parameters for both devices are T_{BOX} (back-gate oxide thickness) = 50 nm, T_{GOX} (front-gate oxide thickness) = 1.4 nm, and L_G (gate length) = 40 nm, respectively.

III. Results and Discussion

In this study, we applied the ISE-DESSIS [8] to simulate the current characteristics for both devices. Then, for comparison, we can extract some electrical

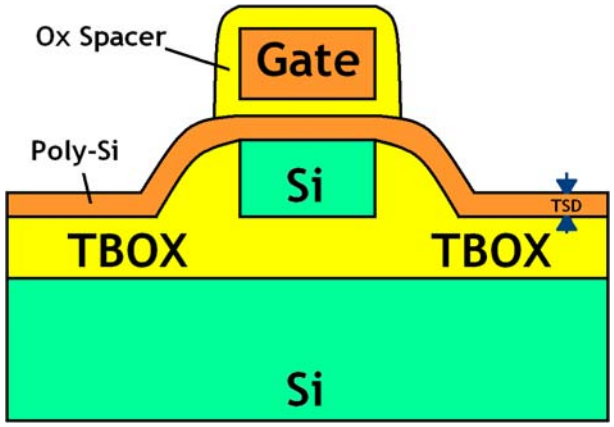


Figure 2. A 2-D view of the FDSOI with block oxide (bFDSOI).

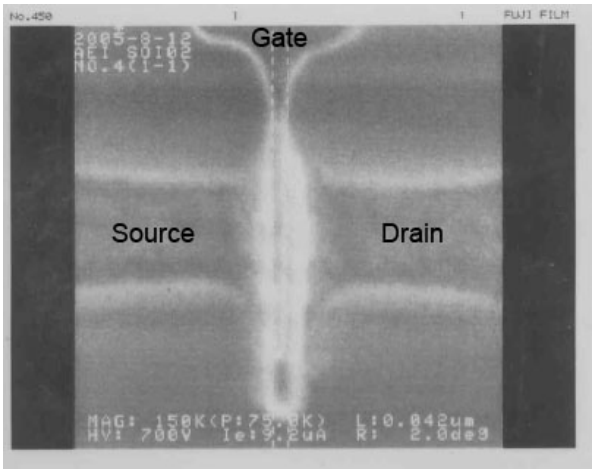


Figure 3. SEM top view of bFDSOI-FET [6-7].

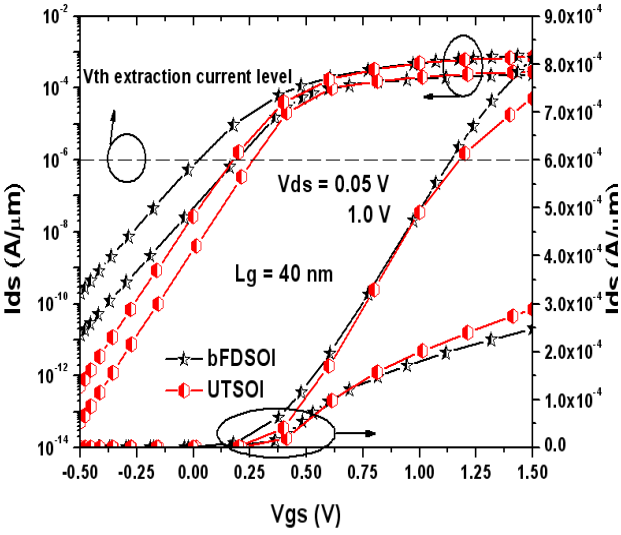
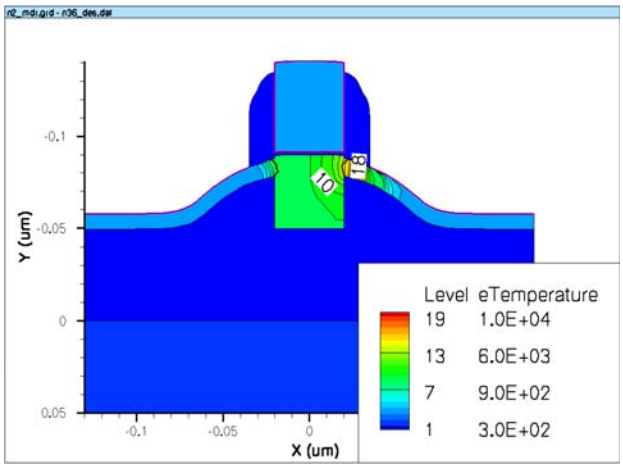
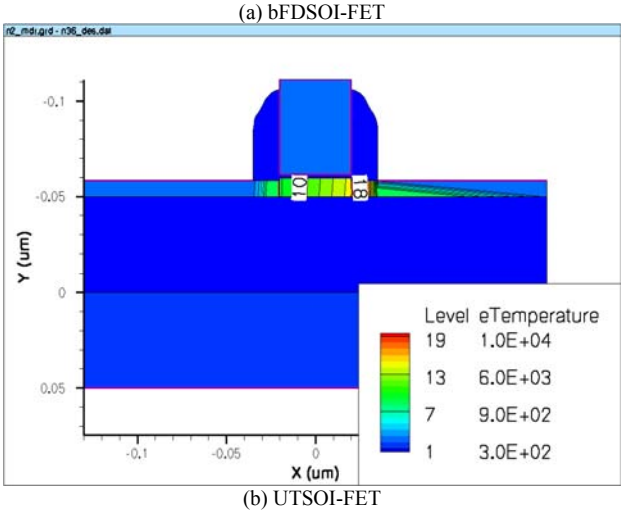


Figure 4. I_{DS}-V_{GS} characteristics o f the bFDSOI and UTBSOI structures for V_{DS} = 0.05 V and 1.0 V. The device parameters for the bFDSOI transistor are T_{Si} = H_{BO} = 30 nm and T_{SD} = 10 nm. The device parameters for the UTBSOI transistor are T_{Si} = T_{SD} = 10 nm. Other parameters are T_{BOX} = 50 nm, T_{GOX} = 1.4 nm, and L_G = 40 nm.

parameters from them. For example, the linear threshold voltage ($V_{TH, lin}$) at drain-to-source voltage (V_{DS}) = 0.05 V



(a) bFDSOI-FET



(b) UTSOI-FET

Figure 5. Electron temperature contours in the bFDSOI and UTBSOI MOSFETs with V_{GT} = 1.0 V. The device parameters for the bFDSOI transistor are T_{Si} = H_{BO} = 30 nm and T_{SD} = 10 nm. The device parameters for the UTBSOI transistor are T_{Si} = T_{SD} = 10 nm. Other parameters are T_{BOX} = 50 nm, T_{GOX} = 1.4 nm, and L_G = 40 nm.

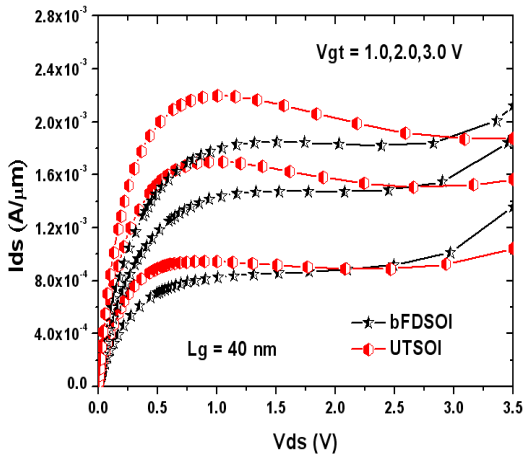
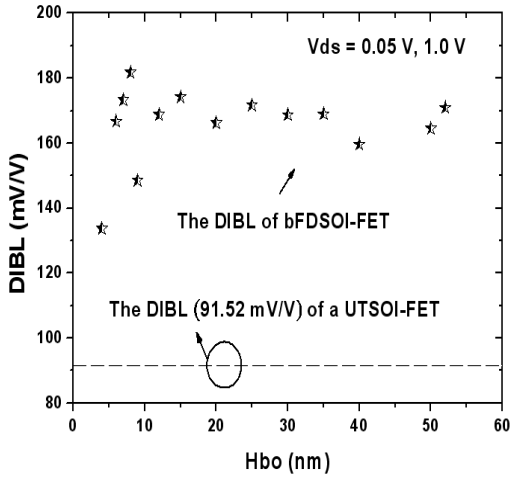
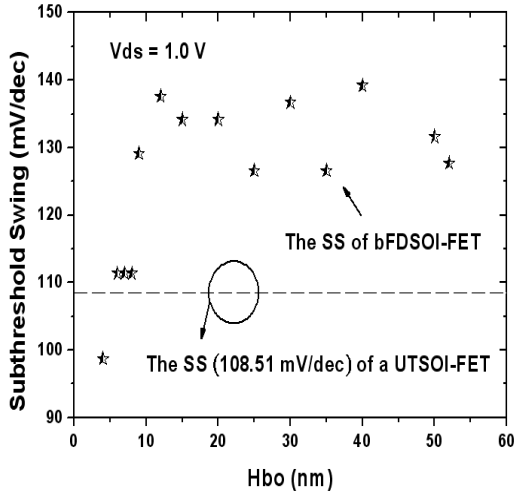


Figure 6. I_{DS}-V_{DS} characteristics of the bFDSOI and the UTBSOI structures for V_{GT} = 1.0 V, 2.0 V, and 3.0 V. The device parameters for the bFDSOI transistor are T_{Si} = H_{BO} = 30 nm and T_{SD} = 10 nm. The device parameters for the UTBSOI transistor are T_{Si} = T_{SD} = 10 nm. Other parameters are T_{BOX} = 50 nm, T_{GOX} = 1.4 nm, and L_G = 40 nm.

and the saturation threshold voltage ($V_{TH, sat}$) at V_{DS} = 1.0 V are extracted at drain current (I_{DS}) = 1 μA/μm. The drain-induced barrier lowering (DIBL) is defined as the difference between the $V_{TH, lin}$ and the $V_{TH, sat}$. In addition, the drain on-state current (I_{ON}) is the I_{DS} at V_{DS} = 1.0 V and gate-to-source voltage (V_{GS}) = 1.0 V; the drain off-state current (I_{OFF}) is the I_{DS} at V_{DS} = 1.0 V and V_{GS} = 0.0 V. The subthreshold swing is measured in the $dV_{GS}/d(\log I_{DS})$. The physical models used in SOI are also used for the bFDSOI and UTSOI MOSFETs. Owing to the presence of the silicon body being as the seeds for the bFDSOI, the deposited poly-Si served as the active layer can be recrystallized after the body-implantation processes. Thus, the models used for poly-Si are not used in this work for the bFDSOI. Furthermore, all of the device simulations are implemented by DESSIS-ISE [8].



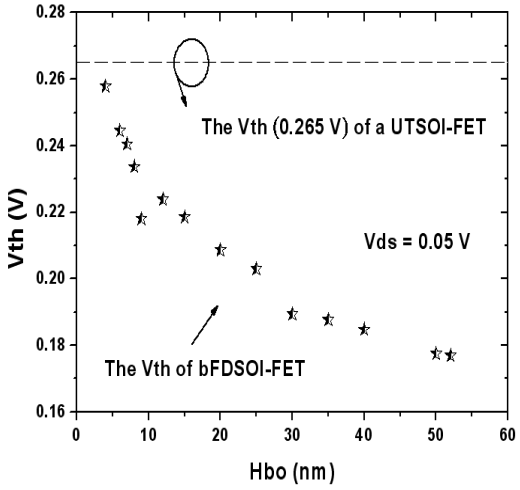
(a) DIBL versus H_{BO}



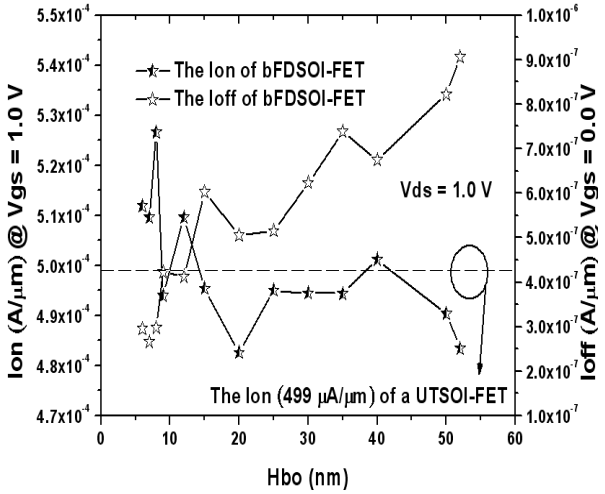
(b) Subthreshold swing versus H_{BO}

Figure 7. (a) DIBL and (b) Subthreshold swing versus H_{BO}. The device parameters for the bFDSOI transistor are T_{Si} = H_{BO} and T_{SD} = 10 nm. The device parameters for the UTBSOI transistor are T_{Si} = T_{SD} = 10 nm. Other parameters are T_{BOX} = 50 nm, T_{GOX} = 1.4 nm, and L_G = 40 nm.

In Fig. 4, the subthreshold I-V curves of the bFDSOI structure are compared with the UTSOI-FET. In the bFDSOI-FET, both DIBL and subthreshold swing are worse than the UTSOI mainly owing to its thick body thickness, T_{Si}. Although the short-channel characteristics of the bFDSOI are poor, exploiting the block oxide enclosed silicon body can eliminate a requirement of uniform ultra-thin body structure. That is the process constraint, the big issue in an UTSOI-FET can be totally relaxed. Moreover, both of these slightly worse results are acceptable because the total body thickness of the bFDSOI-FET is 40 nm thick, compared to that 10 nm of the UTSOI-FET. These results illustrate that the use of block oxide to the thick-silicon-body FDSOI structure can achieve acceptable results in either DIBL or subthreshold swing. In other words, the charge sharing from S/D and the short channel effects can be effectively suppressed in the bFDSOI-FET.



(a) V_{TH} versus H_{BO}



(b) I_{ON}, I_{OFF} versus H_{BO}

Figure 8. (a) V_{TH} and (b) I_{ON}, I_{OFF} versus H_{BO}. The device parameters for the bFDSOI transistor are $T_{Si} = H_{BO}$ and $T_{SD} = 10$ nm. The device parameters for the UTBSOI transistor are $T_{Si} = T_{SD} = 10$ nm. Other parameters are $T_{BOX} = 50$ nm, $T_{GOX} = 1.4$ nm, and $L_G = 40$ nm.

Fig. 5 shows the electron temperature contours. It is worth nothing that the bFDSOI structure exhibits better electron temperature profiles when compared with the UTSOI structure. In the case of a bFDSOI, the thick silicon body not only maintains the electrical characteristics like those of the UTSOI, but it also improves the thermal stability. However, in the UTBSOI, the electron temperature profiles are seriously affected by its structural limit – ultra-thin body, which leads to a negative differential conductance observed in the output I-V curves as shown in Fig. 6. Finally, the UTSOI structure will limit its high-performance applications mainly due to the degraded device reliability. But, the thick silicon body of the bFDSOI-FET can help to ameliorate the thermal effects so that the effects of self-heating-induced negative output conductance can be eliminated at the $V_{GT} = 1.0$ V case. Even if the V_{GT} increases to a level of 3.0 V, only a little negative output conductance is observed in the bFDSOI-FET. While on the contrary, the UTSOI has serious thermal limitations because of SHEs.

When the H_{BO} of bFDSOI is getting smaller, the short-channel characteristics, such as DIBL and subthreshold swing, will become better, as observed in Fig. 7. This is due to the decreased charge sharing encroached from the S/D regions thereby resulting in the improved controllability of gate voltage to the drain current. It should be noted that the current trend is towards the ultra-thin body thickness, T_{Si} (= H_{BO}), for obtaining both the reduced DIBL and the ideal subthreshold swing in a bFDSOI. It is also worth noting that owing to the presence of a fixed T_{Si} (= T_{SD} = 10 nm), the UTSOI structure exhibits a straight line of the DIBL and subthreshold swing as shown in Fig. 7. In addition, it can be observed that the UTSOI has slightly better short-channel behavior than the bFDSOI.

Fig. 8 shows the V_{TH} and I_{ON}, I_{OFF} characteristics versus H_{BO} for both the configurations. From the figures, as the H_{BO} increases, the V_{TH} of bFDSOI-FET decreases, resulting in a higher leakage current. Therefore, the degraded subthreshold swing of bFDSOI-FET also results in lower drain on-state current. Compared with the bFDSOI-FET, the UTSOI-FET deserves a higher V_{TH}, which leads to attain a lower leakage current (< $1x10^7$ A/um). In addition, the improved subthreshold swing of UTSOI also helps to get a higher drain on-state current. Owing to the non-optimized V_{TH}, the value of drain off-state current is not acceptable. But, this problem can be improved by using metal-gate stack and high-K technology [9]. Thus, the threshold voltage can be optimized.

It is interesting to note that this study shows different results at same investigation ($T_{Si} = H_{BO}$) compared with the previous one [10]. We believe that this study is reasonable because the T_{Si} of an SOI MOSFET is one of the key parameters for determining the short-channel

characteristics. The thicker T_{Si} the SOI is, the poor performance the SOI becomes. The previous study demonstrates different results are due to that too-much lower drain current (< $1x10^4$ A/um) was designed.

IV. CONCLUSION

We have investigated the effects of H_{BO} variations on a 40 nm gate length n-channel bFDSOI-FETs, which is newly-designed. Exploiting the block oxide enclosed body, the PN junction is reduced significantly resulting in less parasitic capacitance, less junction leakage current and suppressed short channel effects. Based on the 2-D simulation results, we have found that the H_{BO} is one of the important parameters of the bFDSOI-FET because the T_{Si} is equal to H_{BO}. In other words, the higher H_{BO} the bFDSOI-FET is, the higher DIBL the bFDSOI-FET becomes. Nevertheless, a requirement of a uniform ultra-thin body can be eliminated from the proposed structure for improving short-channel characteristics. Additionally, it is due to the presence of thick silicon body compared with the UTSOI, the bFDSOI shows improved thermal stability.

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