Low Power SRAM with Boost Driver Generating Pulsed Word Line Voltage for Sub-1V Operation

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Abstract—**Instability of SRAM memory cells derived from the process variation and lowered supply voltage has recently been posing significant design challenges for low power SoCs. This paper presents a boosted word line voltage scheme, where an active body-biasing controlled boost transistor generates a pulsed word line voltage by capacitive coupling only when accessed. Simulation results have shown that the proposed approach not only shortens the access time but mitigates the impact of V_{th} variation on performance even at ultra low supply voltage less than 0.5 V.**

Index Terms— **SRAM, Circuit methodology, Low power, Low voltage, PD-SOI, V_{th} variation**

I. Introduction

In recent years, lots of serious problems in accordance with aggressive technology scaling, known as "red brick wall," have been posing significant design challenges for performance improvement of LSI's. Power reduction is becoming one of the most critical design issues especially for battery-operated portable devices due to severe power constraints. In addition, since the area of on-chip SRAM memory has been continuing to grow, both the active and leakage power consumption on memory area dominates the total chip power [1]. Hence, power management in SRAM operating at low power consumption is indispensable for future system LSI designs. Therefore, we propose a circuit design methodology for low power SRAM with single supply voltage. The rest of this paper is organized as follows. First, Section II gives an overview of previous low power approaches mainly focusing on dynamic voltage control with multiple supply voltages. Next, Section III refers several issues of SRAM operating at low supply voltage. Then, we propose a boosted word line voltage scheme for single power supply SRAM employing capacitive coupling of ABC (Active Body-biasing Controlled)-SOI capacitor in Section IV. Section V provides circuit simulation results. Finally, we summarize the key results in Section VI.

II. Low Power Technique by Dynamic Voltage Control

Lowering the supply voltage (V_{DD}) has been one of the most effective approaches in order to pursue ultra low power operation since the dynamic power consumption decreases in proportion to the square of V_{DD}. The lowered supply voltage also has an advantage of reduction in the leakage power consumption derived from the sub-threshold and gate leakage current during the standby mode. A V_{DD}-hopping scheme [2] where the supply voltage is dynamically controlled according to workload of a processor is known as one of the representative low power design methodologies employing hardware-software cooperatively oriented algorithm. In addition, a DVS (Dynamic Voltage Scaling) [3] and a DVFS (Dynamic Voltage Frequency Scaling) [4], lowering a frequency and supply voltage as long as lower performance is allowed, are becoming a standard approach for reducing active power consumption when performance requirements vary. The design style of voltage scaling which is moving from coarse-grained approaches to fine-grained ones even aims at scaling the threshold voltage (V_{th}) in small steps [5].

III. Issues of SRAM Operating at Low Supply Voltage

When applying the dynamic voltage control to SRAM, the difficulty of SRAMs operating at low supply voltage comes from the degradation of access speed due to a lack of driving current. This is based on the fact that the transistor delay increases exponentially as the lowered supply voltage. The other obstacles to low voltage operation include instability of SRAM cells such as an increase in soft-error rate (SER) and reductions of static noise margin (SNM) [6]. Although the conventional approach boosting the supply voltage in memory cells improves the deteriorated SNM [7], [8], it cannot avoid the issue of exponential increase in the write/read access

time in low voltage operation. The use of 8T-SRAM [9] with a separated read-port has been discussed to enhance the stability by eliminating cell disturbs during a read access even when V_{DD} is scaled down to sub-1V. However, additional transistors unfortunately deteriorate the write access time for 8T-SRAM as lowered supply voltage. Hence, it is important to accelerate the write/read access time even in low voltage operation while maintaining the SNM.

In this paper, we propose a design methodology employing a boosted voltage scheme with a single power supply rail which can be widely applied and especially aims at 8T-SRAM for the SNM improvement. In the case of 6-transistor SRAM basic memory cells shown in Fig. 1, the access time for read and write operation mainly depends on the access transistors connecting bit lines (BL, BLB) and a cross-coupled inverter latch. Here, the access transistors consist of nMOS pass-transistors with the disadvantage of the output voltage drop at high level. Even though the drain voltage V_{drn} is expected to be $V_{drn} = V_{DD}$, the drain voltage actually rises only up to $V_{drn} = (V_{DD} - V_{th})$, which results in a lack of on-current. The issue of voltage loss is becoming more serious in accordance with lowered supply voltage since V_{th} is scaled down more moderately than V_{DD}. To avoid them, we propose a speed-up technique boosting the word line node for reduction in voltage loss based on a bootstrap scheme [10] employing an ABC-SOI for strong capacitive coupling. Our strategy includes the following two features:

i) Boosting the word line nodes quickly by a Bootstrap-type driver.

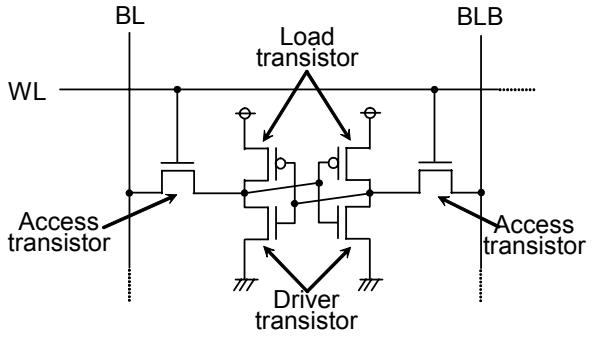


Figure 1. 6T-SRAM memory cell.

ii) Strong boosting effect by the Active Body-biasing Control.

IV. Boosted Word Line Voltage Scheme for Single Power Supply SRAM

In this section, we propose a novel design style for SRAM employing the ABC-Bootstrap scheme which boosts the word line node voltage higher than V_{DD} to accelerate the write / read speed. In SRAM memory cells, two bit lines and a cross-coupled inverter latch are connected each other through access transistors while the word line activates the access transistors. Then, the write / read operation can be performed by draining on-current at the access transistors. Thus, enhancing the current from bit lines to memory cells helps shorten the delay time in the write mode. On the other hand, in the read operation mode, two bit lines BL and BLB are first charged to V_{DD} during the precharge operation. Then, the carrier at BL or BLB are discharged to the data retention node of "Low" in memory cells right after turning on the access transistors. A sense amplifier detects the difference of bit line voltages between BL and BLB and outputs the data stored in memory cells. Hence, lowering the bit line voltage in short transition time by enhancing the on-current of access transistors is effective for fast read operation. Therefore, boosting the gate voltage of access transistors is expected to shorten both the write and read access time.

A. ABC-SOI Capacitor

The Active Body-biasing Controlled (ABC)-SOI capacitor utilizing the PD-SOI process with the Hybrid Trench Isolation technology [11], [12] provides a strong capacitive coupling.

The strength of capacitive coupling is dependent upon a transistor size and gate voltage. For an nMOS FET with the gate length L = 0.18 μm and the gate width W = 10, 20 μm, we have calculated the capacitance between the gate and source/drain when the gate voltage changes from 0.3 V to 0.6 V. According to the SPICE simulation results shown in Fig. 2, the capacitance is proportional to the gate voltage since the capacitances in the channel of transistor increases in accordance with the gate voltage while the overlap capacitance becomes a constant value.

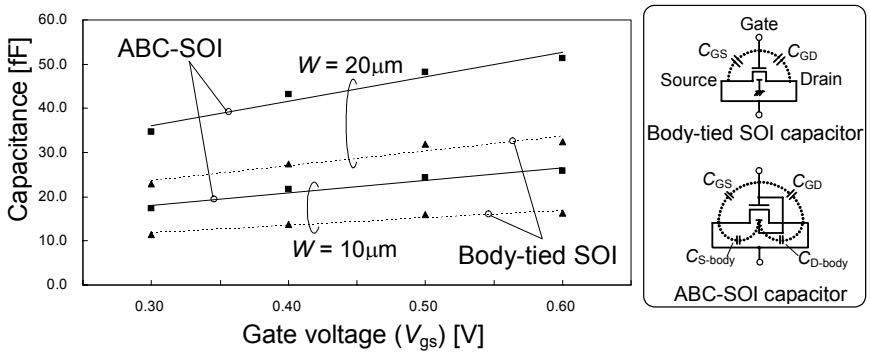


Figure 2. Simulated MOS capacitance in boost transistor.

In addition, even though the capacitance in body-tied SOI mainly derives from the overlap capacitances between the gate and source/drain (C_{GS}, C_{GD}), the ABC-SOI capacitor, where the body is directly connected to the gate, provides the enhanced capacitance owing to the additional capacitances ($C_{S\text{-}body}$, $C_{D\text{-}body}$) between the source/drain and body. We take the advantage of strong capacitive coupling by the ABC-SOI.

B. Word Line Driver with ABC-SOI Capacitor

The proposed approach, boosted voltage scheme with the ABC-SOI capacitor, is shown in Fig. 3. We describe the features in detail.

First, during a low to high transition of the word line as shown in Fig. 4, the pMOS in the transmission gate helps finish the pull-up transition perfectly since the pMOS keeps on-state until the input signal WL via delay circuits cuts off the pMOS. Thus, the word line voltage V_{WL} is allowed to rise up to V_{DD} immediately. Second, the capacitance C_{BS} of the boost transistor starts to boost V_{WL} higher than V_{DD} as illustrated in Fig. 4 as soon as the pMOS turns off in the driver circuit with the single boost transistor shown in Fig. 3 (a). In addition, the driver with double stages of the boost transistor, shown in Fig. 3 (b), divides the capacitance C_{BS} into two boost transistors. The second stage of the boost transistor driven by the second delay circuit prevents V_{WL} from dropping when V_{WL} is boosted by the first stage of the boost transistor. In Fig. 3 (a), V_{WL} actually drops a little due to the current passing through the pMOS before turning off perfectly. Hence, employing double stages of the boost transistor enhances the capacitive coupling and ensures boosting V_{WL} higher than V_{DD}. The higher gate voltage results in an enhanced on-current of the access transistors.

C. Boosting Effect of Word Line Voltage

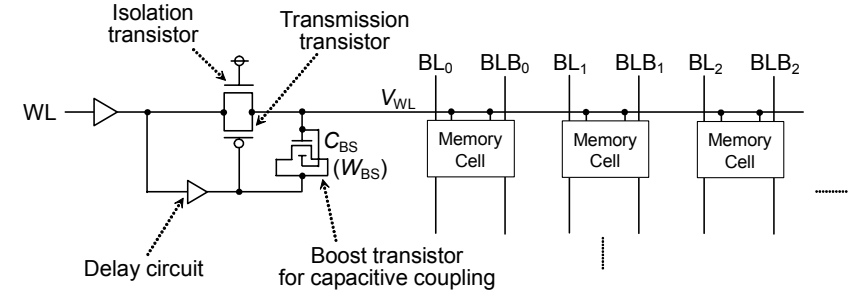
Here, we discuss the boosting effect of the word line voltage. In fact, the capacitive coupling by the boost transistors dominates the maximum voltage level of word line, which boosts the word line voltage V_{WL} up to

$$V_{WL} = \left(1 + \frac{C_{BS}}{C_{total}}\right) V_{DD}, \quad (1)$$

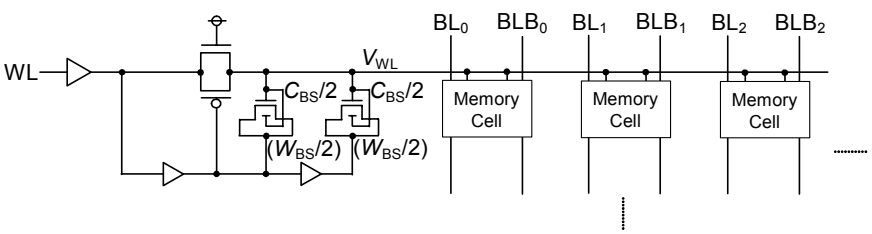
where C_{BS} denotes the capacitance between the gate and source / drain of boost transistors, and C_{total} denotes the total capacitance including the wire capacitance of word line C_{WL}. Thus, the strength of capacitive coupling depends upon the ratio of C_{BS} to C_{total}. Here, C_{BS} is proportional to the gate width W_{BS} of the boost transistor as already shown in Fig. 2, and C_{WL} is in proportion to the length of word line, thus, the number of memory cells in each row. Then, Fig. 5 shows the ratio of word line voltage V_{WL} to V_{DD} (V_{WL} / V_{DD}) calculated by Equation (1) when the number of memory cells arrayed in each row varies. For simplicity, we treat C_{total} as $C_{total} = C_{BS} + C_{WL}$. The capacitance of boost transistors for capacitive coupling has been set to C_{BS} = 14 fF, 28 fF when the gate width W_{BS} = 10 μm, 20 μm, respectively. We have assumed that the wire capacitance of word line per memory cell is C_{WL} = 1.25 fF/cell. In Fig. 5, in the case memory cells of 32-bit are arrayed in each row, for example, the ratio V_{WL} / V_{DD} = 1.4 when the gate width W_{BS} = 20 μm, while the maximum voltage level of word line results in tendency to decrease as the number of bit increases. Hence, an adequate ratio of V_{WL} / V_{DD} ensures low voltage operation and shortens the access time.

V. Simulation Results

We have performed SPICE simulation with the BSIM3-based SOI transistor model for 0.18 μm PD-SOI process in order to evaluate our Enhanced ABC-Bootstrap scheme. The threshold voltages with MOSFETs are set to $V_{th\text{-}n}$ = 0.34 V, $V_{th\text{-}p}$ = – 0.42 V for memory cells and $V_{th\text{-}n}$ = 0.24 V, $V_{th\text{-}p}$ = – 0.34 V for address decoders or



(a) Driver with single boost transistor



(b) Driver with double stages of boost transistors

Figure 3. Boosted word line voltage scheme with ABC-SOI capacitor.

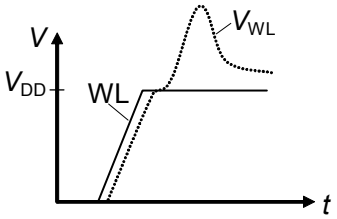


Figure 4. Concept of boosted word line voltage.

peripheral circuits. We define these threshold voltages $V_{th\text{-}n}$, $V_{th\text{-}p}$ as the gate voltage which makes the drain current I_{ds} per width W to be 1 μA/μm when the drain voltage V_{ds} = 1.8 V. We have calculated them by SPICE simulation. We extracted the resistance and capacitance of the wire after designing the 8Kb memory array. We have decided that the gate width W = 5 μm for the word line driver, isolation transistor, and transmission transistor and W = 10 μm for the boost transistor, respectively. With respect to the whole layout area of 8 Kb memory array, for example, our boosted voltage scheme has an area overhead of 10 % due to the additional area of word line drivers.

We have evaluated the access time to a memory cell in the write and read operation mode for the supply voltages from 0.35 V to 0.6 V. A variation in the threshold voltage is also discussed. The Enhanced ABC-Bootstrap scheme has been compared to the SRAM configuration with the normal word line driver without the Bootstrap scheme.

A. Write Operation Speed

First, we discuss the write operation speed to memory cells based on the results shown in Fig. 6. We also consider the waveforms of the clock CK, word line WL, and data-retention node in Fig. 7 (a). Here, we define the write time as the period from the point of V_{DD} / 2 in CK during a low to high transition to that in the date retention node of memory cells during the data inverting operation. We have achieved 10%, 38 % of improvements in the write time at V_{DD} = 0.5 V, V_{DD} = 0.35 V, respectively. This results show our approach is more effective to the lower supply voltage. The data retention node of memory cell in our approach completes charging quickly owing to the boosted word line voltage as shown in Fig. 7 (a). Here, the ratio of word line voltage V_{WL} to V_{DD} in Fig. 7 becomes V_{WL} / V_{DD} = 1.25 that approximates the value calculated by Equation (1) as shown in Fig. 5 even though V_{WL} is lowered a little due to discharging through the transmission transistor.

According to Fig. 6, the write time increases exponentially since lowering supply voltage degrades driving power of transistors in the both approaches. Then, we have confirmed that the proposed approach requires the longer write time than the conventional one if the supply voltage is over 0.5 V. On the other hand, the relation became inverted when it comes to ultra low supply voltage less than 0.5 V. We consider the results from the point of the dependence on the delay time of t_{WL}

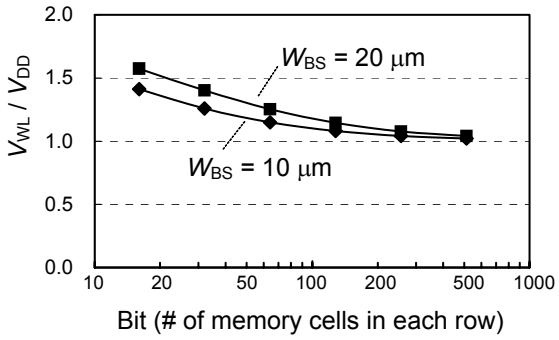


Figure 5. Ratio of boosted word line voltage to power supply (V_{WL} / V_{DD}) depending on the number of bit cells.

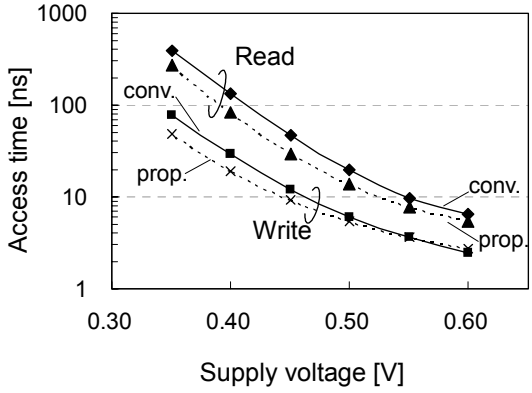
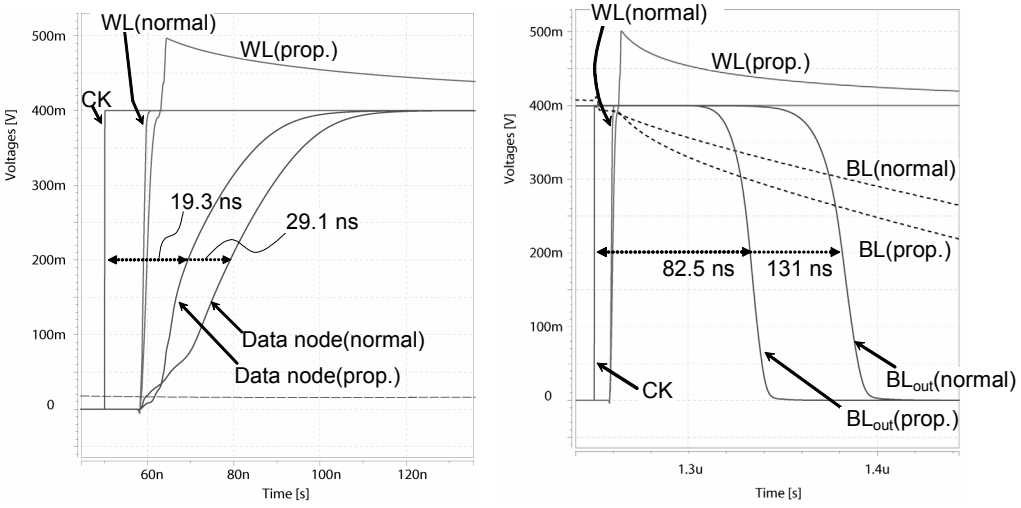


Figure 6. SRAM access time.



(a) Write mode (b) Read mode

Figure 7. Waveforms.

and t_{access}, where t_{WL} represents the propagation delay of the word line and t_{access} means the gate delay of the access transistor. At the higher voltage operation, both t_{WL} and t_{access} have almost the same order of delay time owing to enough driving power. Hence, the proposed approach shows the longer write time since the additional input load to the word line causes the extra delay of t_{WL}. On the other hand, t_{access} becomes much longer than t_{WL} due to the higher threshold voltage of the access transistors as the supply voltage goes down, which conceals the extra delay of t_{WL}. Thus, the gate voltage higher than V_{DD} shortens the write time in the proposed approach at low supply voltage less than 0.5 V.

B. Read Operation Speed

Next, we show the simulation results with the read time in Fig. 6. We also consider the waveforms of the clock CK, word line WL, bit line BL, and output data signal from sense amplifier BL_{out} as illustrated in Fig. 7 (b). Here, we define the read time as the period from the point of V_{DD} / 2 in CK during a low to high transition to that in BL_{out}, while the sense amplifier detects the difference of bit line voltages between BL and BLB and outputs the data stored in memory cells. According to Fig. 8, the lower supply voltage increases the read time exponentially. Our proposed approach shortens the read time by 15 % at V_{DD} = 0.5 V and 30 % at V_{DD} = 0.35 V compared to the conventional approach. Since the read time is dependent on the discharging speed of bit line, enhancing the on-current of access transistors by boosted the word line voltage higher than V_{DD} achieves quick discharging operation of bit line as shown in Fig. 7 (b). As a result, the bit line voltage in the proposed approach drops in shorter transition time than the conventional one. Therefore, the output data in the proposed approach appears first by the quick response of sense amplifier.

C. V_{th} Dependance of Access Time

Here, we analyze the dependence of access time derived from a variation in the threshold voltage (V_{th}). In the low voltage operation such as 0.5 V-V_{DD}, transistors come into the linear or sub-threshold operation since the supply voltage almost reaches the threshold voltage. Especially for SRAM memory cells, their performance is directly dependent upon the on current of access transistors which varies due to V_{th} variation. Then, we have evaluated the difference in access time derived from V_{th} variation between the conventional approach and proposed one through HSPICE simulation.

First, best and worst cases have been analyzed. We have decided that the mean of the threshold voltage V_{th0} = 346 mV and assume a variation of ± 10% as the best and worst cases. Fig. 8 shows the access time of memory cell when V_{th0} changes from $0.9V_{th0}$ to $1.1V_{th0}$. With respect to the difference in access time between the fastest and slowest cases, the maximum difference results in 2.54x in the read mode for the conventional approach. On the other hand, the difference is suppressed down to 1.99x in our approach since the enhanced on current of access transistors by the boosted gate voltage avoids a larger impact of V_{th} variation. The difference in write time is likewise reduced from 1.53x to 1.21x. Therefore, a smaller variation in the access time due to V_{th} variation is expected in our approach.

Next, the impact of V_{th} variation on the distribution of write time has also been analyzed based on the 1k-point Monte Carlo simulations. Here, the global and local V_{th} variations of 3σ are reflected to the histograms shown in Fig. 9, where the standard deviation σ of V_{th} is assumed

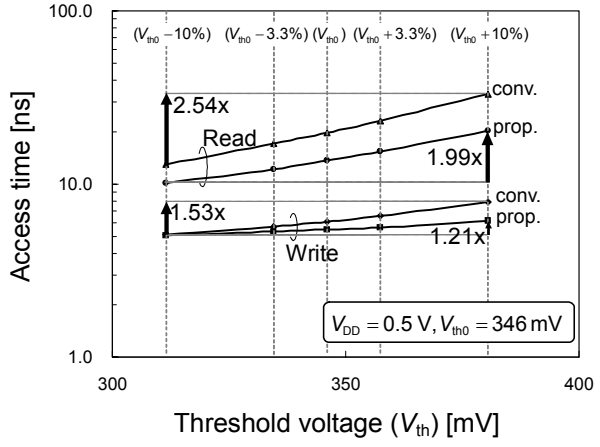


Figure 8. V_{th} dependence of access time based on best and worst analyses.

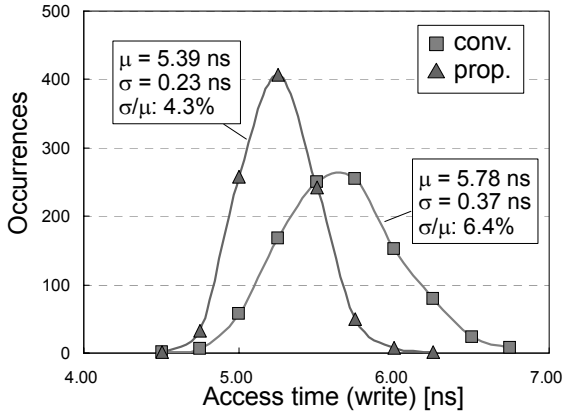


Figure 9. Impact of global and local V_{th} variation based on Monte Carlo simulation.

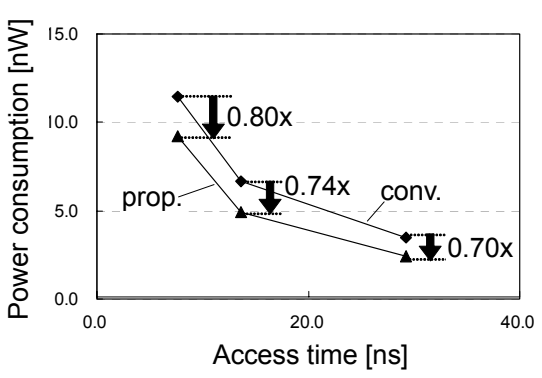


Figure 10. Power saving effect.

that 3 σ corresponds to 10 % of V_{th}. According to the mean (μ) and standard deviation (σ) of access time summarized in Fig. 9, the proposed approach reduces the μ and σ by 7 % and 38 %, respectively. As a result, the coefficient of variation (CV: σ/μ) is improved from 6.4 % to 4.3 %.

D. Power Saving Effect

Using the lower supply voltage is allowed in our approach while maintaining the same operational speed as the conventional approach. Here, we discuss the power saving effect based on Fig. 10. We compare the power consumption in both approaches after adjusting the proper supply voltage in order to achieve the same operational speed. According to Fig. 10, the Enhanced ABC-Bootstrap scheme achieves the power reduction of 30 % in the best case in spite of the additional word line driver in the proposed scheme. It means that the power consumed by a charging and discharging the bit lines dominates the whole power of SRAM, the additional power in the proposed word line driver can be less significant. Therefore, our SOI-SRAM with the Enhanced ABC-Bootstrap scheme ensures LSIs' operation even at ultra low supply voltage.

VI. CONCLUSION

In this paper, in order for SRAM to pursue low voltage operation, we have proposed a low power design methodology employing a boost driver which generates a pulsed word line voltage for single power supply and sub-1V operation. In the proposed word line driver circuit, the use of an active body-biasing controlled boost transistor enhances the impact of capacitive coupling, and the boosted the word line voltage increases the on-current of access transistor. Simulation results have shown the proposed approach not only shortens the access time but mitigates the impact of global and local V_{th} variation on performance even at ultra low supply voltage less than 0.5V.

REFERENCES

[1] International Technology Roadmap for Semiconductor 2005.

[2] H. Kawaguchi, G. Zhang, S. Lee, Y. Shin, and T. Sakurai, "A controller LSI for realizing V_{DD}-hopping scheme with off-the-shelf processors and its application to MPEG4," *IEICE Trans. on Electronics*, vol. E85-C, no. 2, pp. 263-271, Feb. 2002.

[3] B. H. Calhoun and A. Chandrakasan, Ultra-dynamic voltage scaling using sub-threshold operation and local voltage dithering in 90nm CMOS, in *IEEE ISSCC Dig. Tech. Papers*, pp. 300-301, Feb. 2005.

[4] T. Fujiyoshi, S. Shiratake, S. Nomura, T. Nishikawa, Y. Kitasho, H. Arakida, Y. Okuda, Y. Tsuboi, M. Hamada, H. Hara, T. Fujita, F. Hatori, T. Shimazawa, K. Yahagi, H. Takeda, M. Murakata, F. Minami, N. Kawabe, T. Kitahara, K. Seta, M. Takahashi, Y. Oowaki, and T. Furuyama, "An H.264/MPEG-4 Audio/Visual Codec LSI with Modulewise Dynamic Voltage/Frequency Scaling," in *IEEE ISSCC Dig. Tech. Papers*, pp. 132-133, Feb. 2005.

[5] M. Nomura, Y. Ikenaga, K. Takeda, Y. Nakazawa, Y. Aimoto, and Y. Hagihara, "Monitoring Scheme for Minimizing Power Consumption by Means of Supply and Threshold Voltage Control in Active and Standby Modes," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 308-311, June 2005.

[6] E. Seevinck, F. J. List, and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE J. Solid-State Circuits*, vol. sc-22, pp. 748-754, Oct. 1987.

[7] K. Itoh, A. R. Fridi, A. Bellaou, and M. I. Elmasry, "A deep sub-V, single power-supply SRAM cell with multi-V_T, boosted storage node and dynamic load," in *Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 132-133, June 1996.

[8] M. Yamaoka, K. Osada, and K. Ishibashi, "0.4-V Logic Library Friendly SRAM Array Using Rectangular-Diffusion Cell and Delta-Array-Voltage Scheme," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 170-173, June 2002.

[9] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Geuarini, and W. Haensch, "Stable SRAM Cell Design for the 32nm Node and Beyond," in *Symp. VLSI Technology Dig. Tech. Papers*, pp. 128-129, June 2005.

[10] M. Iijima, M. Kitamura, K. Hamada, K. Fukuoka, M. Numa, A. Tada, and S. Maegawa, "Active Body-Biasing Control Technique for Bootstrap Pass-Transistor Logic on PD-SOI at 0.5V-VDD," in *Proc. IEEE International SOI Conference*, pp. 50-51, Oct. 2005.

[11] Y. Hirano, T. Matsumoto, S. Maeda, T. Iwamatsu, T. Kunikiyo, K. Nii, K. Yamamoto, Y. Yamaguchi, T. Ipposhi, S. Maegawa, and M. Inuishi, "Impact of 0.10 μm SOI CMOS with Body-Tied Hybrid Trench Isolation Structure to Break Through the Scaling Crisis of Silicon Technology," in *IEDM Tech. Dig.*, pp. 467-470, Dec. 2000.

[12] Y. Hirano, T. Ipposhi, H. Dang, T. Matsumoto, T. Iwamatsu, K. Nii, Y. Tsukamoto, H. Kato, S. Maegawa, K. Arimoto, Y. Inoue, M. Inuishi, and Y. Ohji, "Impact of Actively Body-bias Controlled (ABC) SOI SRAM by using Direct Body Contact Technology for Low-Voltage Application," in *IEDM Tech. Dig.*, pp. 2.4.1-2.4.4, Dec. 2003.

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