Modeling of Leakage Current Mechanisms in Nanoscale DG MOSFET and its Application to Low Power SRAM Design

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Abstract— **Double-Gate (DG) MOSFET has emerged as one of the most promising devices for logic and memory circuit design in sub 10nm regime. In this paper, we investigate the gate-to-channel leakage, EDT, BTBT and sub-threshold leakage for DG MOSFET. Simulations are performed using 2D Poisson-Schrödinger simulator with tight-binding Green's function approach. Then we analyze the effect of parameter variation to optimize low leakage SRAM cell using DG devices. The DG device/circuit co-design successfully demonstrates the benefit of using metal gate intrinsic body DG devices which significantly reduces BTBT and EDT in SRAM architecture.**

Index Terms—**Double-Gate, BTBT, sub-threshold, leakage, SRAM.**

I. Introduction

For over three decades there has been a quadrupling of transistor density and a doubling of electrical performance every 2-3 years. With the anticipation of unconstitutionality of Moore's law within a decade, researchers have embarked in exploring alternative technologies by harnessing the properties of channel materials, dielectric materials and gate work-function engineering that would provide us with high performance with nanoscale devices. Due to excellent control over short channel effects (SCEs), and better "ON" current, DG MOSFETs become one of the promising candidates in sub-10 nm regime. However, continuous downscaling of device dimensions as well as aggressive scaling of oxide thickness,according to ITRS [1], lead to exponential increase of leakage components, which leads to a large stand-by power dissipation. Thus leakage power management becomes indispensable in high-end microprocessors for cost effective solution.

The major components of leakage in DG MOSFETs are: gate-to-channel leakage, edge direct tunneling (EDT), band-to-band tunneling (BTBT) and subthreshold leakage. The near mid gap metal gate (MG) DG devices become an obvious choice for low power design because their intrinsic body doping and metal gate, eliminates random dopant fluctuation and poly depletion respectively [2]. In symmetric DG (SymDG) devices, threshold voltage is controlled by super "Halo" body doping while in asymmetric DG (AsymDG) devices, work-function difference between front and back gates controls threshold voltage fluctuation. The device structure and body doping have strong impact on the device leakage.

In this paper, we will analyze the effect of variation of device parameters on leakages. High performance and low leakage architecture is the ultimate goal for semiconductor industry. We will also discuss the leakage components in 6-T SRAM cell using DG device. The total leakage in SRAM cell is substantially reduced using MGDG devices. Due to intrinsic body, random dopant fluctuation is absent in MGDG and sensitivity of the cell leakage w.r.t. effective channel length and thickness variation is reduced. We will also discuss the effect of parameter variation in the DG SRAM cell due to independent gate control and advantage of using independent gate control in DG devices in circuit design in sub-10 nm regime.

II. Device Simulation

In a generalized multidimensional system consisting of N macroscopic contact reservoirs R_s, s=1,….,N, a central quantum system QS, and N connecting leads, we normally choose one of the reservoirs to be grounded with chemical potential μ_g to be zero and we require that the (N-1) biases with respect to the grounded reservoir are known [3]. Here DG device is considered as of having four terminals having biases in three terminals. The combination of the thin silicon film thickness and the narrow channel widths will give rise to the aforementioned quantization in both transverse and longitudinal direction leading to an inseparable solution space. Here we have separated the channel quantization and quantum treatment along confinement direction to quantify the probability distribution across the two directions to be independent.

Thus we have taken the initiatives towards independency of the transverse mode from the longitudinal mode distribution. Thus, first we remove the degeneracy between the electron bands in the primed and un-primed valleys around the $\vec{k}=0$ point and an increased separation between adjacent subbands takes place away from the $\vec{k}=0$ point. Thus band-to-band coupling is ignored and transport effectively reduces to ballistic transport.

For each bound energy states of interest (considering 1st four subbands of 1st valley and 1st two subbands of 2nd valley) the quantum transport can be modeled as [4]

$$\begin{pmatrix} E-\varepsilon_1-\sum_L^r & -t_{12} & 0 & 0\cdots & \cdots 0 \\ -\tilde{t}_{12} & E-\varepsilon_2 & -t_{23} & 0\cdots & \cdots 0 \\ 0 & -\tilde{t}_{23} & E-\varepsilon_3 & -t_{34} & \cdots 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & -\tilde{t}_{n-1,n} & E-\varepsilon_n-\sum_R^r \end{pmatrix} \begin{pmatrix} \psi_1^L \\ \psi_2^L \\ \vdots \\ \vdots \\ \psi_n^L \end{pmatrix} = \begin{pmatrix} -2it_{dl}\sin(k_l a)u_l \\ 0 \\ 0 \\ \vdots \\ 0 \end{pmatrix} \tag{1}$$

Now, we can solve the Eigen energies of the Hamiltonian. The proposed algorithm computes a self-consistent solution for the quantum transport equation and Poisson's equation

$$\nabla^2 V(x,y) = -\frac{q}{\varepsilon_{Si}}\left[N_a(x,y)+n(x,y)\right]$$

Here ,q be the charge of the electron, $n(x,y)$ be the 2-D electron concentration in the active device space , $N_a(x,y)$ is the space dependent charge concentration due to an external doping. The longitudinal direction is denoted on the X-axis and transverse direction on the Y-axis. Two dimensional simulation results show that in the insulator gap region, potential can be approximated as a linear function of y.

The electron density evaluated from the wave function can be related to the quasi-Fermi level by

$$n(x,y) = \sum_n \sum_m \int_{-\infty}^{+\infty} \frac{1}{\pi}\sqrt{\frac{m_n^*}{2\hbar^2}}\frac{1}{\sqrt{E-E_{(n,m)}}} f_d(E)\left|\psi_{(n,m)}(x,y)\right|^2 dE$$

where $f_d(E)$ is the Fermi-Dirac function , (n,m) signifies the nth subband of the m th valley.

The coupled Poisson and Schrödinger equations are solved by means of a Newton-Raphson method.The iterations are continued until the norm-two of the difference between the electrostatic potentials obtained at the end of two successive cycles is smaller than a desired minimum value.

Considering the SCEs and quantum-mechanical (QM) effects, threshold voltage of DG device is given by [2],[5]-[8]

$$V_{th} = \frac{E_g}{2q} + \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) + \frac{1}{1+r}\left[\Phi_{Gfs} + r\Phi_{Gbs} - \left(\frac{Q_b}{C_{ox}} - r\frac{Q_b}{2C_{Si}}\right)\right] - \left(\frac{\varepsilon_{Si}t_{Si}t_{oxf}V_{ds}}{\varepsilon_{ox}\alpha L^2} + \frac{\varepsilon_{Si}t_{Si}t_{oxf}E_g}{2\varepsilon_{ox}\gamma L^2}\right) + \frac{E_g}{2q} - \frac{kT}{q}\ln\left(\frac{Q_{inv}^{QM}(E_F=0)}{n_i t_{Si}}\right) \tag{2}$$

where, $r = 3t_{oxf}/(3t_{oxb}+t_{Si})$ is the sensitivity of V_{th} to the back gate bias. For ultra thin t_{Si} due to volume inversion back gate bias can impact the V_{th} even after inversion at all regions of operation [9]. Here, Φ_{Gfs} and Φ_{Gbs} are the work-function differences for the front and back gates, and α and γ are the structure and doping dependent empirical factors.

III. Modeling Leakage Components in DG MOSFET

In DG devices, energy ($E_{(i,j)}$) associated with the j[th] subband of the i[th] valley (both longitudinal and transverse) is given as [10]

$$E_{(i,j)} = \frac{j^2(2\pi\hbar)^2}{8m_i^* t_{Si}^2} + \left[\frac{3hq\varepsilon_{ox}E_{ox}}{4\varepsilon_{Si}\sqrt{2m_i^*}}\left(j+\frac{3}{4}\right)\right] \tag{3}$$

where, m_i^* is the electron effective mass and E_{ox} is the electric field in the oxide region. Since, we are dealing with devices in nanoscale regime and scattering is neglected in our analysis, the electron transport through the proposed device can be considered as ballistic transport. Due to absence of the bulk charge in metal gate devices with intrinsic body, surface electric field is negligible and electron quantization occurs mainly due to structural confinement as we neglect E_{ox} for MGDG devices. However, in Sym DG devices due to the presence of bulk charge, surface electric field below threshold is not negligible. Due to the presence of large inversion charge, the field quantization is high above threshold operation.

A. Modeling Gate Leakage Current

The different physical mechanisms for gate leakage are: conduction band electron tunneling (CBET), valence band electron tunneling (VBET), and valence band hole tunneling (VBHT). In DG devices due to strong quantum confinement, tunneling occurs from quasi-bound states (QBS) and at the interface electron Eigen function is no longer nonzero in the polysilicon/metal gate region. A close analogy between the confined electrons in varying potential and electromagnetic waves in a waveguide with varying refractive indices provides the utilization of the transverse-resonant method [11]. A close look of electron tunneling across gate-to-channel region is depicted in Fig. 1 (a). The terminal impedances $\vec{Z}$ in the transverse-resonance method can be expressed as,

$$\bar{Z}_m = \eta\frac{\bar{Z}_{m-1} - j\eta_m\tan(k_m d_m)}{\eta_m - j\bar{Z}_{m-1}\tan(k_m d_m)} \qquad \text{for } m = 2, 3, \ldots.$$

$$\bar{Z}_m = \eta\frac{\bar{Z}_{m+1} - j\eta_{m+1}\tan(k_{m+1} d_{m+1})}{\eta_{m+1} - j\bar{Z}_{m+1}\tan(k_{m+1} d_{m+1})} \qquad \text{For } m = \text{N-2, N-3,..}$$

The final Eigen function for the leaky QBS is solved by imposing the following condition

$$\vec{Z}_i + \vec{Z}_i = 0 \tag{4}$$

The tunneling current density from the i^{th} QBS is expressed as

$$J_i = \frac{Q_i}{\tau_i} \tag{5}$$

where, τ_i is the life time of the i^{th} QBS.

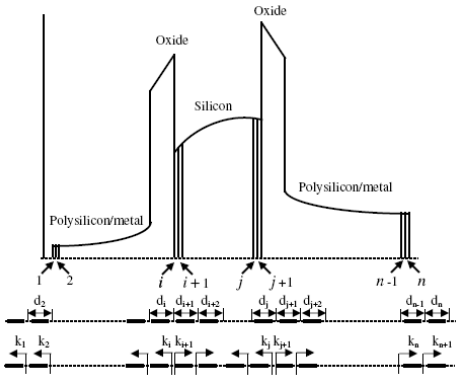

Fig. 1(a) Illustration of electron tunneling across gate-to-channel direction from transverse-resonant method.

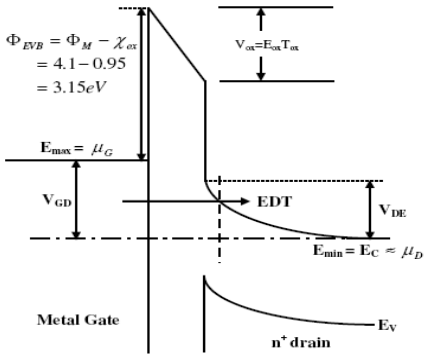

Fig. 1(b) EDT in MGDG devices [2] @IEEE.

Tunneling through source/drain extension region and gate occurs both in "*ON*" and "*OFF*" state. In the "ON" state electron tunnels from S/D region to gate, while in "OFF" state tunneling of electron occurs in opposite direction. In "OFF" state of MGDG structure, electrons from the free states below the Fermi level in metal (or, in the valence band of p^+ poly i.e. VBET) constitute EDT. Electron tunneling from the states above the metal Fermi level is negligible due to lack of electrons. The current density due to tunneling from free states can be expressed as [12]

$$J_{EDT} = \frac{4\pi q m^* kT}{h^3} \times \int_{E_{\min}}^{E_{\max}} T(E) \ln\left[\frac{1+\exp\{q(\Phi_D - V_{GD} - E_{av})/kT\}}{1+\exp\{q(\Phi_D - E_{av})/kT\}}\right]$$

$$E_{\max} = E_V(p^+ poly), \qquad E_{\min} = E_C(n^+ drain), \tag{6}$$

$$D_{WKB} = \exp\left[\frac{E_{G(ox)}\sqrt{2m_{ox}}}{4\hbar q E_{ox}}\left(2\chi\sqrt{\beta} + \sqrt{E_{G(ox)}}\sin^{-1}\chi\right)\right]$$

where, transmission probability is given by $T = D_{WKB}T_R$. Now, the probability of metal electron tunneling is less than that of CBET due to higher barrier height, which reduces EDT in MGDG compared to Sym DG. Fig. 1(b) shows EDT at "OFF" state for MGDG devices.

B. Modeling Band to Band Tunneling Current

Band-to-band tunneling across reversed p-n junction occurs from p-side valence band to n-side conduction band, becomes increasingly important with continued device scaling into nanometer regime and increasing E-fields in the channel. At positive drain bias and/or, negative bias, potential across drain-to-body region can exceed the band-gap voltage, especially at the p^+ surface causing BTBT between drain and body. Similarly, BTBT occurs also in PMOS devices especially at the n^+ surface. Since silicon is an indirect band gap semiconductor, the BTBT current involves the emission of the photons. I_{BTBT} is a function of the local electron-hole pair generation rate, given by [13]

$$G_{BTBT} = \frac{q^2 m^{0.5} E^2}{18\pi\hbar^2 E_g^{0.5}} \times \exp\left(-\frac{\pi m^{0.5} E_g^{1.5}}{2\hbar q E}\right) \tag{7}$$

where, E is the local electric field and E_g is the energy band gap. The units of G_{BTBT} are electron-hole pairs/cm^3-s. This is integrated over tunneling volume, i.e., the region where band-bending is greater than bandgap . Since the transverse band-bending is much smaller than lateral band-bending in underlapped devices, tunneling volume is calculated based on lateral band profile independently at different depths on the body. Typically in MGDG devices with intrinsic body BTBT is lower compared to Sym DG with Halo doping.

C. Modeling Subthreshold Current

Subthreshold current flows in the OFF state of the device, from the drain to the source. For a DG device it is given by[6]

$$I_{sub} = 2\frac{W}{L_{eff}} C_g \mu_0 \left(\frac{KT}{q}\right)^2 \times \exp\left(\frac{V_{gs} - V_{th}}{SKT/q}\right)\left(1 - \exp\left(-\frac{q V_{ds}}{KT}\right)\right) \tag{8}$$

where C_g is the effective gate capacitance and S is the subthreshold swing factor .

IV. Results And Discussions

Now, we will compare leakage currents in different DG devices. Due to presence of bulk charge, electric field inside oxide layer is higher in SymDG compared to MGDG devices. Moreover, due to large bending of subbands, these are at higher energy than those in MGDG devices. Hence, electrons have a higher probability of tunneling across gate oxide region and hence greater

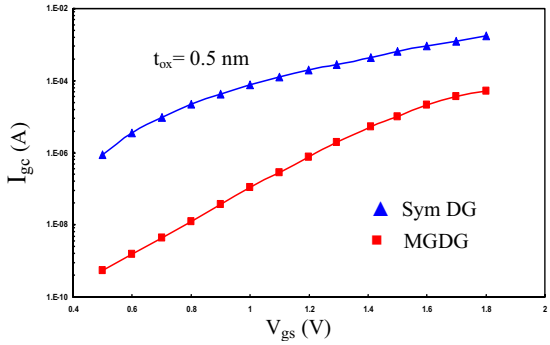

Fig.2 (a) Variation of gate-to-channel tunneling with gate voltage for SymDG and MGDG devices.

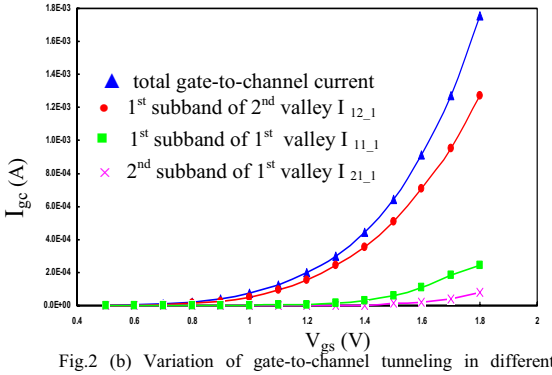

Fig.2 (b) Variation of gate-to-channel tunneling in different valleys of SymDG MOSFET.

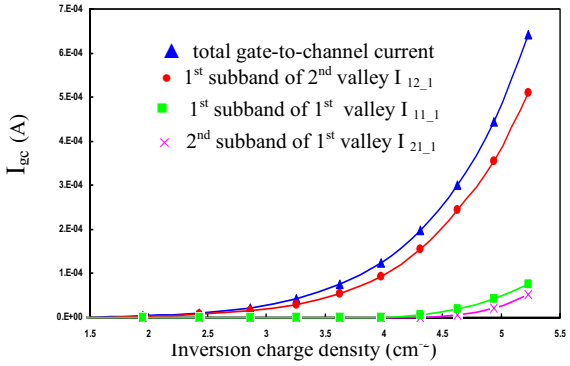

Fig.2 (c) Gate-to-channel tunneling as a function of inversion charge density

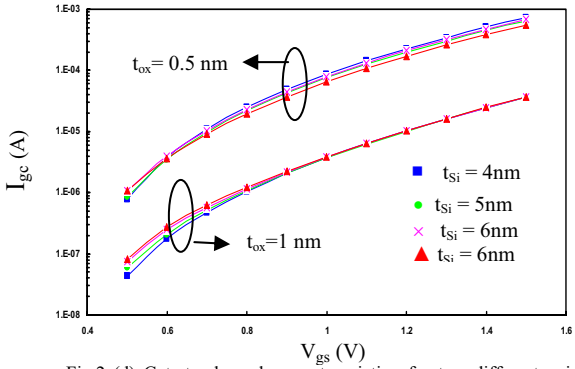

Fig.2 (d) Gate-to-channel current variation for two different oxide thicknesses. On increasing t_{ox} , gate current is reduced by considerable amount.

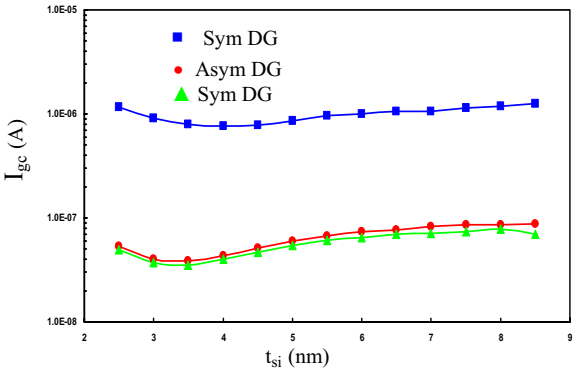

Fig.2 (e) Dependence of gate-to-channel current on body thickness for SymDG device. Below t_{Si} (~ 3nm) increases confinement of carriers towards interface.

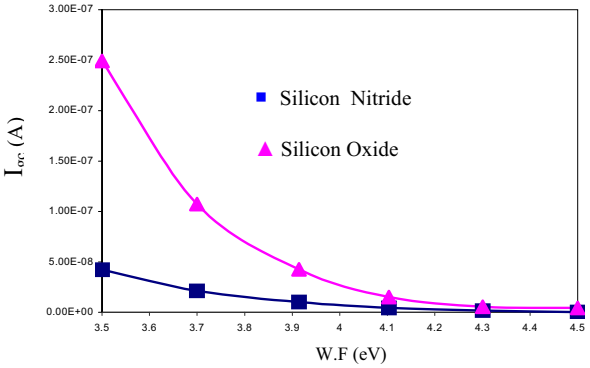

Fig.2 (f) Dependence of gate-to-channel current on metal gate work function for MGDG device.

gate-to-channel current occurs in SymDG devices (Fig.2 (a)). Fig.2 (b) shows contribution of subbands in electron tunneling for SymDG devices. It is observed that 1st subbands of both 1st and 2nd valley constitute almost whole tunneling current while contribution from 2nd subband of 1st valley is almost negligible. This trend is also continued in MGDG and AsymDG devices. Fig.2 (c) describes the gate-to-channel current as a function of inversion charge density. In DG MOSFETs, gate current can be effectively suppressed by reduced vertical electric field compared to bulk MOSFET. Electric field near the bottom of the inversion layer is considerably reduced which in turn reduces depth of the potential well and bound state energy and broadens inversion charge distribution. Life time of the QBS is increased resulting in lower tunneling.

Fig.2 (d) depicts gate current for t_{ox} = 0.5 nm and 1 nm. As oxide layer thickness is increased gate current is considerably reduced. Initial scaling of Si thickness can reduce the gate current to some extent, but excessive scaling increases the gate leakage. As we aggressively scale down the Si thickness, width of potential well is reduced and inversion charge is forced to come closer to interface, increasing the Eigen states of the carrier due to quantum confinement. Thus, carrier lifetime is decreased and gate tunneling is increased.Fig.2 (e) shows the effect of scaling of Si thickness on gate-to-channel current.

Increasing the gate metal work function lowers the effective gate voltage and thereby reducing the gate to channel leakage as shown in Fig. 2f.

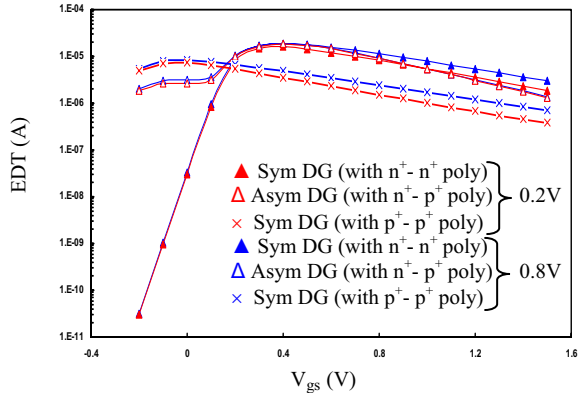

Fig.3 (a) Variation of EDT with gate voltage. SymDG with n^+ poly-n^+ drain shows steeper slope in "OFF" state. There is a considerable decrease of EDT in "ON" state.

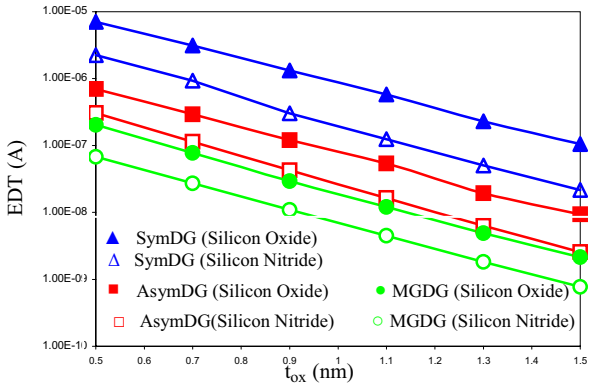

Fig.3 (b) Variation of Edge direct tunneling with oxide thickness for SymDG, AsymDG, and MGDG device.

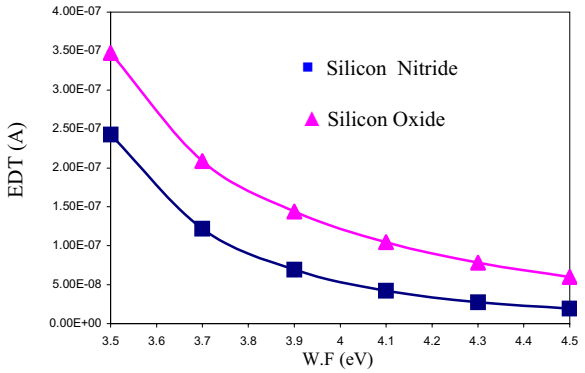

Fig.3 (c) Dependence of Edge direct tunneling on metal gate work function for MGDG device.

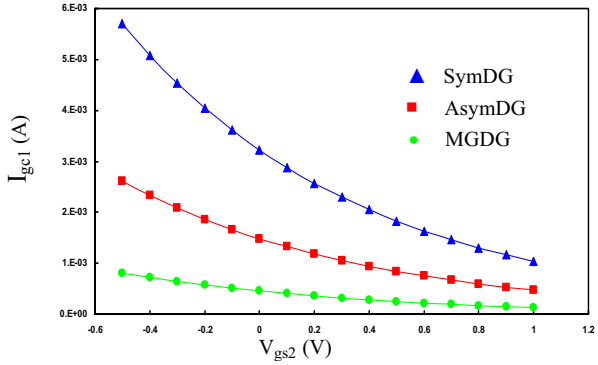

Fig.4 (a) Front gate current variation with back gate bias for SymDG, AsymDG, and MGDG devices.

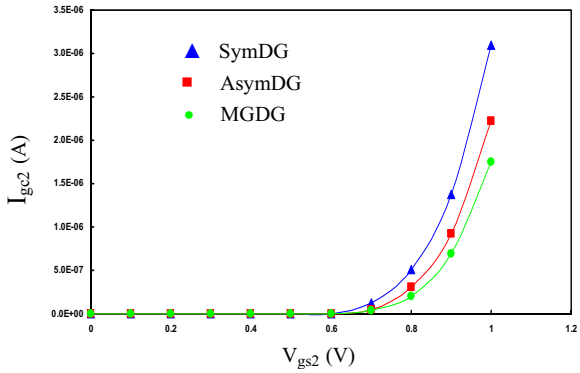

Fig4 (b) Back gate current variation with back gate bias for SymDG, AsymDG, and MGDG devices.

In "ON" state SymDG (n^+ poly-n^+ drain) has higher potential inside oxide layer than AsymDG and SymDG (p^+ poly – p^+ drain) . So, "ON" state EDT is lower in Asym DG and SymDG (p^+ poly-p^+ drain) compared to SymDG (n^+ poly-n^+ drain). EDT in MGDG devices is negligible compared to n^+ or, p^+ poly gates because of higher barrier height and effective tunneling thickness. In "OFF" state, we get steep gate leakage slope in SymDG device (n^+ poly-n^+ drain). As gate bias is increased, gate leakage is increased to reach a maximum and after particular gate bias, leakages of the three devices match. On increasing gate bias, gate leakage is considerably decreased for all three devices (see Fig.3(a)).

EDT can be reduced effectively by increasing the oxide thickness or using high-κ dielectric as shown in fig.3(b) This is similar to our observation for gate to channel leakage .However EDT is found to be more sensitive to the t_{ox} .Variation of EDT with gate metal work function is depicted in Fig. 3(c)

Fig.4(a) shows the variation of gate current in front gate of the devices with back gate bias. Here, different front and back gate voltage is applied to SymDG, AsymDG and MGDG devices. We have plotted the gate current for three different supply voltages. It is seen from the graph as we increase the back gate bias, gate current is decreased— essentially biasing backside of the substrate to more positive voltage in inversion and reducing the vertical electric field in the channel.

Fig. 4(b) shows the variation of gate current in back gate of the devices with change in back gate voltage. The gate current increases with increasing gate bias. The reason is similar to the reason of increase of gate current in front gate with change in front gate bias. As gate voltage is increased, subband energies move closer to the conduction band edge in the oxide, pushing more wave function to the oxide layer. The amount of wave function penetration is influenced by lowering barrier height which allows more wave function to penetrate inside the oxide layer. Thus, gate current is increased.

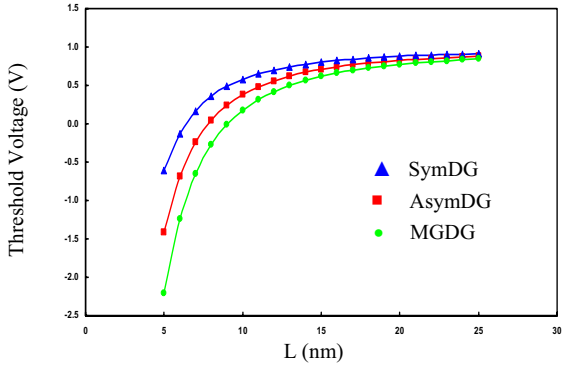

Fig.5 (a) Threshold voltage dependence on gate length for MGDG, AsymDG and SymDG devices. Higher V_{th} in MGDG reduces subthreshold current.

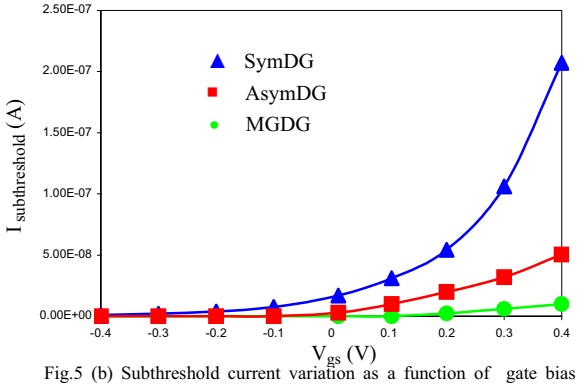

Fig.5 (b) Subthreshold current variation as a function of gate bias for SymDG, AsymDG, and MGDG devices.

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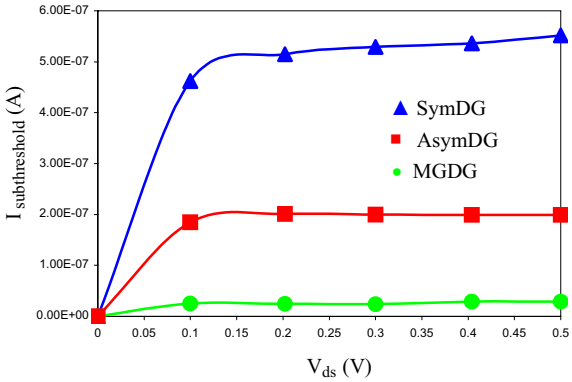

Fig.5 (c) Variation of Subthreshold current with drain bias for SymDG, AsymDG, and MGDG devices.

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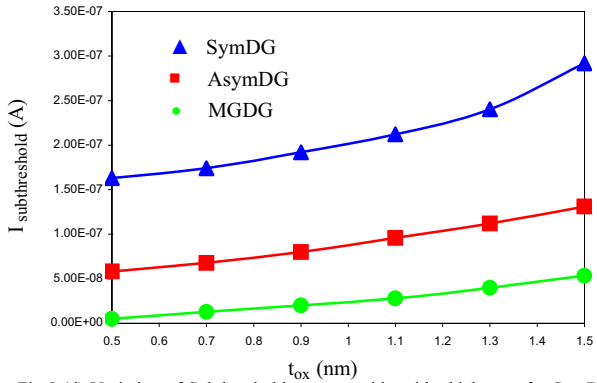

Fig.5 (d) Variation of Subthreshold current with oxide thickness for SymDG, AsymDG, and MGDG device.

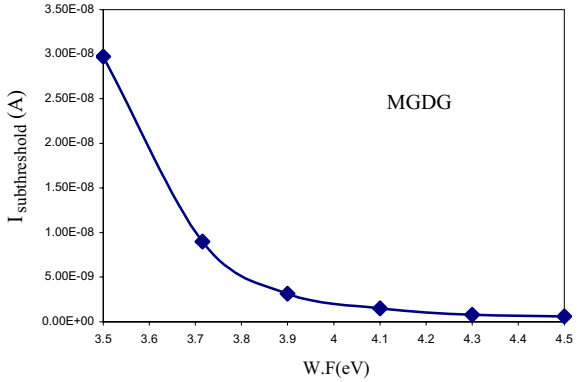

Fig.5 (e) Variation of Subthreshold current with metal gate work function for MGDG device.

Fig. 5(a) shows threshold voltage variation with channel length for SymDG (n^+ poly-n^+ drain), AsymDG and MGDG devices. It can be seen that the threshold voltage goes on decreasing as the channel length is reduced. Hence channel can be formed in lower channel potential increasing conductance quantization . In practically useful devices, the variation in V_{th} should be small in comparison with supply voltage for driving the devices. But as we decrease the effective channel length, the variation in V_{th} becomes more predominant. For L=5nm,in order to keep fluctuations of threshold voltage to a reasonable limit of 80 mV, Si thickness should be controlled better than 0.1nm, much tighter than farthest ITRS projection of 0.7nm for the critical dimension control accuracy — a very hard task to deal with.

Fig 5(b) and 5(c) shows the variation of subthreshold current with gate voltage and drain bias respectively. Elimination of poly depletion results in higher threshold voltage in MGDG compared to Sym and Asym DG devices . This results in much lower subthreshold current in MGDG MOSFET. Increase in the t_{ox} enhances the subthreshold leakage due increase in the SCE as depicted in Fig. 5(d).

Variation of subthreshold leakage with metal W.F is shown in Fig. 5(e).

Fig.6(a)-(f) shows the variation of junction band-to-band tunneling for gate bias and drain bias variations. BTBT increases with increasingly negative V_{gs1} for both MGDG and SymDG devices (Fig.6(a)). This is because of two main reasons: 1) E-field distribution relative to device geometry due to which tunneling region increases and 2) enhanced barrier heights under the gate region. In order to accurately capture and benchmark the dependence of BTBT in MGDG, we have plotted the variation of BTBT on back gate bias V_{gs2}. As we increase the back

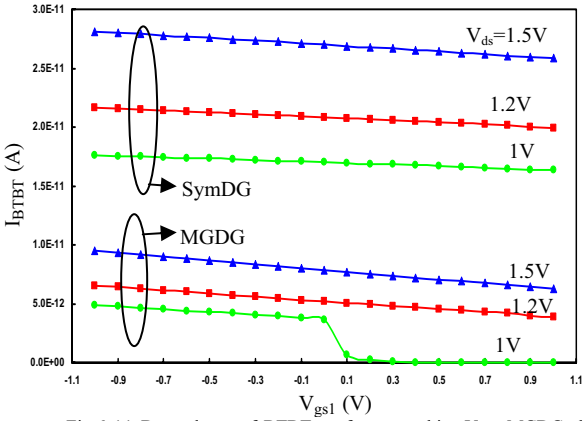

Fig.6 (a) Dependence of BTBT on front gate bias V_{gs1}. MGDG shows lower BTBT tunneling compared to SymDG devices.

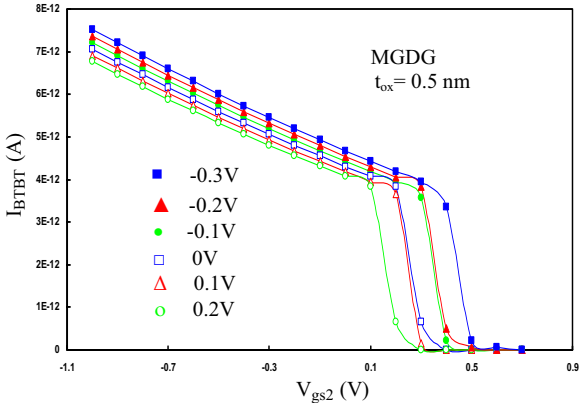

Fig.6 (b) Dependence of BTBT for MGDG on back gate bias V_{gs2} for different front gate biases. As we increase front gate bias, BTBT decreases.

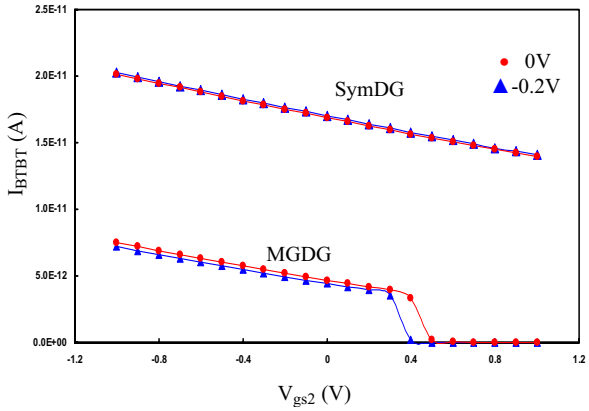

Fig.6 (c) Dependence of BTBT for MGDG and SymDG on back gate bias V_{gs2} for different front gate biases.

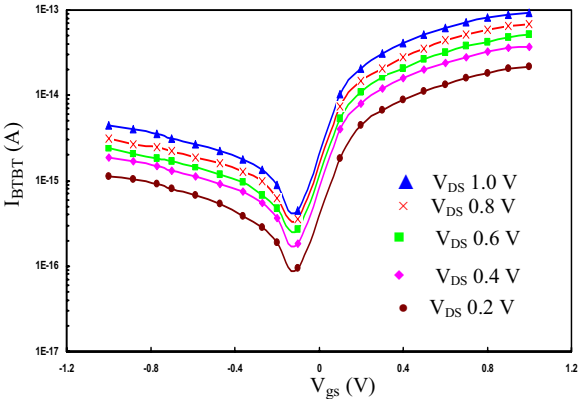

Fig.6 (d) Dependence of BTBT on gate bias for SymDG device with gate-drain overlap.

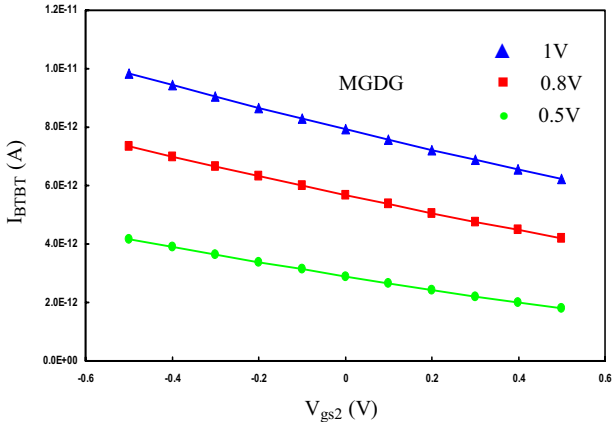

Fig.6(e) Dependence of drain-to-body BTBT on gate bias for MGDG device.

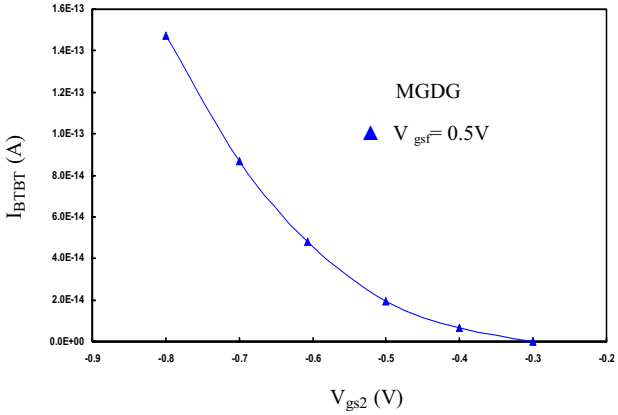

Fig.6 (f) Dependence of source-to-body BTBT on gate bias for MGDG device.

gate bias, which is equivalent to increasing the substrate bias in single gate MOSFET, BTBT is decreased (as shown in Fig.6(b)).Fig.6(c) depicts the dependence of BTBT on back gate bias for both MGDG and SymDG.

Fig.6 (d) shows the BTBT current of MGDG with front gate bias variation when there is effective overlap of gate-to-drain region. Thus on increasing the front gate bias, effective drain voltage is also increased and there is an increasing trend of BTBT current in "ON" state. In "OFF" state, behavior of BTBT is same as the previous figures. Fig.6 (e) shows the variation of drain-to-body BTBT current with back gate bias. As in previous cases, increasing back gate bias, BTBT decreases. Fig. 6(f) shows BTBT variation at source end with back gate bias. BTBT decreases exponentially with increase in back gate bias and becomes zero as we reach approximately 0.3V

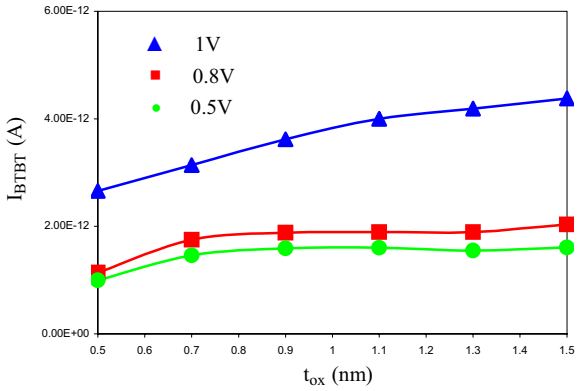

Fig.6 (g) Variation of BTBT current with oxide thickness for SymDG, AsymDG, and MGDG device.

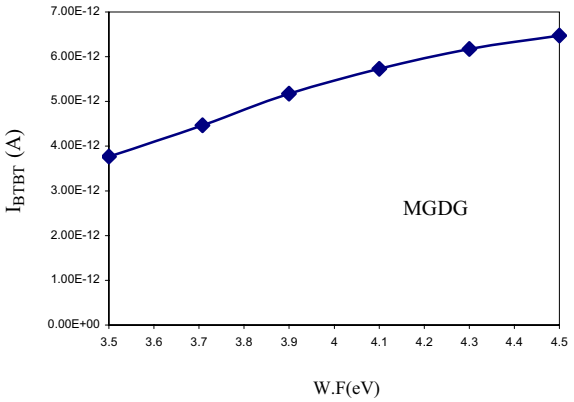

Fig.6 (h) Variation of Subthreshold current with metal gate work function for MGDG device.

BTBT remains almost invariant to the change in t_{ox} . However it shows a sligh t increasing trend due an increase in the effective electric field across the junction(Fig 6(g))

Increasing the gate metal W.F reduces the effective gate voltage and thus enhancing the tunneling current as shown in Fig. 6(h).

The growth of specific power in sub-10nm transistors may considerably exacerbate the problem of leakage power consumption in silicon integrated circuits and leakage power management becomes indispensable in futuristic nano-circuits and nano-architectures. In the next section, we will discuss the effect of stacking effect to evaluate the leakages in 6T DG SRAM cell.

V. Estimation of Leakages and Effect of Stacking in DG SRAM Cell

The effect of transistor stacking on circuit topology was first proposed for subthreshold current. In transistors connected serially, gate-to-source voltage is more negative, when the transistor is top of the stack. Again, threshold voltage of the transistors at top of the stack is increased because of body effect. Hence, "OFF" transistors at stack have lower subthreshold current than individual transistors. It has been experimentally proved that gate input "00" produces lowest subthreshold and BTBT current while "10" produces lowest gate leakage current [14]. So, it is necessary to model the leakages of the transistors in stack as it is important to determine the minimum leakage inputs to model the leakage of the SRAM cell.

A. Modeling with MGDG

We model the SRAM cell with MGDG device. The W/L ratios of the DG transistors are chosen according to [2]. When the SRAM stores 0, the wordlines are at 0 and the bitlines are held at high. If we connect the two gates of each SRAM by a wire , the corresponding

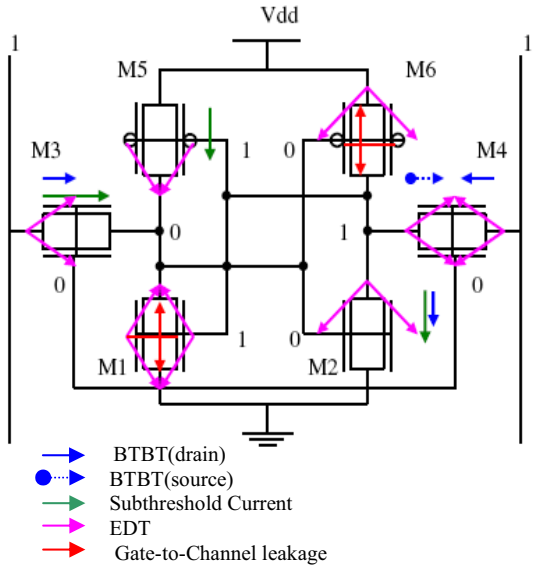

Fig.7 Leakage components in nanoscale DG SRA cell.

leakage currents will be as shown in Fig.7. Now instead of connecting the two gates together if we apply proper bias to the back gate, the leakage currents can be effectively controlled. This back gate voltage should be varied in the range so that the normal operation of SRAM is not violated. First we consider the DG NMOS transistors . For transistors which are in off state

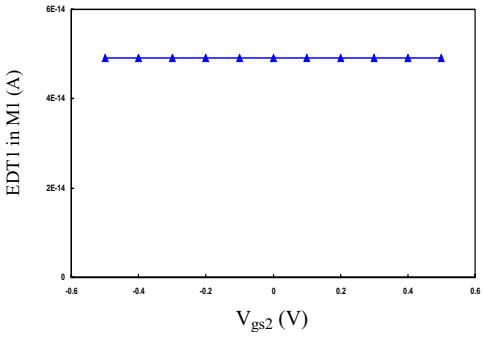

Fig. 8(a) Variation of EDT across front gate-to-drain with back gate bias in M1.

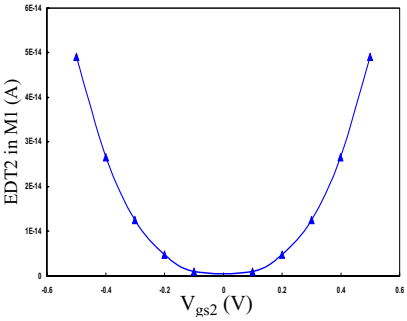

Fig. 8(b) Variation of EDT across back gate-to-drain with back gate bias in M1.

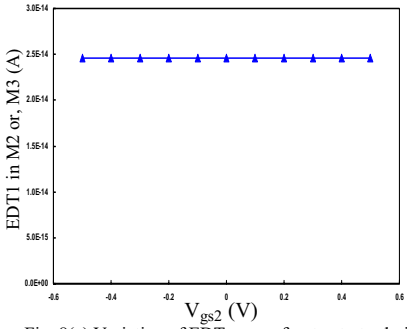

Fig. 8(c) Variation of EDT across front gate-to-drain with back gate bias in M2 or, M3.

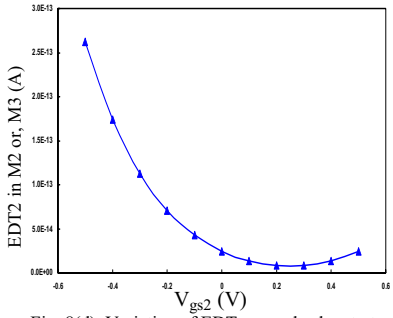

Fig. 8(d) Variation of EDT across back gate-to-drain with back gate bias in M2 or, M3.

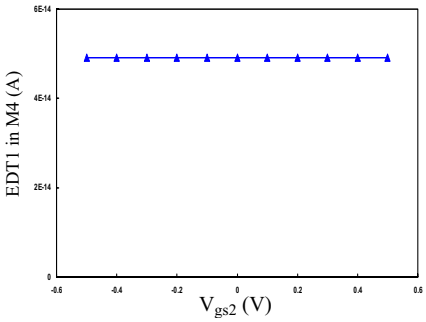

Fig. 8(e) Variation of EDT across front gate-to-drain with back gate bias in M4.

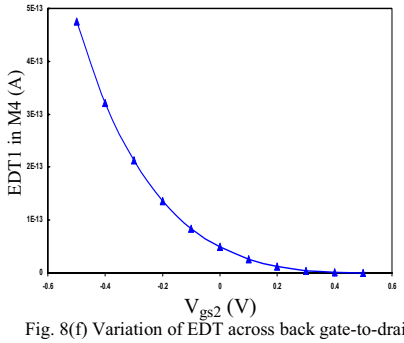

Fig. 8(f) Variation of EDT across back gate-to-drain with back gate bias in M4.

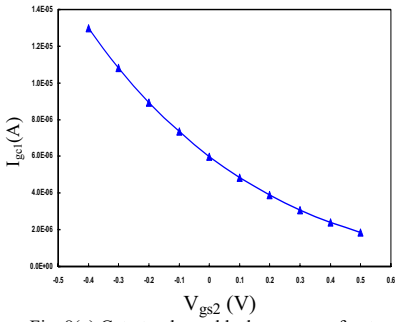

Fig. 8(g) Gate-to-channel leakage across front gate in the SRAM transistor stack.

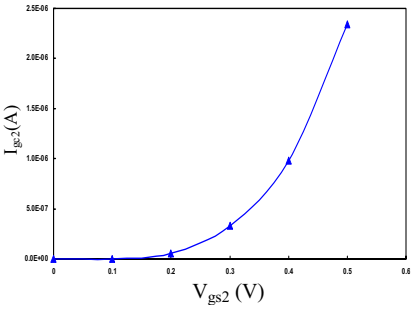

Fig. 8(h) Gate-to-channel leakage across back gate in the SRAM transistor stack.

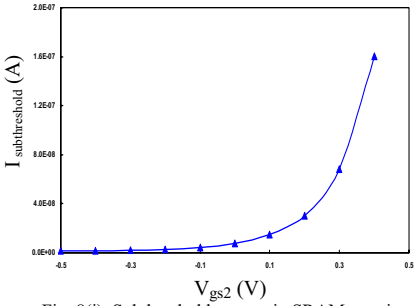

Fig. 8(i) Subthreshold current in SRAM transistor stack.

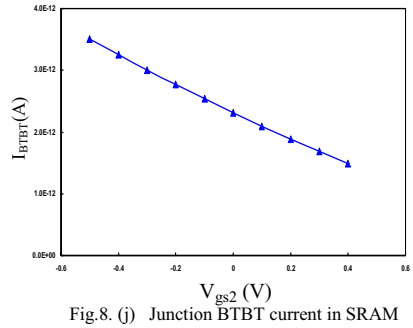

Fig.8. (j) Junction BTBT current in SRAM transistor stack.

(M2,M3,M4)BTBT, subthreshold current and EDT are the main leakage currents. Fig.8 (a)-(j) show how they vary with back gate voltage (V_{gs2}).

As V_{gs2} is decreased, BTBT increases. EDT1 remains invariant to change of V_{gs2} but EDT2 shows an upward trend with decrease in V_{gs2}. But subthreshold current decreases much more rapidly with decrease in V_{gs2} compared to increase in BTBT and EDT2. Thus for transistors in off state leakage can be reduced to a large extent by applying a suitable negative bias (about –0.3V) to the back gate of these transistors during store 0 operation. The main leakage currents in M1 which is in on state are EDT and gate to channel leakage.

As EDT is much small compared to I_{gc} our main objective is to reduce I_{gc}. I_{gc1} decreases with increase V_{gs2}. But we cannot increase V_{gs2} without limit as we should not forget that as V_{gs2} increases I_{gc2} comes into picture and it increases with V_{gs2}. From the figure it is clear that at a back gate voltage of about 0.3V the total gate to channel current is minimum

B. Interconnection Effect

So far in our discussions we have assumed the node voltages V_1 and V_2 to be ideally at 0 and Vdd respectively. But due to finite leakage currents as well as on state currents , V_1 will be raised to some non-zero voltage and voltage at V_2 should be something lower than Vdd. This change in node voltages not only affect the drain to source voltages but also modify the gate voltages of the p and n type MOSFETS and thereby influencing the leakage currents in dual ways. We name this effect as interconnection effect. We use numerical methods for finding the two node voltages and the modified leakage currents.

Applying KCL at the two nodes we get

For 1st node

Ibtbt_3+ Isub_3+ Isub_5+ Igdo_5+ Igcd_1+ Igdo_1-Ids_1=0 (9)

For 2nd node

Ibtbtd_4- Ibtbts_4+ Isub_4 -Igso_4 +Ids_6-Igcd_6-Ibtbtd_2-Isub_2-Igdo_2=0 (10)

Where

Ibtbtd_3=BTBT current due to drain in M3

Ibtbts_4=BTBT current due to source in M4

Isub_3 = subthreshold current in M3

Igdo_1= EDT at gate to drain overlap region in M1

Igso_4= EDT at gate to source overlap region in M4

Igcd_1=gate to channel current which goes to drain in M1

Ids_1=on state drain to source current.

We solve (9) and (10) self consistently to get the desired results. The various leakage currents in different n-MOSFETS of symmetric MG DG are shown in the table (I)-(IV). The first row represents leakage currents without considering the Interconnection effects while 2nd row represents those after these effects have been taken into account.

As seen from the tables Isub has decreased in M3 which is but obvious as drain to source voltage has reduced. Also we get non zero Isub in M4 due to reduction in v2.Again, though drain to source voltage has reduced in M2, I_{sub} has increased due to increase in gate to source voltage. Decrease in gate voltage in M1 has reduced the gate to channel current in it. I_{btbt} has decreased in M2 due to decrease in Vds and increase in gate voltage. Another important change is the nonzero gate leakage in M2 and M3 at the source gate overlap region due to difference in source and gate voltages induced by non zero v1.

M1 table I

I_{gc}	I_{gdo}	I_{gso}
2.5805e-4	2.8780e-9	2.8780e-9
2.5791e-4	2.8443e-9	2.8777e-9

M2 table II

I_{sub}	I_{btbtd}	I_{gdo}	I_{gso}
2.3092e-10	2.814e-12	2.878e-9	0
2.5222e-10	2.8030e-12	2.8443e-9	4.378e-14

M3 table III

I_{sub}	I_{btbtd}	I_{gdo}	I_{gso}
2.3092e-10	2.814e-12	2.878e-9	0
2.3021e-10	2.8140e-12	2.878e-9	4.378e-14

M4 table IV

I_{sub}	I_{btbtd}	I_{btbt_s}	I_{gdo}	I_{gso}
0	2.814e-12	7.6792e-13	2.8780e-9	2.8780e-9
1.038e-13	2.814e-12	7.6784e-13	2.8780e-9	2.8777e-9

Thus it is seen that due to the interconnection effect some leakage currents increases while others decreases. So this effect must be studied minutely for effective design of a SRAM.

VI. Conclusions

This paper embarks on a comprehensive quantitative approach towards the simulation of different leakages predominant in a nano circuit and architecture. We have developed the simulation tool for evaluating electrostatics and transport by solving 2D Poisson and Schrödinger equations self-consistently. We also developed the numerical models for evaluating gate-to-channel leakage, EDT, subthreshold and BTBT leakage for nanoscale DG MOSFETs. We have comprehensively analyzed the stacking effect of DG devices to model the leakages in 6T SRAM cell. Our analysis shows that use of metal gate (MG) DG devices with intrinsic body doping can significantly reduce all types of leakage components making it very efficient for constructing SRAM cell. Though threshold voltage is higher in MGDG devices than SymDG and AsymDG devices, elimination of poly depletion and random doping fluctuation can efficiently decrease the subthreshold current. Intrinsic body doping also helps to reduce EDT. As there is no bulk charge for MGDG, gate-to-channel leakage is also reduced. Hence, we can conclude that MGDG devices can emerge as one of the promising candidate for reducing all leakage components making it efficient for low power circuit design in sub-10nm regime.

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