A Dual-Backup Configuration Memory of Embryonic Self-Repairing Hardware

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Abstract: Embryonic hardware is a kind of digital circuit structure which has the innative characteristics of distributed autonomous control and self-repairing. Configuration memory is the important module in cell circuit to determine function and interconnection of cells, it remains reliable is the precondition for the cell array to work normally. At present, the self-repairing and structural simplification of configuration memory are key research directions. Many structures and design strategies have been put forward for circuit simplification, but few methods for hardware self-repairing, while which should be more important. New techniques should combine the abilities of self-repairing and simplification need to be continuously explored. Currently known self-repairing strategies only ensure the configuration memory store the configuration data, but not ensure the reliability of the registers in which the configuration data are stored. In this paper, a dual-backup configuration memory structure based on shift registers is proposed. Each cell saves the configuration data of the left adjacent cell and the configuration data of the current cell as backups. The function of a fault-cell can be replaced by its right cell. Each cell only needs to save three pieces of configuration data to ensure that the configuration memory can be repaired in a variety of faults. The circuit structure and self-repairing strategy of configuration memory are given, and the self-repairing ability is simulated and verified.

Key words: Embryonic hardware, configuration memory, self-repairing strategy, dual-backup structure.

1. Introduction

Embryonic self-repairing hardware, also referred to as embryonic hardware, is a kind of reconfigurable hardware with outstanding mechanisms of distributed self-replication, self-organization and self-repairing [1]-[4]. The circuit of embryonic hardware is composed of electronic cells with same structure in the form of arrays, it is a very suitable design method for improving the hardware reliability of electronic system in harsh environment [5]-[7]. At present, embryonic hardware represents an innovative structure of high-reliability digital system.

Configuration memory is the module for storing configuration data in embryonic cells. Correct configuration data is the basis for the cell array to work normally. Current methods to access the reliability are to store redundant data and back up a large number of cell configuration data. Therefore, hardware consumption of configuration memory accounts for a high proportion of embryonic hardware circuits [8], [9], in full-backup storage structure, each cell stores configuration data of all cells, so resource redundancy

is enormous [3]. Therefore, many simplified methods on the configuration data of configuration memory emerges. In part-backup storage structure, only configuration data of the possible alternative cells are stored. Tyrrell *et al* [10], Zhang X *et al* [11], [12], Samie *et al* [13], CAI J *et al* [14] proposed the corresponding configuration memory structure and self-repairing strategies, the redundancy was reduced. In another correlation-backup storage structure, each cell needs to store its own characteristic configuration data and relevant configuration data with other cells, the working configuration data is generated in the process of self-repairing [15]. Among the three structures, part-backup storage structure is the main research direction, but, up to present, none of them solves the self-repairing problem of registers which store the configuration data.

At present, the main research achievements of the configuration memory are simplification, but lack of repair methods for hardware failure. In most self-repairing strategy, it is often considered that configuration memory is reliable when the configuration data are included, but if the register circuit fails, the cell array can't be repaired actually. Circuit simplification and self-repairing strategy of configuration memory are two problems need to be solved urgently.

In this paper, a dual-backup configuration memory structure based on shift registers is proposed. Configuration data can be shifted and transferred during normal operation period of cells. The new structure can reduce the redundancy of configuration data. The circuit and self-repairing strategy of configuration memory is presented, and the ability of self-repairing is verified.

2. Structure of Configuration Memory

The typical architecture of the self-repairing embryonic hardware is two-dimensional cell array, all cells are the same in internal. Each cell is mainly composed of four modules: Controller, Function circuit, I/O routing switch and Configuration memory [2]. Controller controls all operations of the cell. Function circuit is the processing block with the LUT as core part. The I/O routing switch is responsible for connecting and transferring data with surrounding cells. The Configuration memory deposits all configuration information of cells. Fig. 1 shows the structure of embryonic cell array and internal modules.

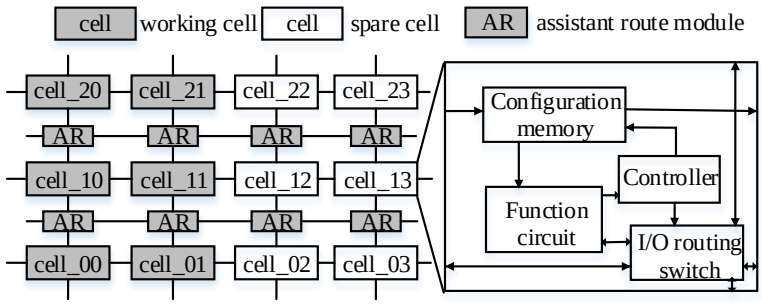

Fig. 1. Two-dimensional embryonic cell array and internal modules.

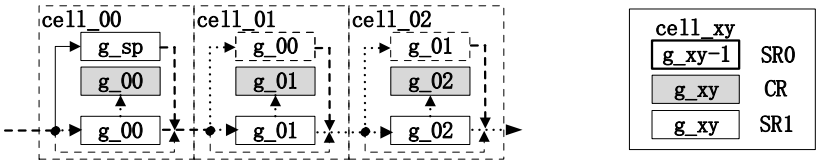

Fig. 2. Interconnection diagram of dual-backup configuration memory module.

Designed based on shift registers, the structure of configuration memory is characterized that the shift transfer mechanism can avoid hardware redundancy caused by the backup of a large amount of

configuration data, and realize the simplification of the circuit. However, to prevent the breakage of the shift chain between registers, a simple series structure of the shift register chain need to be avoided, and at the same time, the configuration data needs to be transferred dynamically to reduce the shift time.

The dual-backup configuration memory and interconnection diagram is shown in Fig. 2. The configuration memory in each cell contains three registers, SR0, SR1, and CR. The CR stores the working configuration data of current cell. SR0 and SR1 save the configuration data of left cell and configuration data of current cell for backup, both of them are serial input, serial/parallel output shift registers. In the Fig.2, cell_xy represents the coordinate of cell at the xth row and yth column in the array, g_xy represents configuration data in the register. There are at least two backups of the configuration data for each cell, one in the current cell and another one in the adjacent right cell, and they are connected by a unidirectional shift register chain. The right cell can send a shift signal to the left cell, and the right cell will be rewritten with the configuration data in left cell.

Fig. 3 shows the internal structure of configuration memory. '*M*1' and '*M*2' control which backup configuration data is loaded in CR, and 'bypass' controls whether the configuration memory is transparent. The configuration memory can work in three modes, two normal work modes and transparent mode. Table 1 shows the values of control signals and work modes of the internal registers.

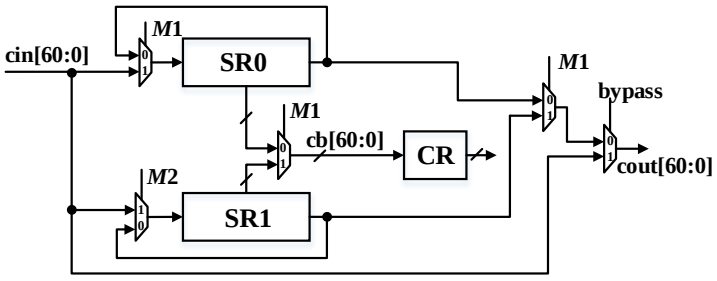

Fig. 3. Structure diagram of configuration memory.

Table 1. Control Signals and Work Modes of Configuration Memory

Working mode	Working mode 0	Working mode 1	Transparent mode
Explanation	SR0 backs up the configuration data of left cell, SR1 backs up the configuration data of current cell	SR1 backs up the configuration data of left cell, SR0 backs up the configuration data of current cell	The configuration memory is eliminated
*M*1	1	0	1
*M*2	0	1	1
bypass	0	0	1

3. Self-repairing of Configuration Memory

3.1. Shifting Strategy

If a fault occurs in the register that stores the backup configuration data of left cell, the shifting self-repairing will be triggered. Assume all the cells are working in mode 0, so the register SR0 in current cell saves the backup configuration data of left cell and connects to the SR1 in left cell. When a fault is detected in SR0, the current cell sends shift signal to the left cell, then the configuration data in SR1 of the left cell will be shifted into SR0 of the current cell for reconfiguration.

Fig. 4 illustrates the repairing process of shifting strategy in a cell row. In Fig. 4(a), a transient fault in SR0

of cell_01, so cell_01 sends a shift signal to cell_00 (the left cell), then the configuration data g_00 will be shifted from SR1 of cell_00 to SR0 of cell_01. In Fig. 4(b), the transient fault in SR0 of cell_01 will be repaired after the shifting for reconfiguration. If SR0 suffered a permanent fault, the fault will be detected again, then the eliminating self-repairing will be triggered.

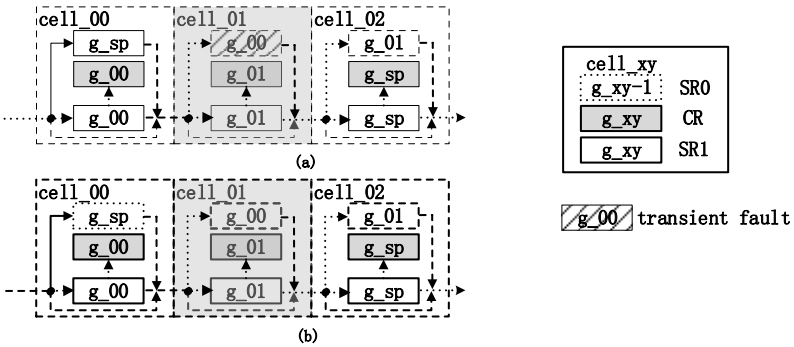

Fig. 4. Repairing process of shifting strategy.

3.2. Eliminating Strategy

If the CR or the backup register for configuration data of the current cell (SR1) is detected in fault, the eliminating of configuration memory will be triggered. The configuration memory of current cell will work in the transparent mode, and all the cells on the right side of the fault cell switch their working mode, then load the CR with the configuration data in SR0 to implement the function replacement.

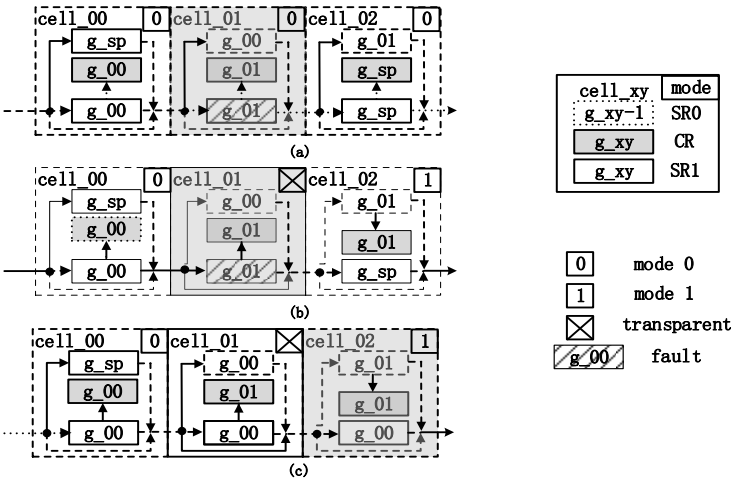

Fig. 5. Repairing process of eliminating strategy.

Fig. 5 illustrates the repairing process of eliminating strategy. Assume the initial working status of cells is mode 0, the situations of the injected faults are as follows: a fault in g_01 in SR1 of cell_01, where permanent and transient faults are treated in the same way.

In Fig. 5(a), g_01 in SR1 of cell_01 suffers a fault, then cell_01 is eliminated (work in transparent mode), which is shown in Fig. 5(b). The configuration memory of cell_00 is directly connected to cell_02's. At the same time, all the cells on the right side of the fault cell switch to work mode 1, and the CRs are configured with the backup configuration data. Configuration data in CR of cell_02 is g_01, but the process of configuration memory self-repairing is still going on, the configuration data of the left cells need to be

backed up into cell_02 for the next self-repairing, which is shown in Fig. 5(c), SR1 of cell_02 stores the configuration data of g_00. Cell_01 works in transparent mode, both SR0 and SR1 of cell_01 store configuration data of the left cell, but not in connection with the memory of right cell.

4. Simulation and Analysis

In order to verify the self-repairing ability of the configuration memory proposed in this paper. Using VHDL language and Xilinx ISE14.7 to design circuit and ISim for function simulation. The correctness of the self-repairing processes shown in Fig. 4 and Fig. 5 are verified.

Fig. 6 shows the simulation sequence diagram of configuration memory like in Fig. 4 and Fig. 5.

(1) At 1000ns, SR0 in cell_01 is injected a transient fault (signal 'cm_backup_error' in cell_01 is set to 1 and lasts one clock). On the rising edge of the clock, the fault cell sends a request signal for backup to the left cell, where back_up = 1. After receiving the signal 'back_up', on the next clock at 1015ns, the left cell begins to shift backup data.

(2) At 1175ns, the configuration data in SR1 of cell_00 is completed transferred into SR0 of cell_01, which has been reconfigured and self-repaired.

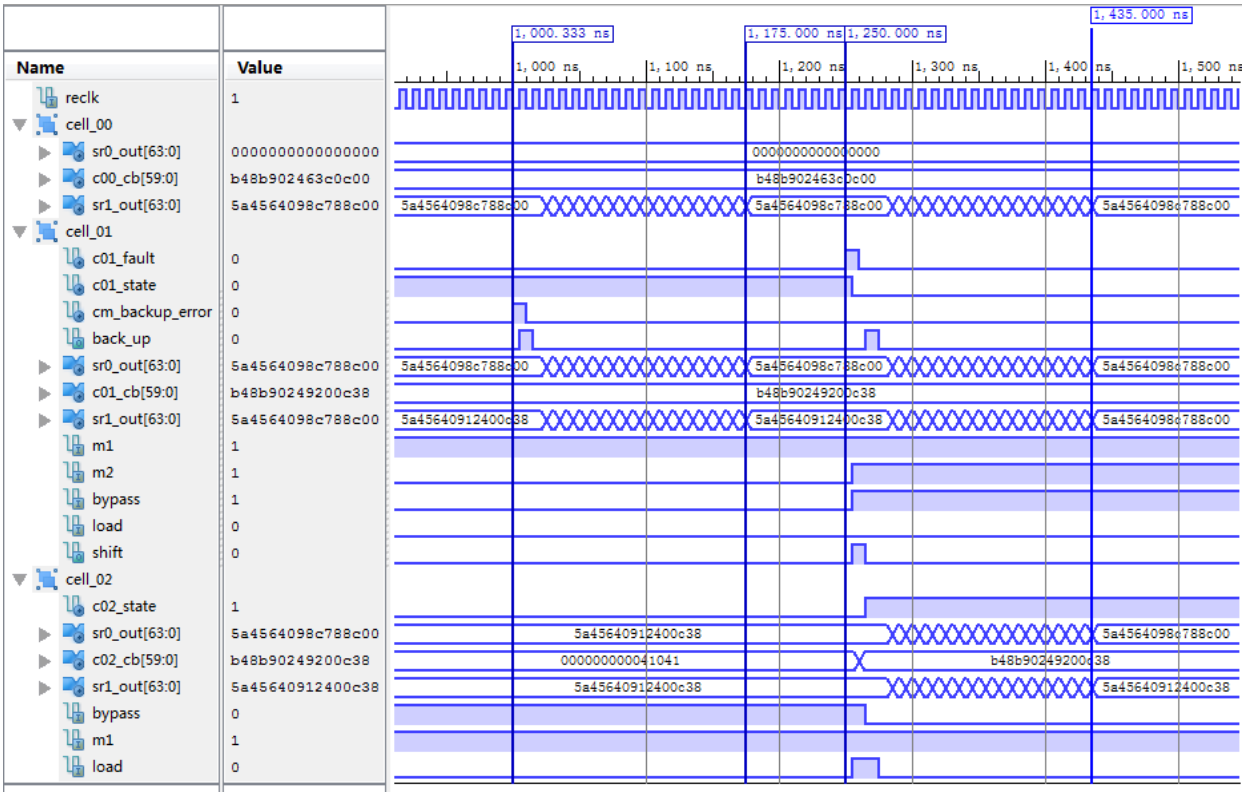

Fig. 6. Simulation sequence diagram of configuration memory.

(3) At 1250ns, SR1 in cell_01 suffers a transient fault, signal c01_fault is 1 and lasts one clock. Self-repairing process starts on the rising edge of the next clock at 1255ns, bypass=1, shift=1, *M*2=1 of cell_01, and the cell switches in transparent mode.

(4) One clock later, cell_02 switches to work mode 1, and be configured to perform the function of cell_01. Function self-repairing of cell array is completed in 2 clocks. The working configuration data of cell_00 on the left side needs to be transferred to SR1 in cell_02 as backup. Cell_01 works in transparent mode, and both SR1 and SR0 back up the configuration data of cell_00, self-repairing process completes at 1435 ns.

5. Conclusions

This paper proposes a dual-backup configuration memory structure based on shift registers. Only 3 copies of configuration data in each configuration memory, they are the working configuration data, the backup configuration data of the left cell and the backup configuration data of the current cell. The circuit of configuration memory is greatly simplified. The backup register for left cell configuration data can be repaired by the way of configuration data shift when suffers transient faults. Faults in other registers are repaired by configuration memory eliminating. Simulation results illustrate that the correctness of self-repairing ability.

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