Effective Routing Algorithm and Topology on Power Consumption in Networks on Chip

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Abstract: Network on Chip (NoC) is used as an appropriate solution to solve the communication problems in System on Chip (SoC). Due to the advanced VLSI technology the power consumption has become a major part in NoCs. In this article we compare the effect of different routing algorithms and topologies on power dissipation in NoCs. This paper illustrates the efficacy of low power encoding approach on power consumption in on chip networks. We assess the impact of deterministic, partially adaptive and fully adaptive routing algorithms and also mesh and torus topologies with and without using low power encoding algorithm on link and total power consumption in NoC.

Key words: Network on Chip, power consumption, low power encoding, routing algorithm, topology.

1. Introduction

The progress of VLSI technology allows researchers to design a complete system on a chip called System on Chip (SoC). There are cores that are connected to each other by means of a network by the name of interconnection network. This Interconnection network has significant duty in SoCs. Researchers have introduced an appropriate structure to improve these interconnections by borrowing a couple of new ideas from computer network field [1] called the Network on Chip (NoC). Network on Chip is a solution for today's problem of System on Chip [1], [2]. Several researchers believe that on chip interconnection has a significant portion of power which is consumed in chip and its contribution is expected to grow up in future [3].

Power dissipation is introduced as an important issue in NoCs because of advanced VLSI technology [4]. Researchers proposed many different approaches to decline energy consumption in NoCs [5]-[19]. A great deal of research has been conducted to reduce the energy dissipation of NoCs with using optimized algorithms [6]-[15]. Another approach to minimize the power dissipation is low power encoding algorithms [5], [16]-[19]. These methods try to reduce the number of switching activities and dynamic power dissipation. It should be mentioned that the power of encoder and decoder are the overhead of low power encoding algorithms which must be considered to evaluate its efficiency. Researchers in [5] present a new low power encoding algorithm for on chip networks which is called MFLP (Most Frequent Least Power).

MFLP [5] decrease the number of ones in the code words. The data is sent with transition signaling, hence, the number of switching activities is declined. Tree based structure is used in MFLP to assign high probability data to the less ones symbols. Based on MFLP most frequent symbols have least number of ones. Thus, the power consumption is minimized [5].

Topology determines the connection among the routers in NoCs. Some researchers present and analysis different topologies for NoCs. In [20], authors suggest a new NoC topology synthesis methodology to generate optimum topology. Power consumption and area are optimized in the generated topology. Mesh and torus are known as famous topologies in NoCs. There is no diagonal links in mesh and torus topologies. The difference between mesh and torus is extra link in the torus topology. While, some researchers present a new topology for interconnection networks that has diagonal links in a direction [21]. Topology divided into two parts; regular and irregular. Mesh and torus are regular topology. In [6], [7], [22], irregular topologies for NoC proposed. These irregular topologies are used for application specific NoC architectures. Investigators in [22] proposed a generation method to create fault-tolerant irregular topology for NoC architectures. In the case of any failure on routing, presented topology select various routing path.

Routers in NoCs route the data according to routing algorithm. Routing algorithms are divided into three groups; deterministic, partially adaptive and fully adaptive. The problems on routing occur when the packets cannot pass from sender to receiver. These problems are deadlock, livelock and starvation. Routers have an impact on power dissipation, performance and throughput in NoCs. Therefore, several researchers work to improve the routing algorithms. New adaptive routing algorithms are introduced to improve fault tolerant ability in NoCs [23]. Their novelty provides the routers to alleviate congestion in NoCs. Presented routing algorithm select the weighted path to preserve the NoC performance [23]. Another adaptive routing algorithm presented in [24]. They improve the throughput and power dissipation with removing additional wires and utilize of free bits in flit to propagate congestion information [24]. Researchers in [25], use ant colony optimization technique to propose a fault aware routing algorithm for NoC. This approach enables router to find minimum congestion path which is not faulty. The optimization algorithm after finding the obstacle in NoC try to search for a new path based on the fault information and finally selects the optimum path [25]. They improve the throughput compare the related researches. The cost of implementation in ant colony optimization algorithm is high. Hence, modified ant colony technique proposed in [26]. In [27], a developed path selection in adaptive routing algorithm suggested. They consider both channel and switch information to find congestion situation. Deadlock due to the irregular topologies in NoCs and load balancing status are two problems in on chip networks. To overcome such problems, in [28], researchers present a routing algorithm that is more efficient compare to the previous routing algorithms.

MFLP as a low power encoding algorithm has an impact on routing algorithm and topology. We examine the effect of deterministic, partially adaptive and fully adaptive routing algorithms on power consumption with and without low power encoding technique. The power dissipation of NoC is divided into two parts; router and link. It should be mentioned that the network interface's power consumption is considered in the router's power. The impact of low power encoding algorithm on link and total power consumption with various routing algorithm is studied. We also assess the effect of low power encoding approach on the link and total power dissipation with different topologies.

We utilize power compiler tool from Synopsys[1] to measure router's power. Static and dynamic power consumption in NoC is evaluated with power compiler tool. Link's power is calculated by $P_{link} = \alpha C V_{dd}^2 f$, where α is the switching activity on the link, C is the link and coupling capacitance, V_{dd} is the power supply of the system and f is the clock frequency.

Based on the International Technology Roadmap for Semiconductors [3], for 65nm technology V_{dd} is 1 volt. According to the critical path of the system clock frequency is 500 MHz. The length of the metal wires for the mesh topology is 2 mm. The capacitance of the wire links and coupling are 0.2 pF/mm and 0.6

[1]Synopsys and Modelsim are registered trademarks

pF/mm, respectively. The transitions of wires are calculated by Modelsim1. The coding methods and the NoC infrastructure are implemented in VHDL.

Default of implementation for the NoC is 16 cores mapped onto the mesh topology and XY routing algorithm. There are two virtual channels per each physical one. Packets are injected with a uniform traffic and the packet length is 32. In the NoC infrastructure the wormhole routing technique is used.

2. Topology

In this section, the effect of two of the famous topologies, mesh and torus on link and total power consumption in NoC are studied. Results on link and total power dissipation which are listed in Tables 1, 2, 3 and 4 show the impact of using low power encoding algorithm with different topologies. In the following tables, N.C stands for the No Coding. It means that in these columns the results of power consumption without using any low power encoding approach is reported. In the column with the title of MFLP, the power dissipation of MFLP as a low power encoding algorithm is listed. The percentage of power improvement due to using low power encoding approach is shown in the next column.

Table 1. The Link Power Consumption with Mesh Topology

Topology	Mesh		
File name	N.C	MFLP	Improvement (%)
.TXT	27.15	19.51	28.11
.GIF	31.08	20.88	32.81
.WAV	30.15	16.22	46.20
.HTML	28.25	22.78	19.38
.JPG	33.00	20.37	38.25
.BMP	15.86	12.53	20.95
.PNG	22.19	15.29	31.09
.PDF	31.83	20.35	36.04
.DOCX	28.40	18.00	36.62

Table 2. The Total Power Consumption with Mesh Topology

Topology	Mesh		
File name	N.C	MFLP	Improvement (%)
.TXT	80.57	72.96	9.44
.GIF	84.93	75.32	11.31
.WAV	84.03	70.09	16.58
.HTML	81.76	76.87	5.98
.JPG	87.12	74.90	14.02
.BMP	70.17	65.09	7.23
.PNG	74.31	68.82	7.38
.PDF	85.89	74.93	12.76
.DOCX	81.97	72.08	12.07

Table 3. The Link Power Consumption with Torus Topology

Topology	Torus		
File name	N.C	MFLP	Improvement (%)
.TXT	27.10	19.68	27.39
.GIF	30.45	21.30	30.06
.WAV	29.98	16.57	44.71
.HTML	28.03	23.02	17.89
.JPG	32.43	20.62	36.40
.BMP	15.53	12.77	17.76
.PNG	21.54	15.71	27.03
.PDF	31.16	20.62	33.82
.DOCX	27.70	18.27	34.03

Table 4. The Total Power Consumption with Torus Topology

Topology	Torus		
File name	N.C	MFLP	Improvement (%)
.TXT	81.94	73.22	10.64
.GIF	85.68	75.87	11.44
.WAV	85.28	70.55	17.26
.HTML	82.95	77.25	6.87
.JPG	87.95	75.27	14.41
.BMP	71.19	65.43	8.09
.PNG	74.96	69.36	7.48
.PDF	86.63	75.33	13.04
.DOCX	82.64	72.47	12.30

Torus topology is a modified form of mesh topology. In torus topology the heads and the tails in each column and also right side and left side of rows are connected to each other. In other words, the difference between mesh and torus topologies is an extra link in each node. The extra link in torus topology damages the consecutiveness in the data. The consecutiveness of data is an important factor in MFLP to be effective in power reduction. As shown in the above tables mesh topology is better than torus in terms of links power dissipation. It is obvious that because of the extra link in each node in torus topology the data is not consecutive as much as mesh topology. Therefore, the links power improvement in mesh topology is better than torus. According to the above results it can be concluded that there is no significant difference between mesh and torus topologies in terms of total power consumption. It is worth mentioning that the effect of the proposed method as a low power encoding technique should be considered in the link's power dissipation. It is obvious that after applying encoder and decoder as overhead of low power encoding algorithm, the router's power in NoC increased.

3. Routing Algorithm

According to the adaptability of routing algorithms, they can be divided into deterministic, partially adaptive and fully adaptive algorithms. Even though the adaptive routings are used in the systems in order to improve the performance, it suffers from a great deal of weakness. Researchers in [29] introduce a scheme to ensure that all packets can be delivered in an orderly format. It can remedy the out-of-order delivery which is a critical problem of adaptive routing algorithm. Moreover, an adaptive routing algorithm which is dedicated to multicast packets is introduced in [30]; it applies a multicast tree in order to have a dead lock free adaptive routing for this kind of packets. This scheme can also be applied for unicast packets which is the advantage of this approach. In [31] a deadlock free routing algorithm which is a new architecture decreasing the complexity of routing algorithms' implementation presented.

In this research XY, OE and Duato routing algorithm are considered to investigate the effect of low power encoding approach on power consumption in NoC. XY is known as a deterministic routing algorithm, OE is partially adaptive routing algorithm and Duato is a fully adaptive routing algorithm.

Table 5. The Link Power Consumption with XY Routing Algorithm

Routing	XY		
File name	N.C	MFLP	Improvement (%)
.TXT	27.15	19.51	28.11
.GIF	31.08	20.88	32.81
.WAV	30.15	16.22	46.20
.HTML	28.25	22.78	19.38
.JPG	33.00	20.37	38.25
.BMP	15.86	12.53	20.95
.PNG	22.19	15.29	31.09
.PDF	31.83	20.35	36.04
.DOCX	28.40	18.00	36.62

To prevent deadlock in Duato routing algorithm at least two virtual channels is needed. Therefore to have a fair comparison between the routing algorithms, we consider two virtual channels for the other routing algorithms.

Table 6. The Total Power Consumption with XY Routing Algorithm

Routing		XY	
File name	N.C	MFLP	Improvement (%)
.TXT	80.57	72.96	9.44
.GIF	84.93	75.32	11.31
.WAV	84.03	70.09	16.58
.HTML	81.76	76.87	5.98
.JPG	87.12	74.90	14.02
.BMP	70.17	65.09	7.23
.PNG	74.31	68.82	7.38
.PDF	85.89	74.93	12.76
.DOCX	81.97	72.08	12.07

Table 7. The Link Power Consumption with OE Routing Algorithm

Routing		OE	
File name	N.C	MFLP	Improvement (%)
.TXT	18.28	13.35	26.95
.GIF	20.45	14.31	30.04
.WAV	20.05	11.49	42.66
.HTML	18.85	15.22	19.27
.JPG	21.50	14.09	34.46
.BMP	11.77	9.42	20.02
.PNG	15.09	11.01	27.03
.PDF	20.80	13.92	33.03
.DOCX	18.63	12.37	33.59

Table 8. The Total Power Consumption with OE Routing Algorithm

Routing		OE	
File name	N.C	MFLP	Improvement (%)
.TXT	69.12	62.59	9.44
.GIF	71.55	64.37	10.04
.WAV	71.16	61.29	13.87
.HTML	69.74	64.90	6.94
.JPG	72.75	64.28	11.65
.BMP	63.14	58.21	7.79
.PNG	65.13	60.45	7.17
.PDF	72.03	64.19	10.88
.DOCX	69.49	62.11	10.61

Table 9. The Link Power Consumption with Duato Routing Algorithm

Routing		Duato	
File name	N.C	MFLP	Improvement (%)
.TXT	29.63	20.95	29.30
.GIF	33.54	22.82	31.97
.WAV	32.84	17.54	46.57
.HTML	30.72	24.70	19.57
.JPG	35.58	22.17	37.69
.BMP	16.97	13.14	22.55
.PNG	23.73	16.50	30.47
.PDF	34.31	22.10	35.58
.DOCX	30.41	19.50	35.87

Tables 5, 6, 7, 8, 9 and 10 compare the link and total power consumption with and without using low power encoding in NoC with XY, OE and Duato routing algorithms. Based on the results, it can be concluded

that from the links power dissipation point of view XY and Duato routing algorithms are better than the OE. Moreover, in terms of total power consumption XY routing algorithm is better than the others.

In this case two facts about power reduction with using low power encoding should be mentioned. Firstly, the power improvement is better when the links power dissipation is increased. The reason is due to the impact of low power encoding techniques on the link's power consumption. In other words, with increasing the link power dissipation, the impact of using low power encoding approaches on power reduction increased as well. Secondly, the distribution of data has an impact on power reduction. In the case of uniformly distribution of data, the traffic distributed smoothly and performance improved, consequently, the link power dissipation goes up. According to the results, with the increased consumption of the network power on the link, our approach is shown to be substantially better. On the other hand, when a routing algorithm is distributed uniformly, the power consumption of the link goes up because the more traffic is distributed smoothly, the more performance we have and, in turn, the more power is consumed. However, the results also show that OE, as a partially adaptive algorithm, cannot distribute traffic more smoothly than XY as a deterministic algorithm.

Table 10. The Total Power Consumption with Duato Routing Algorithm

Routing		Duato	
File name	N.C	MFLP	Improvement (%)
.TXT	75.77	73.08	3.54
.GIF	80.07	76.01	5.07
.WAV	79.31	70.09	11.62
.HTML	77.94	77.56	0.49
.JPG	82.26	75.44	8.28
.BMP	64.78	64.29	0.76
.PNG	69.10	68.71	0.55
.PDF	80.95	75.41	6.83
.DOCX	76.71	72.30	5.75

4. Conclusion

We addressed the effect of various routing algorithms and topologies on power dissipation in on chip networks. Deterministic, partially adaptive and fully adaptive routing algorithms with mesh and torus as famous topologies are examined on NoC. This paper considers the effect of low power encoding algorithm on power consumption along with different routing algorithms and topologies. We have discussed about link and total power improvement of low power encoding approach with several routing and topology in NoC with different benchmarks.

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